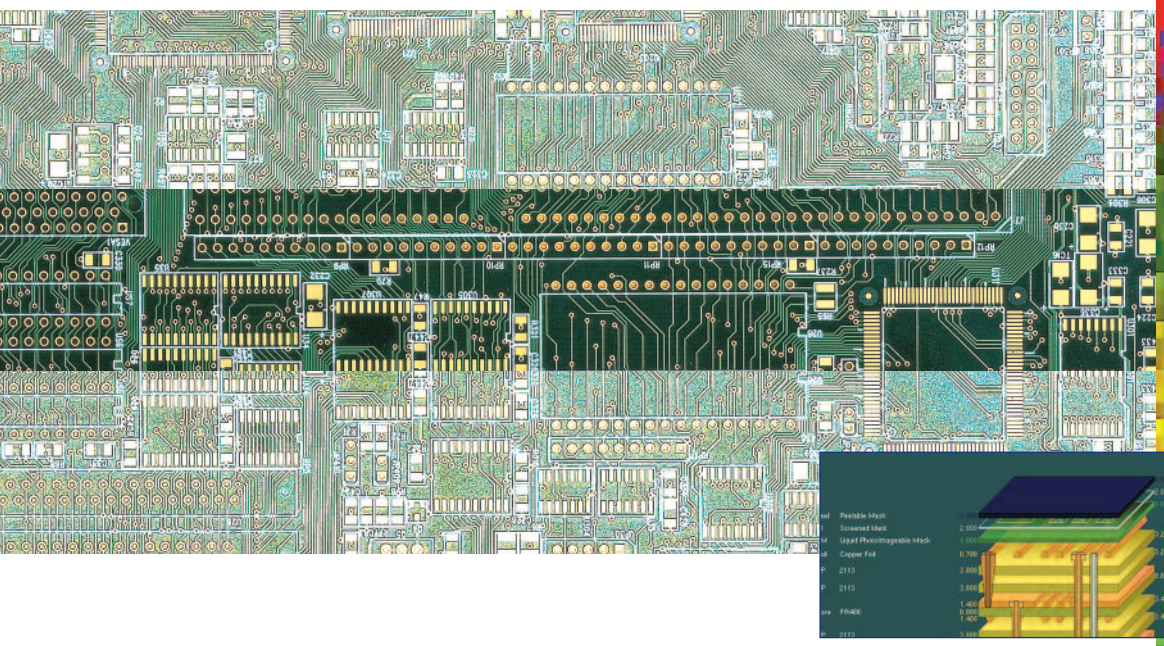
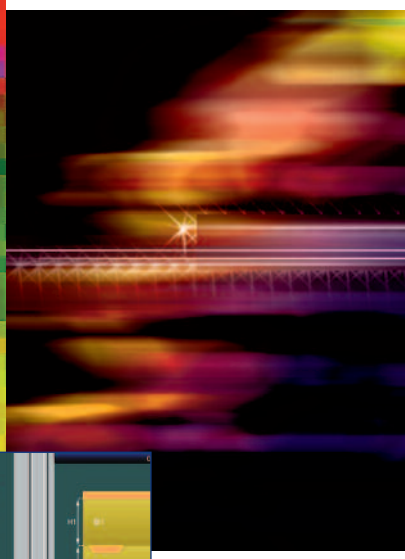
Integrated stackup design for PCB fabricators and OEM designers





Speedstack 2010
Speedstack 2010 Si
Speedstack 2010 PCB
Speedstack Coupon Generator
Speedstack Speedflex

Manual or automatic layer stackup

Supply-chain management & cost control

Error-free documentation

Transmission line modeling

Impedance control

Compatibility with third-party stackup tools

Polar

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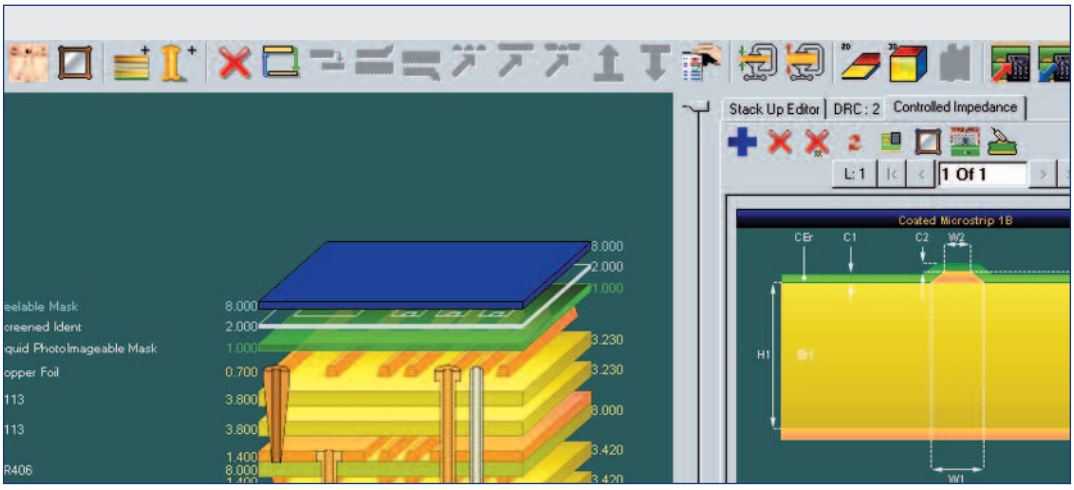
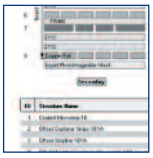


Integrated Stackup Design Environment



Speedstack is a comprehensive Integrated Stackup Design Environment for PCB fabricators and OEM engineers. By collating libraries of materials, costs and suppliers with imports of critical design data such as transmission line design or impedance control, Speedstack can predict manufacturing yields and deliver error-free documentation which can be shared with every level of the production chain. Speedstack's integrated end-to-end approach to stackup design drastically reduces the time required to create, document and control PCB layer stackups

Controlled impedance & transmission line design

Speedstack is compatible with third-party design-for-manufacture (DFM) tools from Ucamco and Zuken, allowing users to add error-free documentation to their existing DFM tools. The Speedstack family also offers versions which fully integrate with Polar design tools for transmission line design and controlled impedance. For PCB fabricators Speedstack PCB incorporates data directly from the the Polar Si8000m controlled impedance design system into the stack-up design process. OEM design engineers can combine Speedstack Si with the Polar Si9000e transmission line design system.

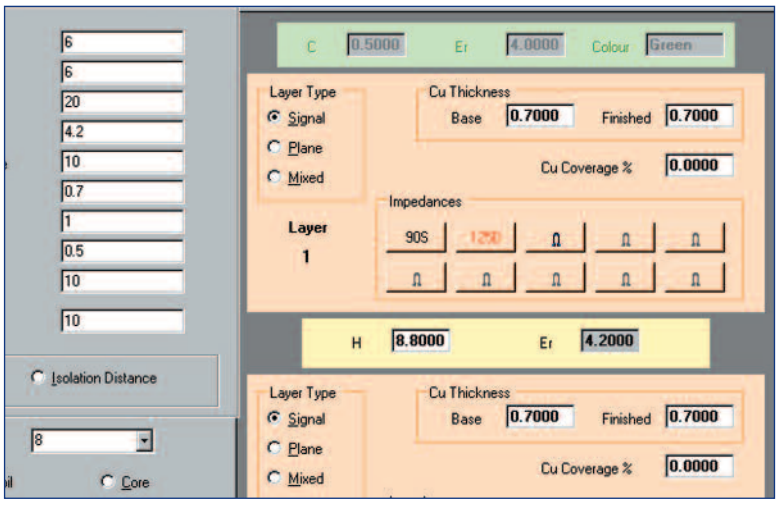
Speedstack Features

- Integrates critical data into single stackup design tool
- Enhanced supplier management and cost control
- Manual or automatic stack-up design
- Easy error-free documentation & communication
- Impedance control data for PCB fabricators (Speedstack PCB)
- Transmission line modeling for OEMs (Speedstack Si)

Speedstack 2010:	Manual or automatic stack creation & error-free documentation
Speedstack 2010 PCB:	Controlled impedance stackup design for PCB fabricators
Speedstack 2010 Si:	High-speed transmission line design for pre-layout engineering

Flexible stackup creation

Polar's Speedstack provides three levels of stackup creation: manual layer-by-layer design, a Stackup Wizard for semi-automatic design and fully automatic stack-up generation. All three methods of stack generation allow flexible manual editing of stacks to balance performance, material availability and cost. Virtual Stack Realisation performs a Monte Carlo analysis of 10,000 virtual builds of selected boards to provide an accurate prediction of manufacturing yields.



Supply chain control

Speedstack combines a generic library of materials of set dielectric thicknesses with the materials libraries from PCB base-material suppliers in the Polar Speedstack material partner programme and user-generated materials libraries. Using these libraries Speedstack can replace hours of complex calculations and eliminate guesswork when assessing how the use or substitution of different materials or suppliers may affect the final board performance.

Cost control

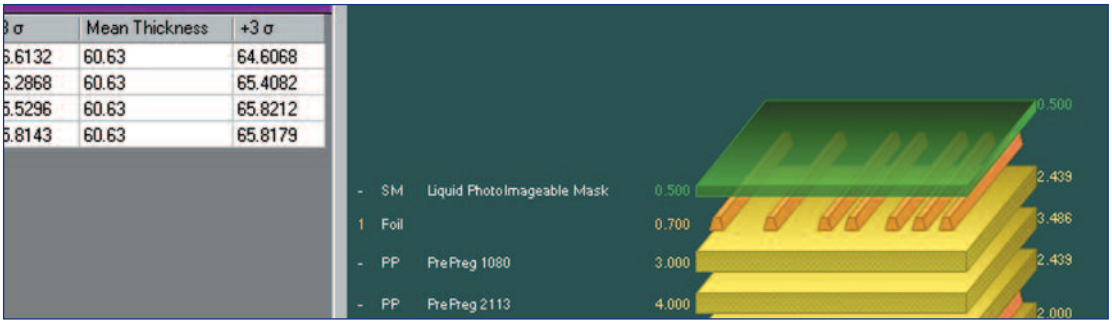
Collaboration between designers and fabricators can ensure the optimum material combinations for minimising build costs. OEMs can specify their critical performance parameters tightly, while fabricators can share their material recommendations with OEMs to ensure that the most cost-effective materials are used in the build.

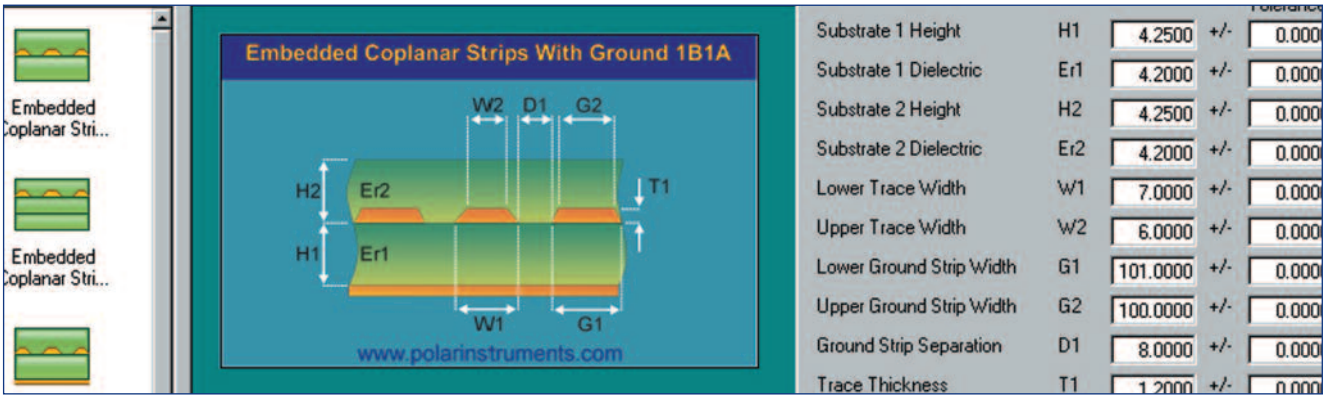
Controlled impedance test data

Speedstack Si and Speedstack PCB can output controlled impedance test files directly for each stackup. This ensures that OEMs provide clear impedance test specifications to suppliers or brokers and enables the fabricator to link the required impedance test characteristics to each build.

Clear graphical documentation

Completed stackups are presented in a graphical or report format and can be exported as a variety of file types, including Gerber, Jpeg and PDF, making it easier for the fabricator and designer to visualise and replicate the stackup design accurately. Speedstack also documents information clearly and accurately on the different materials, drill details and impedance control requirements.





Speedstack PCB for fabricators and brokers

Speedstack PCB provides PCB fabricators and PCB brokers with fast design and documentation of controlled impedance PCB stackups. With a direct link into Polar's Si8000m controlled impedance design system, Speedstack PCB allows fabricators and brokers to import impedance specifications created by OEM engineers using Speedstack Si. The proposed stackup can then be exported back to the customer or other Speedstack users within the supply chain for verification prior to pre-build tests. By sharing accurate stackup data in clear and easy-to-read formats fabricators and OEMs can collaborate more closely and resolve potential issues at the start of the fabrication process.

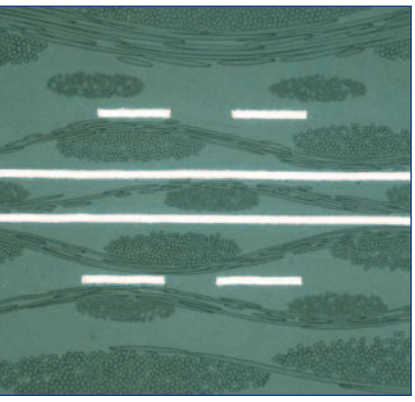
Who should use Speedstack PCB?

Supplier management

When sourcing PCBs from multiple suppliers or moving from prototype to volume production a checklist of design rules for stackup and fabrication ensures that the specific manufacturing capabilities of each supplier are factored into the stackup process. This supports the most effective choice of suppliers as well as ensuring that the chosen suppliers can meet the build criteria.

PCB fabrication

Providing each supplier with a comprehensive and easy-to-read package of Speedstack documentation eliminates communication errors and minimises the risk of critical information being missed or mis-interpreted. The Speedstack .sci file contains detailed information on the layer stackup and includes drill details and precise impedance control specifications. Documentation on the preferred stackups can be completed in minutes and shared with customers or other companies within the supply chain. This significantly reduces the engineering time and increases the accuracy of documenting stackup using the conventional formats of Excel, Word or PowerPoint.



This photograph illustrates a polished microsection of a typical glass resin composite structure. This is FR4 but could equally be any woven glass reinforced composite. Glass has a dielectric constant of 6, the resin around 3. With high frequency base materials the resin Er can be even lower. On fine geometry boards with differential traces, local variations in the material Er need to be taken into account to obtain the most accurate prediction of impedance.

When the differential pair or coplanar waveguide is designed with very close spacings, almost all the electric field occurs in the horizontal gap between the traces. This is often resin filled (as shown). A number of structures in the Si8000m allow the local Er between the traces to be defined. This is essential to maximise first-time yields.

Speedstack PCB is designed for fabricators who need to manage controlled impedance builds. Speedstack PCB uses the proven Polar Si8000m multiple dielectric boundary element field solver to provide the impedance data for the stack. In addition, Speedstack PCB licence holders have full access to the stand-alone Si8000m Quicksolver.

More about the Si8000m

Designed especially for extracting controlled impedance parameters on multiple dielectric builds, the Si8000m employs Polar's proven boundary element field-solving engine. The Si8000m is able to model a wide range of single and multiple dielectric structures. In demanding applications and high volume environments, where the highest yields need to be achieved during the production process, the Si8000 can even model resin rich areas between differential traces. The Si8000m Quicksolver supports goal seeking and impedance extraction at the click of a mouse and calculates minimum and maximum process parameters. This allows full exploration of "what if" and worst-case scenarios without the need to use Excel spreadsheets.

Enhanced Quicksolver speeds design
Powerful impedance design system
Boundary element field solver
Sensitivity analysis increases yields
Ideal for PCB design and front end
Easy graphing and sharing of data
Predict impedance tolerance
Account for local variations in dielectric constant

To further improve the PCB production process the test results and physical microsection data can be exported back into the Si8000m to discover which production process has most effect on impedance values. With experience, production processes can be altered to suit incoming material variations. For example, if a batch of core material is at or around its upper thickness limit Si8000m can be used to investigate whether altering trace dimensions within their specified range will allow the PCB to still meet the customer's specifications. If more adjustment is required the Si8000m provides easy-to-read documentation which can be shared with the original designer to allow a discussion on further alteration of the traces.

Differential impedance PCB structures
Differential coplanar impedance structures
Single-ended impedance modelling
Microstrip and stripline constructions
Field solving by Boundary Element Method – BEM
Extraction of odd, even and common impedance

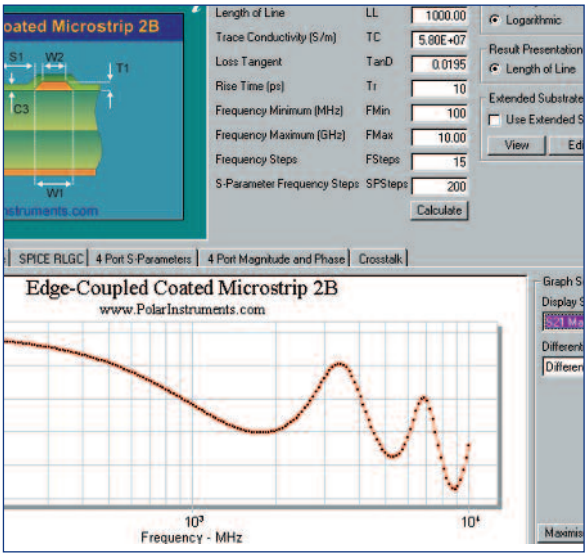
Speedstack Si for design engineers

With a direct link to the Polar Si9000e PCB transmission line design system Speedstack Si provides a comprehensive design environment which allows design engineers to create stackups in minutes. Error-free documentation ensures that the stackup specification is communicated accurately throughout the PCB supply chain. Controlled impedance test requirements can also be incorporated into the stackup and a test file can be directly exported to the Polar Controlled Impedance Test System (CITS).

Who should use Speedstack Si?

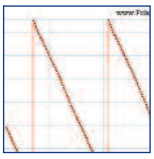
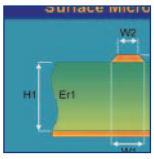
Electronic designers prior to layout design

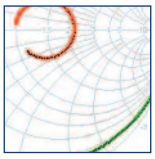
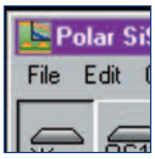
Speedstack Si quickly guides designers through the complex decisions required to create efficient stackups prior to layout. By using the Speedstack Si, material selections for layer stackup can be discussed and optimised for cost, signal integrity, manufacturability and reliability with the fabricator prior to production. Alternatively, the stackup can be created using generic materials, allowing the fabricator to fine-tune the stack-up using different materials to improve manufacturing cost and yield.

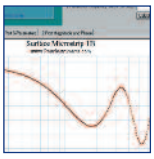
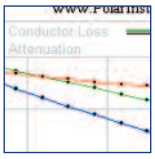


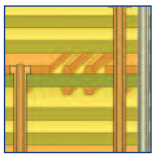
Interconnect designers

Interconnect designers can use Speedstack Si to share layer stackup and ensure that the PCB build matches the performance specified by the electronic designers and fabricators. The Stackup Controlled Impedance (.sci) file provides a convenient format for communicating accurately all build data and transmission line geometries in one simple package. Including Gerber file names in the .sci ensures the files are attached to the correct physical layer.



Speedstack Si

Speedstack Si has a direct link to the Polar Si9000e PCB transmission line design system.

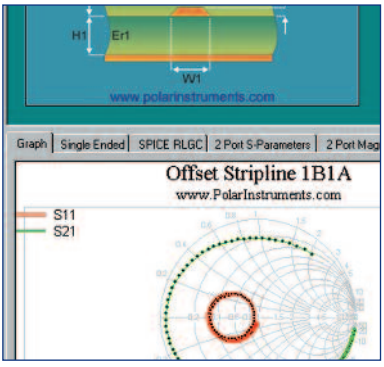
More about Si9000e:

The Si9000e PCB transmission line design system extracts full transmission line parameters to support modeling of transmission line losses.

With its fast, accurate, frequency-dependent transmission line modeling the Si9000e is designed to model loss and extract full transmission line parameters from over 90 popular PCB transmission line structures. Employing boundary element method field solving the Si9000e extracts RLGC matrices and rapidly plots a range of transmission line information for the structure that is being designed. Loss is graphed in three ways, with a clear indication of dielectric, copper and combined loss. S-parameter extraction is fast and S-parameters may be displayed graphically or output in Touchstone™ format. The Si9000e boundary element field solver also communicates with Speedstack for consistent layer stackup creation and documentation.

The Si9000e boundary element field solver also communicates with Speedstack for consistent layer stackup creation and documentation.

Si9000e can be used for single or multiple dielectric builds, and can also include solder mask performance by setting mask coverage to be adjacent, between and above traces.



Si9000e

Extracts frequency dependent impedance

Accurate BEM impedance field solver

Model odd, even, differential and common impedance

Manufacturing tolerance prediction

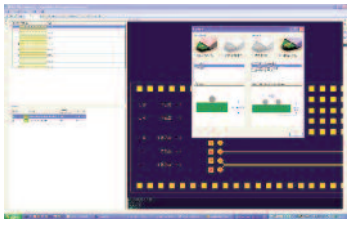
Graph copper, dielectric and combined loss

S-parameter graphs

Touchstone outputs

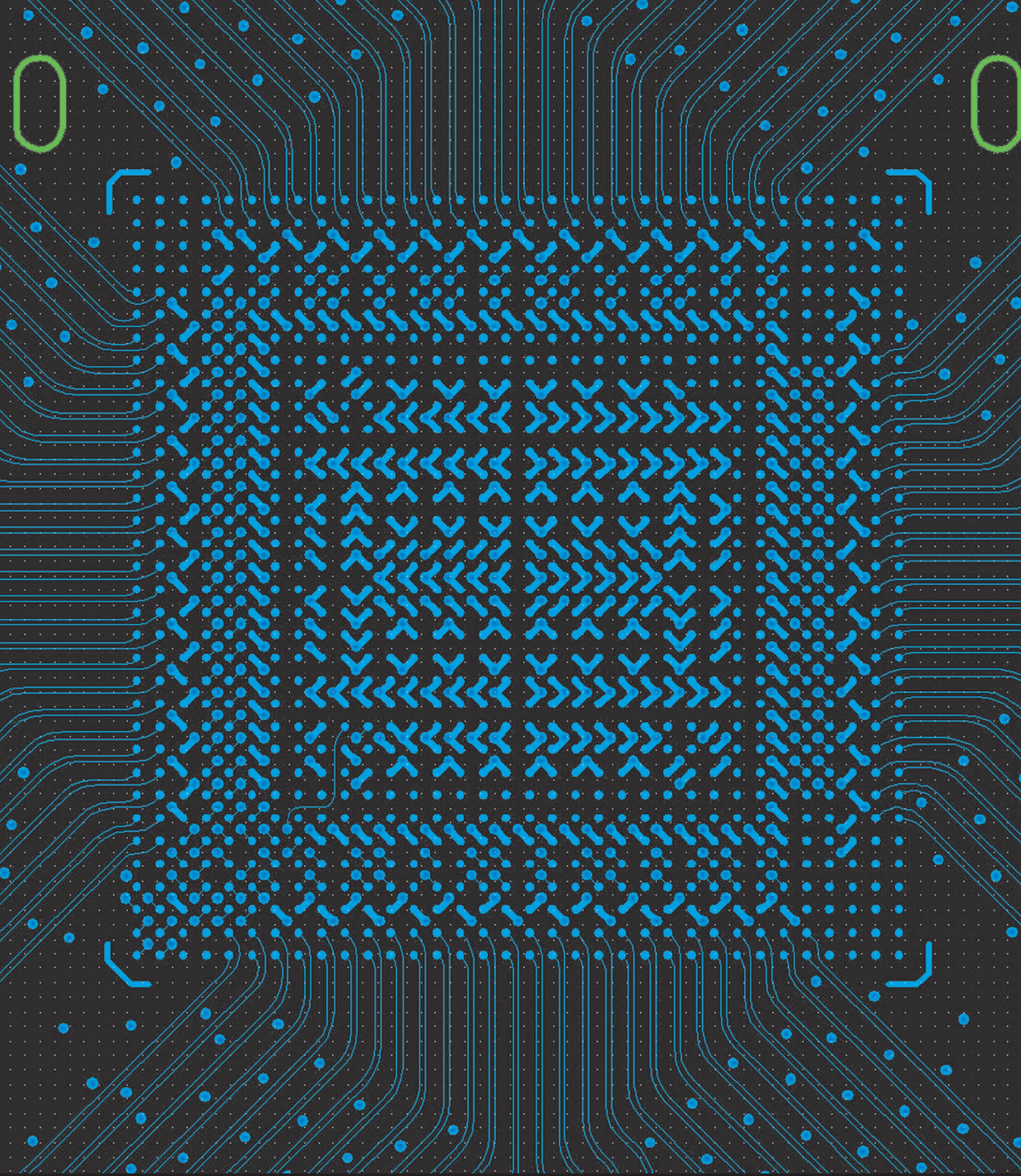
Speedflex for Speedstack

Speedflex is an option that extends Speedstack's capability into flex-rigid applications – see Speedflex literature LIT231.



Speedstack Coupon Generator

Speedstack Coupon Generator is an impedance coupon generator which generates coupons and drills for Speedstack Stackups - see Speedstack Coupon Generator literature LIT224.



Speedstack material partner program

ARLON · DOOSAN Electro-Materials · GORE · Hitachi Chemical · isola · LG Chem · MGC · nelco · Panasonic ideas for life · ROGERS CORPORATION · TACONIC · TECHNOLAM · VENTEC

A comprehensive Integrated Stackup Design Environment (ISDE) for PCB fabricators and OEM engineers

Disk missing?

If your evaluation disk is missing please contact your local Polar office or representative for a replacement.

Alternatively you can download a copy from www.polarinstruments.com

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LIT:218

Specifications

Speedstack professional stackup design system

	Speedstack 2010	Speedstack 2010 PCB	Speedstack 2010 Si
Autostackup	Yes	Yes	Yes
Max layer count	64+	64+	64+
Materials library	Yes	Yes	Yes
Build height Monte Carlo simulation	10 000 builds	10 000 builds	10 000 builds
Finished thickness compensation	Yes	Yes	Yes
User library	Yes	Yes	Yes
CITS Test file generation	No	Yes	Yes
Impedance support	No	Yes	Yes
Impedance goal seek	No	Yes	Yes
Stack documentation	Technical report Gerber .dxf .csv .jpeg	Technical report Gerber .dxf .csv .jpeg	Technical report Gerber .dxf .csv .jpeg
Impedance structures	No	90+	90+
Single ended impedance	No	Yes	Yes
Differential	No	Yes	Yes
Odd mode / even mode	No	Yes	Yes
Frequency dependent impedance	No	Yes	Yes
Skin depth	No	No	Yes
Copper losses	No	No	Yes
Dielectric losses	No	No	Yes
S-Parameter plots	No	No	Yes
Touchstone™ export	No	No	Yes
Smith chart plots	No	No	Yes

Flex-rigid stackup option – see Speedflex literature LIT231
Speedstack Coupon Generator – see Speedstack Coupon Generator literature LIT224

About Polar Instruments

Polar provides innovative and easy to use measurement, test, design tools and utilities for the PCB fabrication industry and related disciplines. Polar is best known for CITS and RITS controlled impedance test systems and professional impedance calculation tools.

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