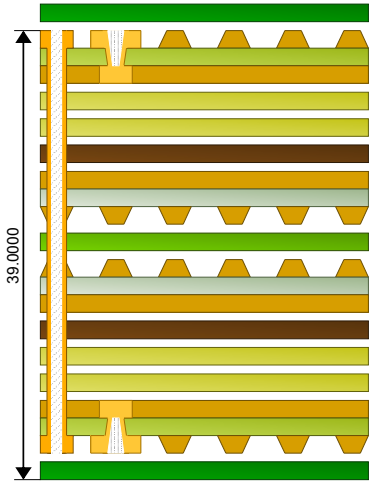
Layer	Stack up	Supplier	Supplier Description	Description	Type	Processed Thickness	Mask Thickness	εr	Color	Impedance ID
		Generic	SM/005	Photoimageable Solder Mask	SolderMask		0.700	4.000	Green	
1						1.900				1, 2, 3
		Generic		FR4 H/H Core	FR4	5.000		4.200		
2						0.700				
		Generic	FR4 1080 NF	FR4 1080 No Flow	PREPREG	2.500		4.200		
		Generic	FR4 1080 NF	FR4 1080 No Flow	PREPREG	2.500		4.200		
		Generic coverlayer	FR0110	FR0110 Coverlayer	Coverlay	2.000		3.500		
3						0.700				
		Generic	AP8525	Flexicore AP8525	Poly	2.000		3.800		
4						0.700				4, 5
		Generic	FR0111	FR0111 Bondply	Dielectric	3.000		3.800		
5						0.700				6, 7
		Generic	AP8525	Flexicore AP8525	Poly	2.000		3.800		
6						0.700				
		Generic coverlayer	FR0110	FR0110 Coverlayer	Coverlay	2.000		3.500		
		Generic	FR4 1080 NF	FR4 1080 No Flow	PREPREG	2.500		4.200		
		Generic	FR4 1080 NF	FR4 1080 No Flow	PREPREG	2.500		4.200		
7						0.700				
		Generic		FR4 H/H Core	FR4	5.000		4.200		
8						1.900				8, 9
		Generic	SM/005	Photoimageable Solder Mask	SolderMask		0.700	4.000	Green	

39.0000

Copper Thickness = 8.000 | Dielectric Thickness = 31.000 | Overall Processed Thickness = 39.000 |

Notes

Impedance ID	Structure Image	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width	Upper Trace Width	Trace Separation	Target Impedance	Tol (+/- %)	Calculated Impedance
1		1	2	0	8.187	7.187	0.000	50.000	10.000	49.750
2		1	2	0	8.113	7.113	11.887	50.000	10.000	49.960
3		1	2	0	9.406	8.406	10.594	85.000	10.000	85.050
4		4	3	6	3.469	2.469	16.531	85.000	10.000	84.740

StackName: Rigid 1	Version: 2013	Revision:	Modification:	Date of Revision:	Editor	
Date: 11/10/2012	Associated Documents:	1.001	Sample stack	11 October 2012	Martyn G	Page 2/5
Author: Richard Attrill	Stackup report generated by Polar Speedstack PCB stackup design and documentation system. Stackup courtesy of Printed Circuits Inc (c) Printed Circuits Inc 2013 (c) Polar Instruments Ltd 2013					
Department: Engineering						
Site: www.polarinstruments.com						

Impedance ID	Structure Image	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width	Upper Trace Width	Trace Separation	Target Impedance	Tol (+/- %)	Calculated Impedance
5		4	3	6	8.113	7.113	11.887	50.000	10.000	49.960
6		5	3	6	3.469	2.469	16.531	85.000	10.000	84.740
7		5	3	6	2.500	1.500	17.500	100.000	10.000	100.000
8		8	7	0	2.844	1.844	0.000	75.000	10.000	75.350
9		8	7	0	9.406	8.406	10.594	85.000	10.000	85.050

Drill Image	1st Layer	2nd Layer	Column Position	Drill Type
	1	8	1	Mechanical PTH
	1	2	2	Laser PTH
	8	7	2	Laser PTH

StackName: Rigid 1	Version: 2013	Revision:	Modification:	Date of Revision:	Editor	Page 3/5
Date: 11/10/2012	Associated Documents:	1.001	Sample stack	11 October 2012	Martyn G	
Author: Richard Attrill	Stackup report generated by Polar Speedstack PCB stackup design and documentation system. Stackup courtesy of Printed Circuits Inc (c) Printed Circuits Inc 2013 (c) Polar Instruments Ltd 2013					
Department: Engineering						
Site: www.polarinstruments.com						