Application Notes

Application Note 151

Copper thickness, edge coupled lines and characteristic impedance

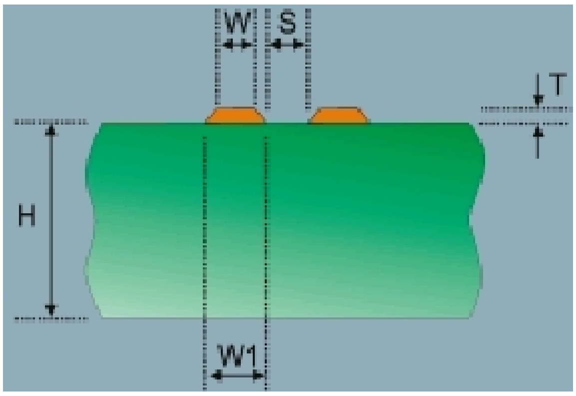
Background

Sometimes fabricators receive board specs which look unrealizable given the specifications supplied. This may be a result of a simple error from the originator of the spec, or it could be the original designer had not taken into account the constraints of the PCB fabrication process.

How do you resolve this?

If the error is clear then you obviously need to contact the originator to put things right and re issue the spec. However if there is no clear error on the spec but the board still looks impossible to make, then you need to work with all the available specs to see if the problem can be fixed by using the room to move given to you in the specification.

This application note describes just such a case with an edge coupled differential pair. This is a relatively uncommon structure as there are no reference ground planes in the design — it is a "pure" differential pair.



Edge coupled differential pair
without ground plane

The above structure relies on the coupling between the two traces, and unlike many PCB structures has no reference ground plane. This limits the number of options available to you when the structure as specified does not appear to meet specification.

Typically you would look at trace width, trace separation and material thickness when looking at options for altering impedance. On boards with a lower ground plane the trace width has a major influence.

Here is the problem and the approach taken to resolve it...

The board specification called for a board with 100 Ohm differential pair; however the dimensions specified yielded an expected impedance of 135 Ohms. The challenge was to see if it was possible to get the board to meet impedance specification without a major change in specification.

On this edge coupled differential pair there is no lower ground plane, and reducing the trace separation too much (towards 3 mil) will start to cause yield problems.

As a starting point we looked at increasing trace width towards the high side of specification, while holding the track separation constant. This did not yield enough change, so other areas were investigated. A second route was to increase both the trace width and reduce the separation; to minimise any potential routing difficulties we adjusted the Si6000b spreadsheet to add a column for Pitch between trace centers. Then any width increases caused a corresponding reduction in separation. Whilst this helped it still did not bring us close enough to a solution.

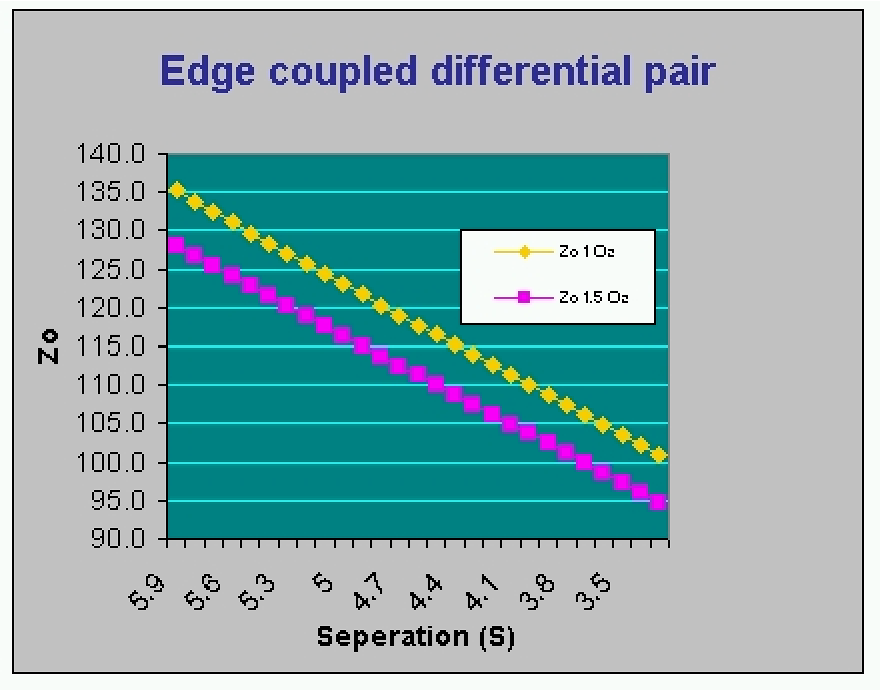
Modified Si6000 sheet allowing separation variation with constant pitch, this modification allows front end engineers to adjust trace width and separation without the need for layout changes.

H	W	W1	T	D	S	P	Er	Z/D/L/C	Zdiff
91.0	4.6	5.1	1.4	100	5.9	11	4.3	Z	135.2
91.0	4.7	5.2	1.4	100	5.8	11	4.3	Z	133.8
91.0	4.8	5.3	1.4	100	5.7	11	4.3	Z	132.4
91.0	4.9	5.4	1.4	100	5.6	11	4.3	Z	131.0
91.0	5	5.5	1.4	100	5.5	11	4.3	Z	129.7

Si6000b sheet with column added for Pitch (click picture to enlarge)
Separation then modified so s=p-w1

Finally by looking at the structure it became obvious that, as the majority of the field is between the two conductors, an increase in copper thickness should have an effect. Just how much can be shown with the Si6000b. The graph below plots two curves both for Zo whilst increasing trace width with a constant pitch between the trace centers.

The yellow curve shows how the target impedance is only achievable with a trace separation of 3 mil (~75µm) while the bottom trace shows that if the copper is plated up to 1.5 ounces, the desired impedance can be achieved at a more comfortable spacing of around 4 mils.



Increasing copper weight by
1/2 ounce helps reduce Zo in
this case by 5 to 7 Ohms

Modifying designs.
By using the graphing capabilities of the Si6000b, PCB fabricator and designer can feed data between themselves so minimising any problems in the fabrication process. **More information?**

Further information on measuring PCB controlled impedances is available by email from martyn.gaudion@polarinstruments.com

For information on field solving impedance design software please contact: ken.taylor@polarinstruments.com

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