Application Note 169

Using the Si8000 field solver to model changes of thickness of LPI solder mask between traces

Printed circuit boards are often prototyped at a prototype/quick turn specialist shop before hand over to a volume plant. This note explains how impedance may be affected when the prototype shop and the volume fabricator deploy different soldermask application methods. We describe how the Polar Instruments Si8000 Field Solver can be use to predict changes in the final impedance value of LPI coated differential traces due to non-uniform coating thickness (particularly between finely separated differential traces). We briefly mention some of the most popular application methods for Liquid Photoimageable Soldermask (LPI), and note that these different methods can result in finished board impedances different from the design value.

Silk screen print

The silk screen print method applies the LPI to the board with a squeegee blade through a tensioned mesh. Ink deposit is controlled by varying the mesh count and print settings, speed, angle and pressure. Semi-automatic screen print-applied LPISM is the most prevalent solder mask application method today. Non-uniformity of coating can result from the "damming" effect on the leading edge of the trace in the direction of the squeegee movement. There is compression of the screen on the crown of the trace which results in extremely thin coating(s) and in the case of differential traces, the flooding effect in the space between the traces must be taken into account. All affect the resulting impedance.

Curtain-coat

With the curtain-coat technique LPI is applied as the printed circuit board passes through a sheet, or *curtain*, of low viscosity ink falling through a narrow slot. Curtain-coating is widely practised and well understood within the board manufacturing industry. Curtain coating exhibits a coating variation phenomenon unique to its method — "shadowing". Shadowing is the occurrence of reduced solder mask on the trailing edge of traces parallel to the curtain compared with the leading edge of those traces. The trace passing through the curtain presents a dam-like effect causing the build-up of mask on the leading edge of the trace, and reducing the mask on the trailing side of the trace.

Electrostatic spray

In the electrostatic spray technique LPI is applied from a rotating bell, which, aided by compressed air, atomizes the ink, and deposits it on the PCB. The LPI is given a negative charge and the PCB is earthed so the LPI is attracted to the board. However, the electrostatic effect tends to attract the LPI to the copper areas, resulting in less than uniform coating.

Air spray

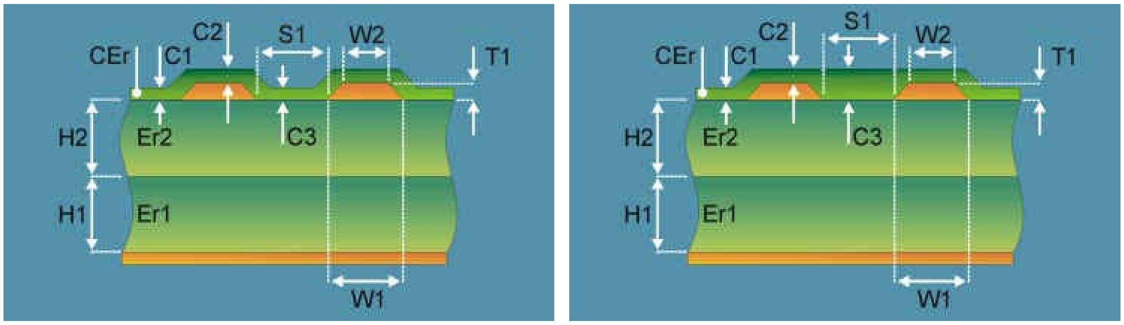
Using air-spray the LPI is applied using single or multiple spray gun(s). The ink is atomized by mixing with decompressing air. Uniform coating can prove difficult to achieve as multiple gun spray systems have a tendency to form stripes, due to overlap or interference between adjacent guns, across the board.

The problems are exacerbated if one technique is used to produce pre-production engineering samples and another to manufacture the final product. The actual differential impedance value of the traces on the finished board can be several ohms different from the design value if the thickness of the LPI coating between the traces changes significantly.

In structures such as the edge-coupled coated microstrip below, the final differential impedance value will decrease as the coating thickness C3 increases.

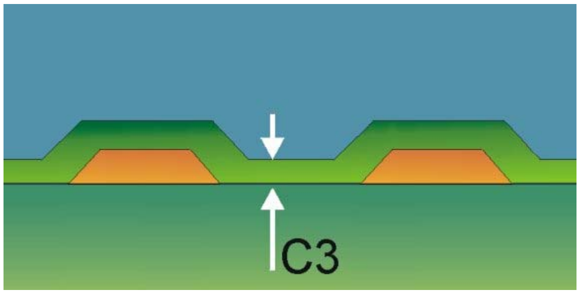
Modelling LPI thickness between differential traces

The Polar Si8000 allows the designer to calculate impedance changes with changes in C3. In this example we use the Si8000m Quick Solver to model the structure with the coatings at minimum and maximum values.

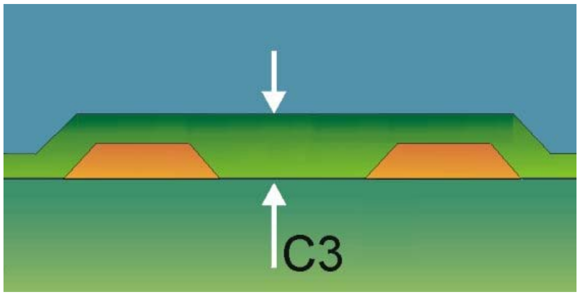


Si8000 models of edge-coupled surface microstrip showing different coating thicknesses between traces.

Solder mask thickness between traces is given by C3 in the Si8000 structure diagrams above . Magnified views of the gaps between traces showing different LPI fills are shown below.

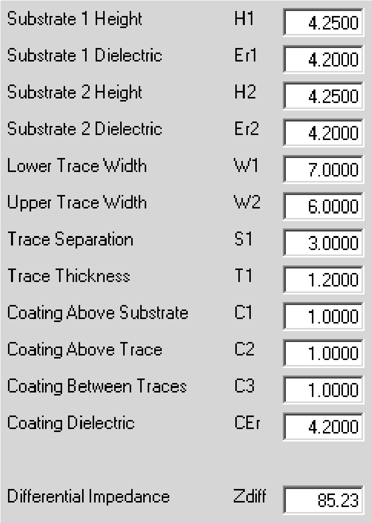


Minimum fill

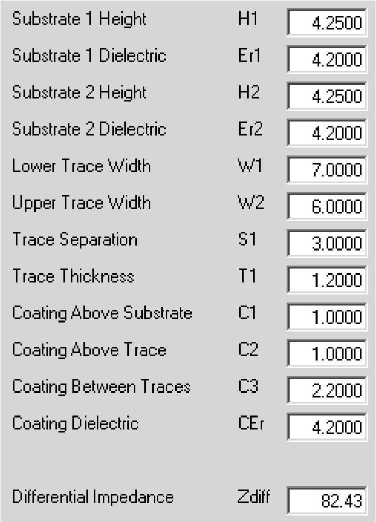


Maximum fill

The Si8000 Quick Solver values and solutions for the structures above are shown below



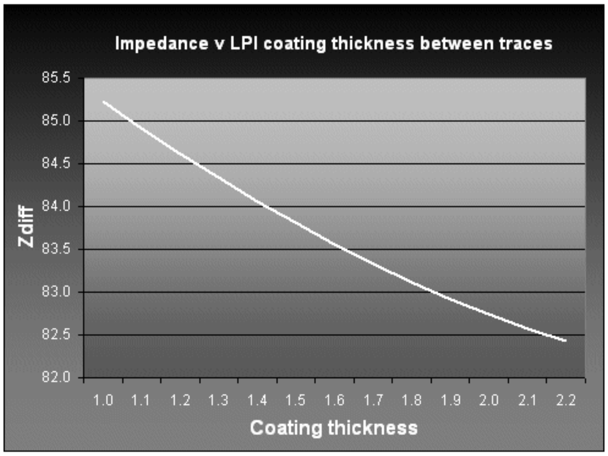
Substrate 1 Height	H1	4.2500
Substrate 1 Dielectric	Er1	4.2000
Substrate 2 Height	H2	4.2500
Substrate 2 Dielectric	Er2	4.2000
Lower Trace Width	W1	7.0000
Upper Trace Width	W2	6.0000
Trace Separation	S1	3.0000
Trace Thickness	T1	1.2000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Between Traces	C3	1.0000
Coating Dielectric	CEr	4.2000
Differential Impedance	Zdiff	85.23



Substrate 1 Height	H1	4.2500
Substrate 1 Dielectric	Er1	4.2000
Substrate 2 Height	H2	4.2500
Substrate 2 Dielectric	Er2	4.2000
Lower Trace Width	W1	7.0000
Upper Trace Width	W2	6.0000
Trace Separation	S1	3.0000
Trace Thickness	T1	1.2000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Between Traces	C3	2.2000
Coating Dielectric	CEr	4.2000
Differential Impedance	Zdiff	82.43

Using the parameters above we observe an approximately 3% decrease in differential impedance between minimum and maximum coating thicknesses between traces. The impedance change will depend on the separation between the traces.

Using the Si8000 Excel interface we can model the changes in impedance over a range of values of C3.



The graph above illustrates the change in impedance against coating thickness between the traces.

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