



**PWB Interconnect Solutions Inc.**

103-235 Stafford Road West  
Nepean, Ontario  
Canada  
K2H 9C1  
Email: [pwb@pwbcorp.com](mailto:pwb@pwbcorp.com)  
URL: [Http://pwbcorp.com](http://pwbcorp.com)

**Tel (613) 596-4244**  
**Fax (613) 596-2200**



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## **Rationale For IST Testing Temperatures – Ambient to 150C**

### **Introduction**

Reliability of electronic hardware is defined as the probability that a system, product or component can perform its intended functions for a specified interval of time under stated conditions. Ensuring high reliability requires good practices in manufacturing, the selection of base materials/components, design, testing and maintenance. The history of accelerated stress testing goes back over 40 years, when various companies involved in the manufacture and use of military and commercial products developed protocols to quantify the inherent reliability of the printed wiring board (PWB) interconnections.

The test regime included cyclic exposures to anticipated temperature extremes, generally  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The upper level was established knowing that the materials in the test vehicles were exceeding their glass transition ( $T_g$ ) temperature. In the '60s and '70s the most commonly used base materials were di-functional and usually measured  $T_g$ s between  $115^{\circ}\text{C}$  and  $120^{\circ}\text{C}$ . In today's PWBs the standard material types are multi-functional or blended epoxies, designed to achieve a  $T_g$  between  $160^{\circ}\text{C}$  and  $180^{\circ}\text{C}$ . Although the materials have undergone tremendous advancements, the industry standard (IPC or Mil spec's) testing methodologies have remained unchanged; the reality of this  $T_g$  progression is that testing protocols have a maximum test temperature below  $T_g$ ; this will limit the user's ability to discern latent reliability concerns, due to the inability to create sufficient stress required to uncover the potential defects.

The influence of the negative temperatures on the stress applied to PWBs (specifically bare boards) has never been truly characterized, although consensus is held that solder joint reliability testing definitely benefits from the negative temperature environment.

Recent advancements in accelerated stress testing methods and protocols have confirmed that the majority of damage and cycles fatigue created within the interconnect structures are caused in two primary situations; 1) The elevated temperatures, times at/to temperatures and the number of potential cycles experienced in the assembly/rework environment are responsible for the majority of damage caused or created to the interconnect structure. 2) The temperature transition at the elevated stage of the heating cycle and the immediate/initial phase of the cooling cycle are responsible for the stress which leads to the damage to various interconnect structures.



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One widely accepted industry test method is Interconnect Stress Testing (IST); this tool offers many advantages over traditional oven testing. The primary benefits include fast time to results, stopping the stressing exactly when the test vehicles reach the 10% rejection criteria, 260<sup>0</sup> C temperature capability, very friendly user interface, minimal operator time, excellent repeatability and reproducibility and a growing acceptance of IST as the industry standard testing methodology.

Companies involved in the military, aerospace, avionic, automotive and telecom industries are required to simulate conditions where their products experience temperatures below an ambient environment. The obvious question regarding the IST testing protocol is directed toward the uncertainties in performance differences between accelerated testing from an ambient state (22<sup>0</sup> C) and a traditional test that achieves a negative state of -55<sup>0</sup> C. This document will discuss the results of testing completed that characterizes how materials change at different temperature and the potential influences of how stress is applied to the interconnect structures.

### **IST - Reliability Testing and the Effect of Negative Temperatures**

IST testing is typically performed at temperature ranges between 22<sup>0</sup> C (ambient) and 150<sup>0</sup> C. IST test equipment can achieve much higher temperatures (up to 275<sup>0</sup> C), which are used to simulate the temperature experienced during component assembly and rework. IST equipment has no capability to test below ambient and some have suggested that the inability to test into negative temperatures is a significant limitation in reliability testing of printed wire boards (PWB). An explanation is offered in this report why the IST testing philosophy (ambient and above) is a better reliability test method than the traditional -55<sup>0</sup> C to 125<sup>0</sup> C. Confirmation is offered in this report that IST has consistently achieved correlation with thermal cycling ovens that cycle to the negative temperatures extremes.

Also, with the impending legislation of "Lead Free" RoHS requirements, and new findings based on reliability test data of "microvia" interconnections there is compelling evidence that thermal cycle testing above 150<sup>0</sup> C may be necessary to detect discrepant product or identify products that may not survive the upper temperature extremes experienced during lead free assembly and rework.

### **IST Temperature Range Rationale**

Conventional oven testing equipment is generally limited to an upper temperature of approximately 160<sup>0</sup> C, while IST testing can achieve temperatures up to 275<sup>0</sup> C (in 3 minutes). The need for quick time to results and capability of higher test temperatures for specific types of interconnections are demanding a change from conventional testing with its inherent limits to the more adaptable IST testing methodologies.



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IST testing equipment has a greater flexibility in the upper temperature limit, and the temperature ranges adopted for standard IST evaluations (ambient to 150C) were established in response to 3 major considerations:

1. By not taking the time to reach the negative temperatures, time to results can be significantly reduced. The cycle time from ambient to the required elevated temperature and back again is between 4 and 5 minutes; this allows IST testing to achieve between 288 and 360 thermal cycles in 24 hours. A traditional thermal cycling oven typically achieves 24 to 48 cycles in 1 day. The ability of IST equipment to achieve faster cycles supports the industries need for shorter time to results that are required for Just In Time (JIT) manufacturing, product acceptance and process monitoring and control. IST's fast cycling better meets the demands of today's business environment.

2. The traditional IST test temperature of 150<sup>0</sup> C was established back in the early '90s in relation to the dielectric material Tgs being used at that time. The typical Tg of tetra-functional and multifunctional resins was about 135<sup>0</sup> C to 150<sup>0</sup> C. By testing below Tg coupons are exposed to "Z-axis" coefficient of thermal expansion (CTE) that are relatively constant, with a range of about 20 to 50 ppm/C. Near and above Tg there is a significant change in CTE (up to 300 ppm/C) and testing in that range is producing faster results without changing the failure mode. Since the temperatures of most end-use environments will not exceed the Tg of the material, testing at 150<sup>0</sup> C was adopted. Now with the advent of higher Tg (160<sup>0</sup> C to 180<sup>0</sup> C) materials there is serious consideration for increasing the test temperatures to higher than 150<sup>0</sup> C.

3. Quantifying and simulating assembly and rework have always been part of IST testing protocol. Coupons are subjected to "preconditioning" at 230<sup>0</sup> C or 260<sup>0</sup> C on the system prior to 150<sup>0</sup> C IST testing. The typical solder temperature preconditioning cycles have been established at 3 or 6 thermal excursions to 230<sup>0</sup> C. The typical lead free temperature preconditioning cycles have been established at 3 or 6 thermal excursions to 260<sup>0</sup> C. This preconditioning is from ambient to 230<sup>0</sup> C or 260<sup>0</sup> C in exactly 3 minutes. There are many different thermal profiles established for assembly of printed circuit boards (PCB). Assembly cycles vary greatly within the electronics industry. The goal with IST preconditioning is not to replicate the exact thermal profile of a reflow oven but to establish one prescribed method against which all test results may be compared. By establishing a preconditioning standard of 230<sup>0</sup> C or 260<sup>0</sup> C in 3 minutes the vagaries of different procedures are eliminated and all data are relatively comparable. It is important to note that assembly never starts with parts at negative temperatures; a range of ambient to high temperatures is appropriate in assembly and rework simulation.



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**Test Temperature Comparisons:**

There are 5 testing and preconditioning temperatures that have been established in IST evaluations. The standard testing is performed from ambient to 150<sup>0</sup> C. Microvias are now being tested from ambient to 190<sup>0</sup> C. Flex circuits with thin dielectrics and adhesive systems are being tested from ambient to 210<sup>0</sup> C. Preconditioning is being performed from ambient to 230<sup>0</sup> C for tin/lead or 260<sup>0</sup> C to emulate lead free assembly and rework.

The standard IST testing is 22<sup>0</sup> C to 150<sup>0</sup> C for a delta of 128<sup>0</sup> C in 4 to 5 minutes. Conventional ovens are typically limited to test from -50<sup>0</sup> C to 125<sup>0</sup> C for a delta of 175<sup>0</sup> C in 60 minutes. IST evaluations, however, are not limited to 150<sup>0</sup> C and testing can be increased to 275<sup>0</sup> C. IST evaluations achieve these temperatures in 3 minutes. A protocol of 22<sup>0</sup> C to 260<sup>0</sup> C in 3 minutes produces a ramp rate of 84<sup>0</sup> C/minute and a temperature delta of 238<sup>0</sup> C. Conventional ovens by comparison achieve a ramp rate of 6<sup>0</sup> C/minute and a delta of only 175<sup>0</sup> C. The rate of temperature rise will effect the thermal cycle results; this is why IST evaluations have been shown to be about 30% more effective in finding known latent defective boards, compared with thermal cycling ovens.

Table 1 is a comparison of IST protocols and a standard thermal oven protocol. The difference in the two methods' temperatures, heating cycles, ramp rates, cycle times, etc. are offered for review. The slow test rate of thermal cycling ovens allows coupons to de-stress or accommodate expansion, during the thermal cycle; faster cycles times produce faster results with less variation. It should be noted that virtually all PCB failure modes occur during the heating cycle or immediately upon entering the cooling cycle.

**IST vs. Conventional Thermal Cycling**

**Table 1**

	IST						Oven
	Standard	Microvia	Flex Cir.	Precon.	Lead Free	Maximum	Standard
<b>Test Temperature</b>	<b>150</b>	<b>190</b>	<b>210</b>	<b>230</b>	<b>260</b>	<b>275</b>	<b>125</b>
<b>Start Temperature</b>	<b>22</b>	<b>22</b>	<b>22</b>	<b>22</b>	<b>22</b>	<b>22</b>	<b>-50</b>
<b>Temp Delta</b>	<b>128</b>	<b>168</b>	<b>188</b>	<b>208</b>	<b>238</b>	<b>253</b>	<b>175</b>
<b>Time to Temp</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>10</b>
<b>Ramp Rate <sup>0</sup> C /Min</b>	<b>43</b>	<b>56</b>	<b>63</b>	<b>69</b>	<b>79</b>	<b>84</b>	<b>18</b>
<b>Cycle Time</b>	<b>5</b>	<b>5</b>	<b>5</b>	<b>5</b>	<b>5</b>	<b>5</b>	<b>60</b>
<b>Cycles/Day</b>	<b>288</b>	<b>288</b>	<b>288</b>	<b>288</b>	<b>288</b>	<b>288</b>	<b>24</b>



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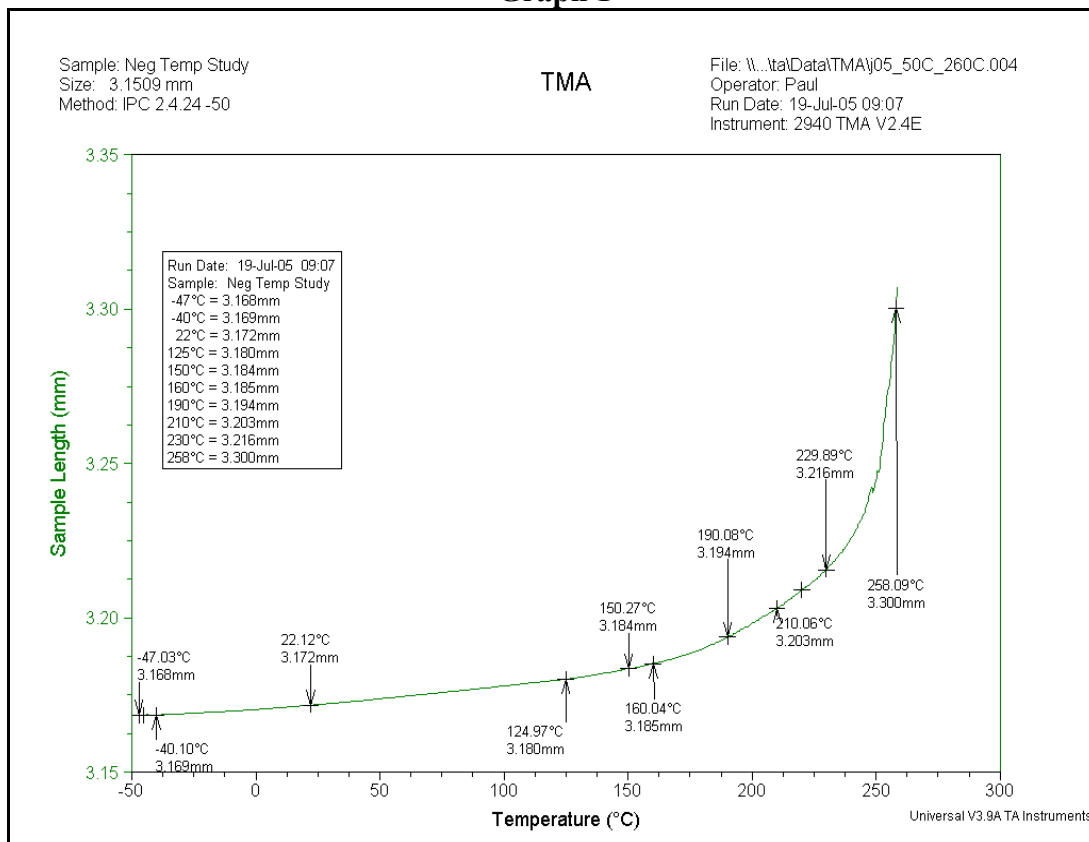
## Thermal Analysis of Material

Material studies suggest that the most significant and interesting changes in the dielectric materials (used in PWB fabrication) occur at temperatures near and above ambient.

**Thermal Mechanical Analysis** - Most of the stress in a PWB is due to Z-axis expansion during thermal excursion. The expansion of material and the coefficient of thermal expansion (CTE) can be measured accurately using Thermal Mechanical Analysis (TMA). TMA measures the changes in thickness of a sample over a range in temperatures. The rate of “Z-axis expansion” is relatively constant from  $-50^{\circ}\text{C}$  to the  $T_g$  of the material. The example below (Graph 1) demonstrates that the CTE below  $T_g$  is a constant  $25\text{ ppm}^{\circ}\text{C}$ . Above  $T_g$  the CTE increases to  $179\text{ ppm}^{\circ}\text{C}$ . In the example below the sample dimension changed from  $3.008\text{ mm}$  at  $-40^{\circ}\text{C}$  to  $3.172\text{ mm}$  at ambient ( $22^{\circ}\text{C}$ ). At  $150^{\circ}\text{C}$  the same sample measured  $3.184\text{ mm}$ ; that is a  $.006\text{ mm}$  change from  $-40^{\circ}\text{C}$  to  $22^{\circ}\text{C}$  and  $.012\text{mm}$  from  $22^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ . At  $190^{\circ}\text{C}$  the sample size increased to  $3.194\text{ mm}$  and at  $230^{\circ}\text{C}$ ,  $3.216\text{ mm}$ . At  $260^{\circ}\text{C}$ , the temperatures achieved in lead free assembly, the sample has increased  $.135\text{mm}$  to  $3.307\text{ mm}$ . Below  $T_g$  the amount of change per degree is constant and small. Approaching  $T_g$  the rate increases dramatically and above  $T_g$  the rate of change is 300% to 500%.

### Thermal Mechanical Analysis of a PWB

Graph 1





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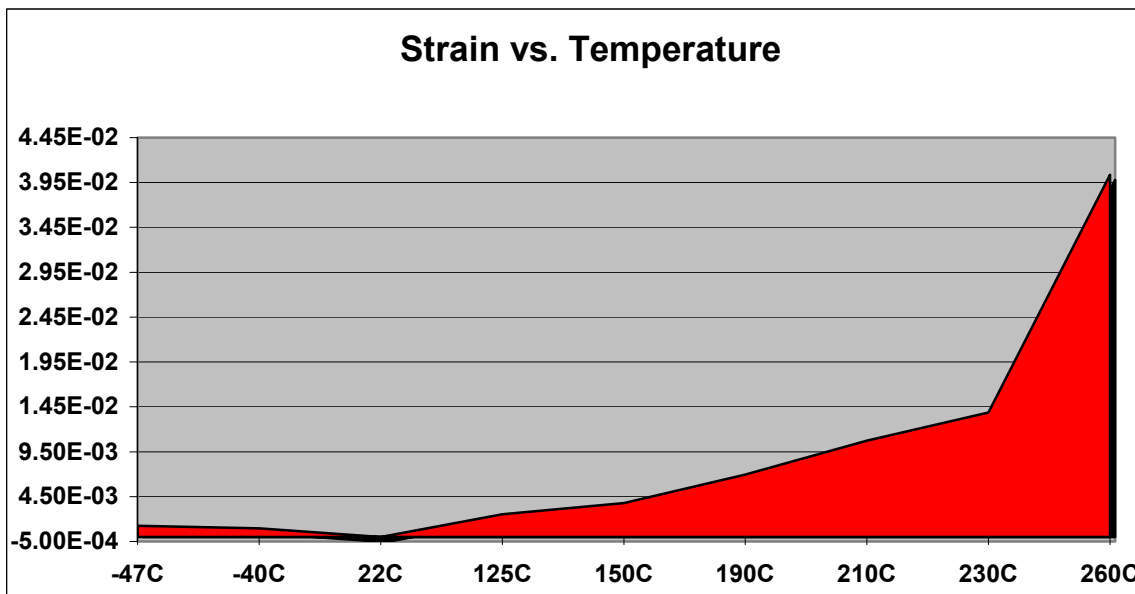


Strain ( $\epsilon$ ) is defined as the change in length divided by the initial length. For this study we chose a sample measuring 3.172 mm at ambient and measured the change in Z-axis from  $-47^{\circ}\text{C}$  to  $258^{\circ}\text{C}$ . Since the printed circuit board is manufactured at ambient temperature the initial length of 3.172 mm at  $22^{\circ}\text{C}$  is considered strain free. At  $-40^{\circ}\text{C}$  the strain on the sample was  $9.46 \times 10^{-4}$  (compressive stress). From ambient to  $125^{\circ}\text{C}$  the strain increased to  $2.5 \times 10^{-3}$  approximately 2.5 times greater at  $125^{\circ}\text{C}$  than at  $-40^{\circ}\text{C}$ . At  $150^{\circ}\text{C}$  there is 4 times more strain in the sample than at  $140^{\circ}\text{C}$ . There is much more strain induced into the system from testing at temperatures above ambient than that exerted below ambient.

**Strain In Material Due to Z-axis Expansion/Contraction**  
**Table 2**

Test Temperatures vs. Strain									
	Lowest	Oven Min	Ambient	Oven Norm	IST	Microvia	Flex	Sn/Pb	RoHS
Temp	-47C	-40C	22C	125C	150C	190C	210C	230C	260C
Length	3.168	3.169	3.172	3.180	3.184	3.194	3.206	3.216	3.300
Delta L	0.004	0.003	0	0.008	0.012	0.022	0.034	0.044	0.128
Strain	1.26E-03	9.46E-04	0.00E+00	2.52E-03	3.78E-03	6.94E-03	1.07E-02	1.39E-02	4.04E-02

**Graph of Strain at Test Temperatures**  
**Graph 2**



**Dynamic Mechanical Analysis** – The stress on a printed circuit board is influenced by the amount of strain from “Z-axis” expansion and the viscoelastic properties of the dielectric expressed as Young’s Modulus (storage modulus). The elasticity of a material is best measured with Dynamic Mechanical Analysis (DMA). DMA measures, among other things, the change in the elastic state of materials over a temperature range. Typically the Young’s Modulus is



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increasing at a low relative constant rate from  $-40^{\circ}\text{C}$  to the  $T_g$  of the material, usually around  $170^{\circ}\text{C}$ . The most interesting changes occur well above ambient; typically the Storage Modulus  $T_g$  occurs at  $160^{\circ}\text{C}$  to  $180^{\circ}\text{C}$  in the epoxy systems currently used in PWB fabrication. Results suggest an 11% reduction in elasticity from ambient to  $150^{\circ}\text{C}$  and 56% reduction at  $200^{\circ}\text{C}$ . The important point is that the rate of change is constant until the sample reaches  $T_g$  after which there is a sharp decrease in elasticity.

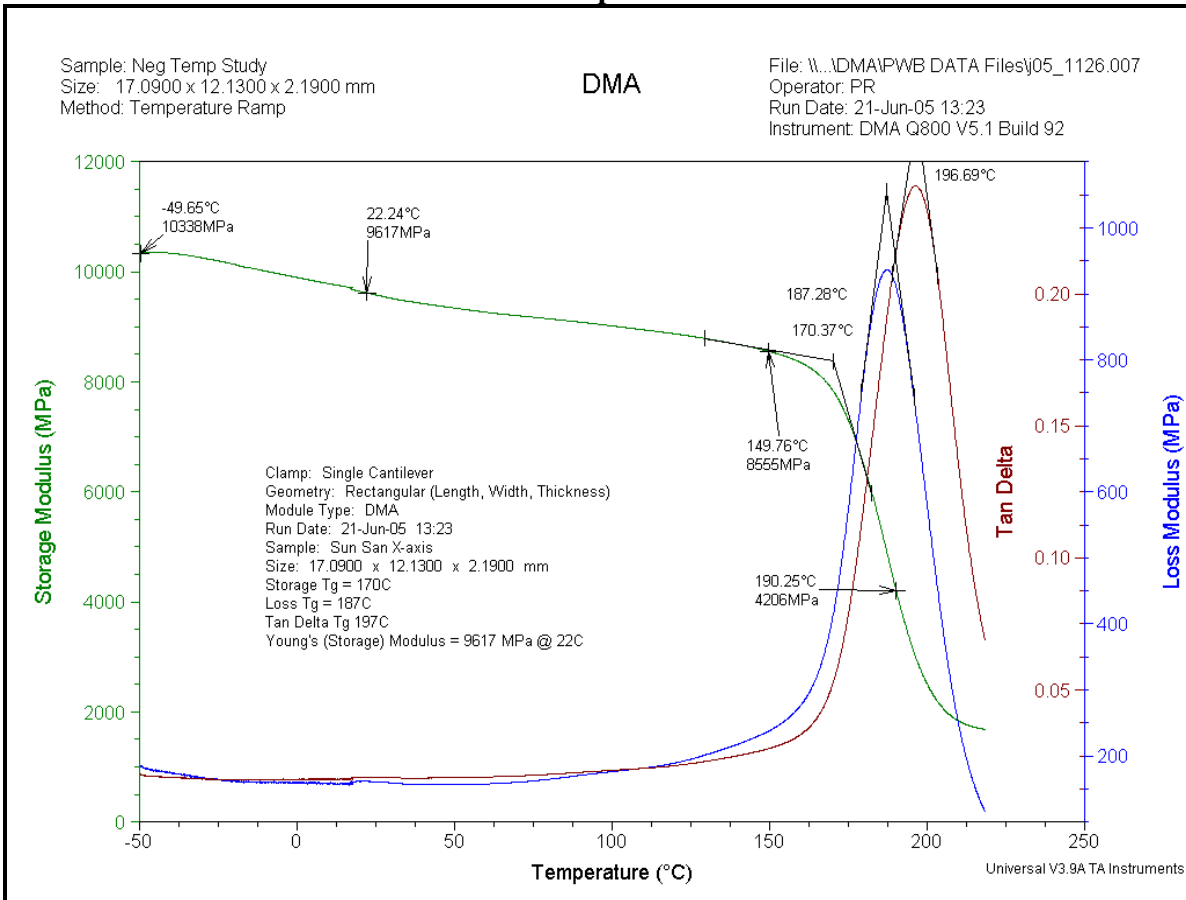
### DMA Results -40 to +200C

Table 3

	DMA				
	Tgs	-40C	22C	150C	200 C
Loss M	187 C	175 MPa	163 MPa	238 MPa	580 MPa
Tan Delta	197 C				
Storage M	170 C	10338 MPa	9617 MPa	8555 MPa	4206 MPa
% Change		7%	0%	-11%	-56%

### Dynamic Mechanical Analysis

Graph 3





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**Current Trends and Findings:**

Recent studies have shown that microvias require testing above Tg. PWB Interconnect Solutions Inc. has recently established the testing of microvia should be thermal cycled to 190<sup>0</sup> C. Testing at 190<sup>0</sup> C allows enough thermal expansion to cause a compromised microvia to fail in less than 500 cycles and at the same time does not produce any artifacts in the failure mode. Testing at 150C will produce mean time to failure well in excess of 1000 cycles. Testing at temperatures higher than 190<sup>0</sup> C produces faster time to results but, upon microscopic analysis, the failure mode may not reflect the same failure mechanisms that are experienced in assembly or the end-use environment.

**Conclusion:**

The most influential factors affecting reliability of PWBs are best tested using temperature ranges from ambient to near or above the Tg of the material. For certain structures (microvias) IST testing offers the advantage of easily testing above Tg. The high temperatures and fast thermal cycling of IST offers quicker time to results with greater sensitivity, accuracy and reproducibility than conventional oven thermal cycling. This faster cycle time is achieved by not testing below ambient and since the IST test method has been demonstrated to be more accurate at finding discrepant product than conventional oven thermal cycling protocols, testing below ambient is becoming academic.

Paul Reid

A handwritten signature in blue ink that reads "Paul Reid". The signature is written in a cursive, flowing style.

Program Coordinator  
PWB Interconnect Solution Inc.