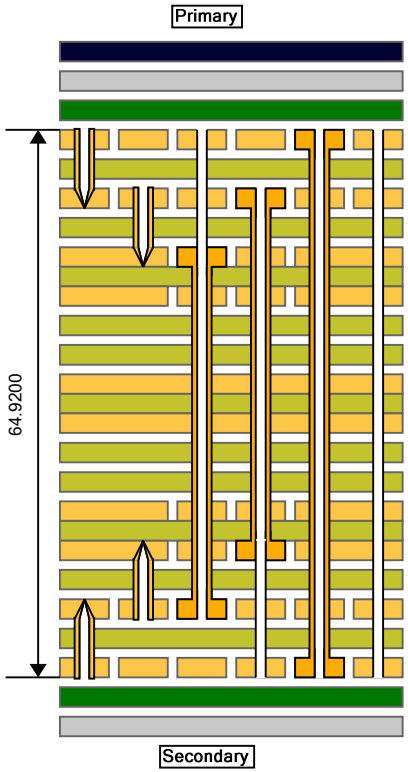

Layer	Stack up	Supplier Description	Description	Stock Number	Base Thickness	Finish Thickness	εr	Impedance ID	N1
		PE/001	Peelable Mask	700-001					
		ID/001	Screened Ident	600-001					
		SM/001	Liquid PhotoImageable Mask	500-001			4.000		
1		FO/001	Copper Foil	100-001	0.700	1.400		1, 2, 3	
		PP/001	PrePreg 1080	300-001	3.000	3.000	4.200		
2		FO/001	Copper Foil	100-001	0.700	1.400		4	
		PP/001	PrePreg 1080	300-001	3.000	3.000	4.200		
3					1.400	1.400			
		CO/020	FR4 Core	400-020	12.000	12.000	4.200		
4					1.400	1.400		5	
		PP/003	PrePreg 3113	300-003	4.000	4.000	4.200		
		PP/003	PrePreg 3113	300-003	4.000	4.000	4.200		
5					1.400	1.400			
		CO/002	FR4 Core	400-002	2.000	2.000	4.200		
6					1.400	1.400			
		PP/003	PrePreg 3113	300-003	4.000	4.000	4.200		
		PP/003	PrePreg 3113	300-003	4.000	4.000	4.200		
7					1.400	1.400		6	
		CO/020	FR4 Core	400-020	12.000	12.000	4.200		
8					1.400	1.400			
		PP/001	PrePreg 1080	300-001	3.000	3.000	4.200		
9		FO/001	Copper Foil	100-001	0.700	1.400		7	
		PP/001	PrePreg 1080	300-001	3.000	3.000	4.200		
10		FO/001	Copper Foil	100-001	0.700	1.400		8, 9, 10	
		SM/001	Liquid PhotoImageable Mask	500-001			4.000		
		ID/001	Screened Ident	600-001					

Impedance ID	Structure Name
1	Coated Microstrip 1B
2	Coated Microstrip 1B
3	Edge Coupled Coated Microstrip 1B
4	Embedded Microstrip 1B1A
5	Edge Coupled Offset Stripline 1B1A
6	Edge Coupled Offset Stripline 1B1A
7	Embedded Microstrip 1B1A

StackName: 10-Layer Sample Print Stack	Version: A	Revision:	Modification:	Date of Revision:	Editor	Page 1/2
Date: 17/06/2006	Associated Documents:	2	3113 swp to 1080	31/3/09	JAS	
Author: James Stapley		3	made 10 Layer	13/5/09	JAS	
Department: Engineering						
Site: Waterlooville						

Impedance ID	Structure Name
8	Edge Coupled Coated Microstrip 1B
9	Coated Microstrip 1B
10	Coated Microstrip 1B

Notes

PCB Thickness = 1.6 mm (+/- 10%) -
1) Finished thicknesses (i.e. isolation distances) must be complied (within a +/- 10 % manufacturing tolerance) with to ensure consistent crosstalk characteristics and impedance.
2) Track and gap width may be modified to meet target impedances. This must be approved by engineering Dept. before PCB manufacture can commence.
3) If impedance targets cannot be met by modifying track geometries alone then dielectric thicknesses may be modified. This must be approved by engineering Dept. before PCB manufacture can commence.
4) To aid manufacturing via sizes may to modified and Cross-hatching may be added to outer layers, but must be placed a least 250 thou (6.35mm) away from any tracks, pads or board outline.
5) PCB must be tested to CAD net list supplied.
6) Min plating down barrels of holes 25um.
7) This PCB is to be supplied 2 up per panel. Scrap in panel acceptable.

StackName: 10-Layer Sample Print Stack	Version: A	Revision:	Modification:	Date of Revision:	Editor	Page 2/2	
Date: 17/06/2006	Associated Documents:	2	3113 swp to 1080	31/3/09	JAS		
Author: James Stapley		3	made 10 Layer	13/5/09	JAS		
Department: Engineering							
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