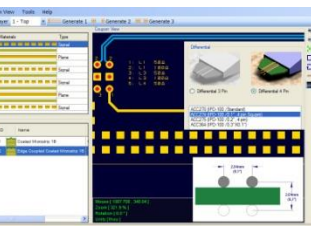
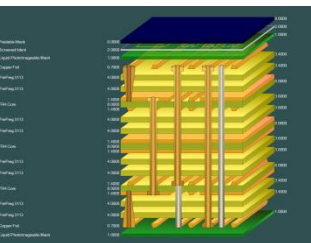
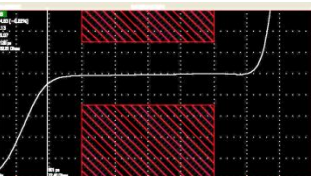
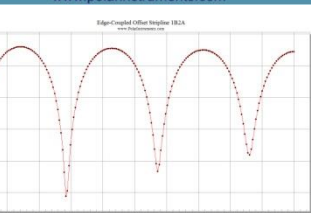
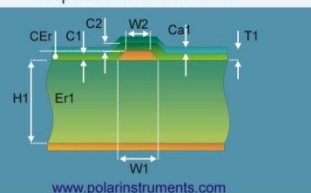




Speedstack 2018 Introduction

Richard Attrill / John Lee – Aug 2018 (Rev 6)

Impedance calculation



A brief note regarding the major enhancements in Speedstack 2018.

The application and licensing changes for Speedstack 2018 are significant. If you are an existing customer currently running Speedstack 2017 or earlier, please note that all Speedstack Si and Speedstack PCB users in an organisation will need to simultaneously upgrade in order to use the 2018 license.

Importantly, as Speedstack allows comprehensive bidirectional copy and paste into Si8000m / Si9000e and CGen it is important that all products are updated to the 2018 editions at the same time.

During 2018 there have been four releases of Speedstack.

V18.08 (August)

- Import and export for industry-standard IPC-2581 Rev B files
- Eight new coplanar structures added, requested specifically for flex and rigid-flex designs
- Online Library - new On-Premise Mode

V18.05 (May)

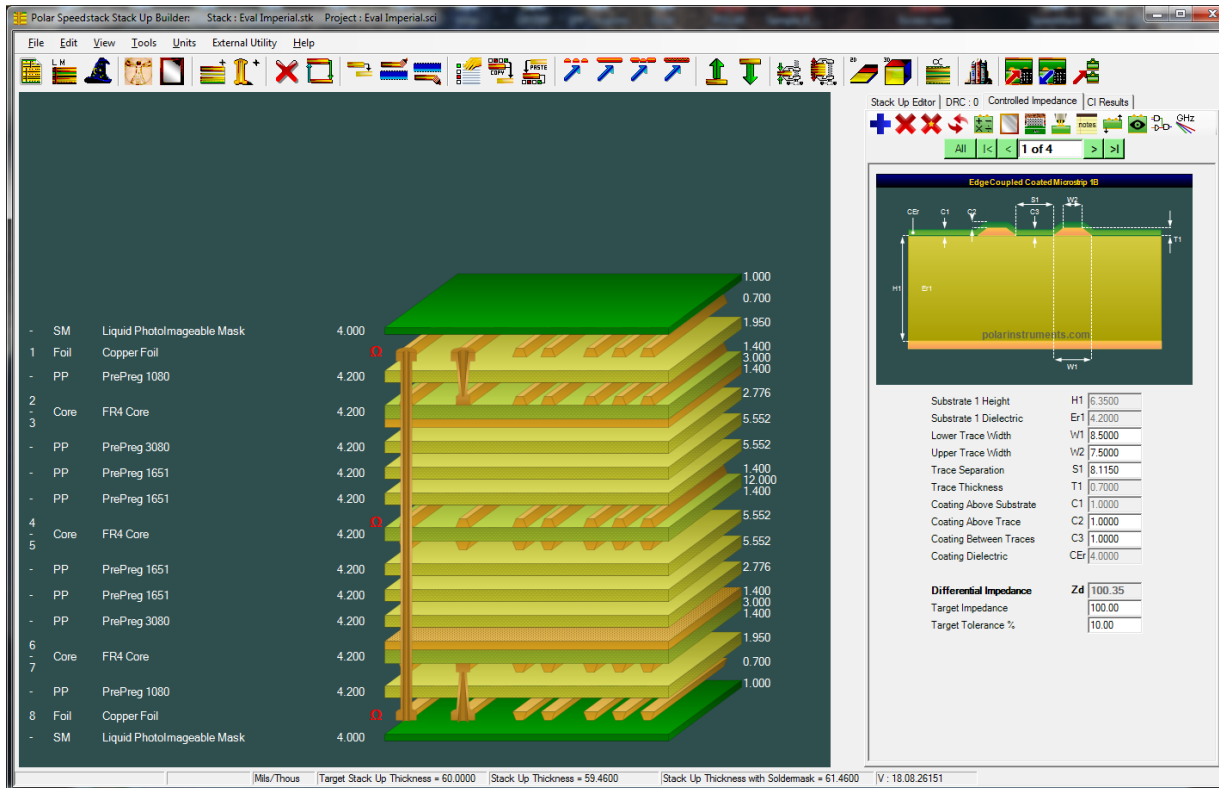
- New Cannonball-Huray method added to Surface Roughness Compensation options

V18.03 (March) / V18.01 (January)

- Full insertion loss data per structure including roughness modelling methodology
- Insertion loss graphs and data in reports
- Rich copy / paste insertion loss data to / from Si9000e
- Export insertion loss projects to Si9000e

Speedstack v18.08 (August 2018)

Import / Export industry-standard IPC-2581 Rev B files

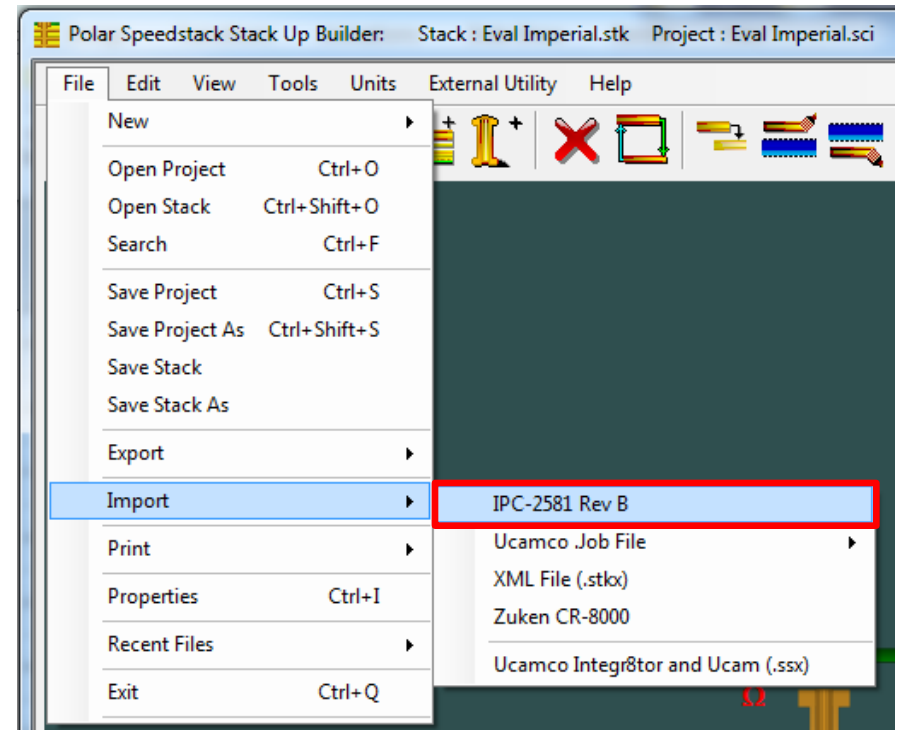
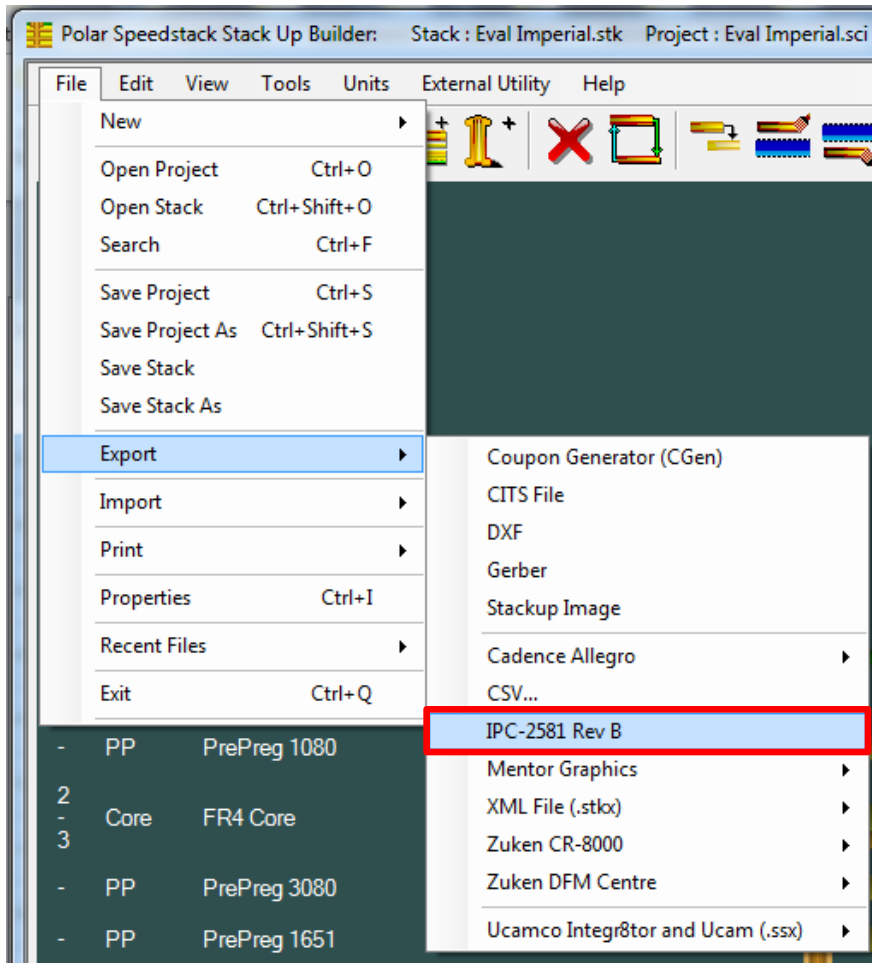


Speedstack v18.08 can export and import stack up and impedance structure data using the IPC-2581 Rev B XML file format



Other popular EDA tools can export and import IPC-2581 files, allowing easy exchange of stack up data with Speedstack

Import / Export industry-standard IPC-2581 Rev B files



New Export and Import IPC-2581 Rev B options introduced to the File menu

Export to IPC-2581 Rev B

Speedstack 2018 Introduction

A new dialog guides the user through the **Export** process.

Useful file info including Revision and Units (IPC-2581 support Inches, Millimetres and Microns)
No support for Mils / Thou

Export IPC-2581 Rev B

IPC-2581 File Information

Filename: C:\Program Files\Polar\Speedstack\Samples\Eval\Imperial.xml

Revision: B

Units: INCH

Software Package (that generated the file)

Name: Speedstack

Revision: 18.8.26151

Vendor: Polar Instruments Ltd

Export

Cancel

Notes: 1

Export Options

☒ Export Target Impedance as the IPC-2581 Impedance data

☐ Export Calculated Impedance as the IPC-2581 Impedance data

Assign Note field value as Loss Tangent: None

Assign resin rich Dielectric Constant value: 3.5000

Display Options

User-selectable options to control how the IPC-2581 data is to be exported from Speedstack

Software Package details the application that generated the IPC-2581 file. In this case Speedstack

IPC-2581 CONSORTIUM

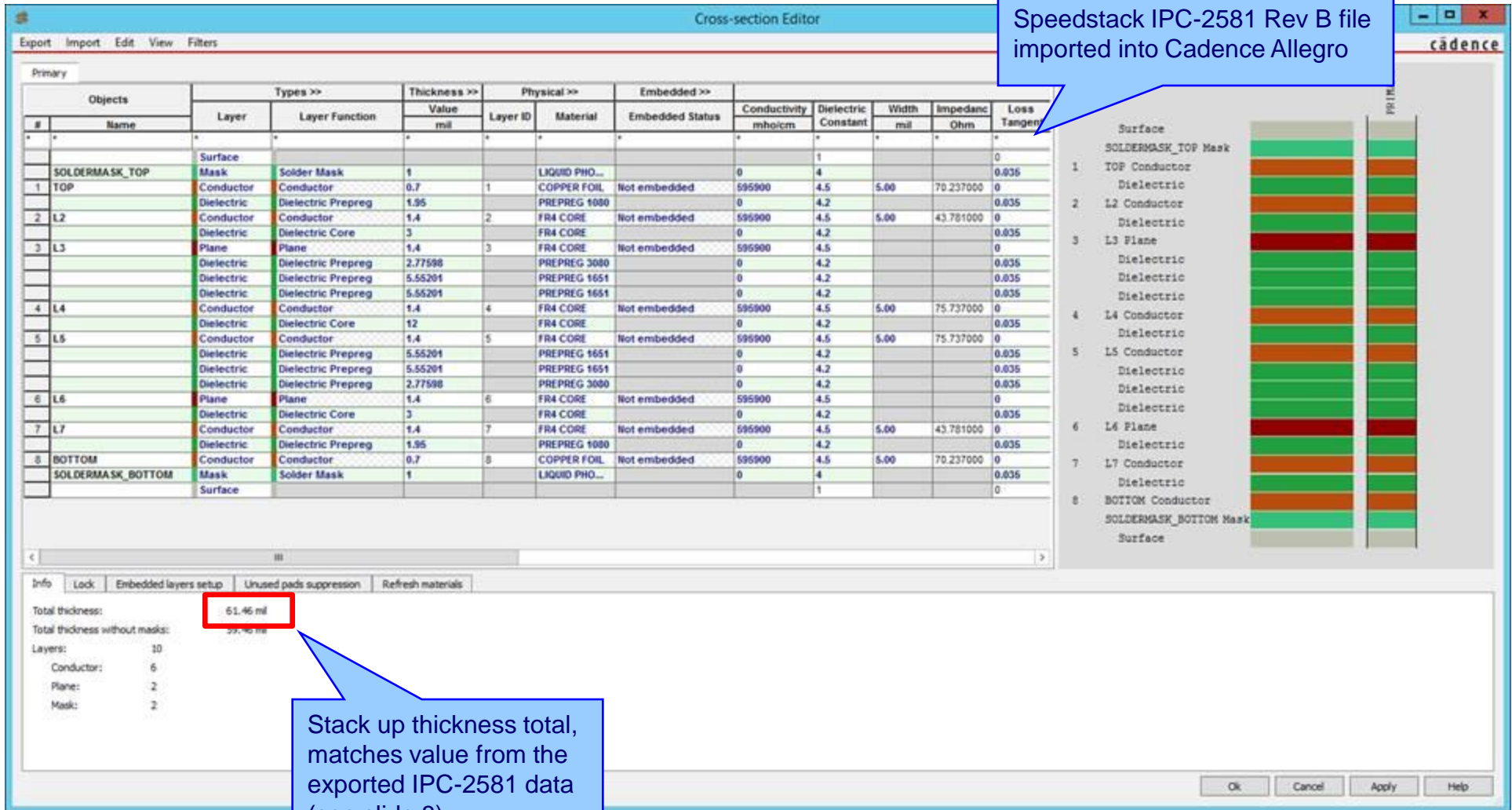
Speedstack Layer Number	Layer Name	Specification Name	Layer Function	Side	Thickness	TolPlus	TolMinus	Sequence	Material Description	Resin Content
	SOLDERMASK_TOP	SOLDERMASK_TOP_SPEC	SOLDERMASK	TOP	0.001000	0.000000	0.000000	1	Liquid PhotoImageable Mask	
1	L1	L1_SPEC	SIGNAL	TOP	0.000700	0.000000	0.000000	2	Copper Foil	
	DIELECTRIC_1	DIELECTRIC_1_SPEC	DIELECTRIC	INTERNAL	0.001950	0.000000	0.000000	3	PrePreg 1080	60.00
2	L2	L2_SPEC	SIGNAL	INTERNAL	0.001400	0.000000	0.000000	4	FR4 Core	
	DIELECTRIC_2	DIELECTRIC_2_SPEC	DIELECTRIC	INTERNAL	0.003000	0.000000	0.000000	5	FR4 Core	60.00
3	L3	L3_SPEC	PLANE	INTERNAL	0.001400	0.000000	0.000000	6	FR4 Core	
	DIELECTRIC_3	DIELECTRIC_3_SPEC	DIELECTRIC	INTERNAL	0.002776	0.000000	0.000000	7	PrePreg 3080	60.00
	DIELECTRIC_4	DIELECTRIC_4_SPEC	DIELECTRIC	INTERNAL	0.005552	0.000000	0.000000	8	PrePreg 1651	47.00
	DIELECTRIC_5	DIELECTRIC_5_SPEC	DIELECTRIC	INTERNAL	0.005552	0.000000	0.000000	9	PrePreg 1651	47.00
4	L4	L4_SPEC	SIGNAL	INTERNAL	0.001400	0.000000	0.000000	10	FR4 Core	
	DIELECTRIC_6	DIELECTRIC_6_SPEC	DIELECTRIC	INTERNAL	0.012000	0.000000	0.000000	11	FR4 Core	46.00
5	L5	L5_SPEC	SIGNAL	INTERNAL	0.001400	0.000000	0.000000	12	FR4 Core	
	DIELECTRIC_7	DIELECTRIC_7_SPEC	DIELECTRIC	INTERNAL	0.005552	0.000000	0.000000	13	PrePreg 1651	47.00
	DIELECTRIC_8	DIELECTRIC_8_SPEC	DIELECTRIC	INTERNAL	0.005552	0.000000	0.000000	14	PrePreg 1651	47.00
	DIELECTRIC_9	DIELECTRIC_9_SPEC	DIELECTRIC	INTERNAL	0.002776	0.000000	0.000000	15	PrePreg 3080	60.00
6	L6	L6_SPEC	PLANE	INTERNAL	0.001400	0.000000	0.000000	16	FR4 Core	
	DIELECTRIC_10	DIELECTRIC_10_SPEC	DIELECTRIC	INTERNAL	0.003000	0.000000	0.000000	17	FR4 Core	60.00
7	L7	L7_SPEC	SIGNAL	INTERNAL	0.001400	0.000000	0.000000	18	FR4 Core	
	DIELECTRIC_11	DIELECTRIC_11_SPEC	DIELECTRIC	INTERNAL	0.001950	0.000000	0.000000			
	SOLDERMASK_BOTTOM_SPEC	SOLDERMASK_BOTTOM_SPEC	SOLDERMASK	BOTTOM	0.001000	0.000000	0.000000			
					0.061460					

Stack up to be exported to IPC-2581 shown in data grid form. The Layer Function determines the layer / material type

Stack up thickness total

The Foil, Prepreg, Core and Solder Mask material data grid colours are determined by the Speedstack Configuration, so colour scheme familiar to users

Speedstack IPC-2581 Rev B file imported into Cadence Allegro



Objects		Types >>		Thickness >>	Physical >>		Embedded >>								
#	Name	Layer	Layer Function	Value mil	Layer ID	Material	Embedded Status	Conductivity mho/cm	Dielectric Constant	Width mil	Impedance Ohm	Loss Tangent			
		Surface							1			0			
	SOLDERMASK_TOP	Mask	Solder Mask	1		LIQUID PHO...		0	4			0.035			
1	TOP	Conductor	Conductor	0.7	1	COPPER FOIL	Not embedded	595900	4.5	5.00	70.237000	0			
		Dielectric	Dielectric Prepreg	1.95		PREPREG 1080		0	4.2			0.035			
2	L2	Conductor	Conductor	1.4	2	FR4 CORE	Not embedded	595900	4.5	5.00	43.781000	0			
		Dielectric	Dielectric Core	3		FR4 CORE		0	4.2			0.035			
3	L3	Plane	Plane	1.4	3	FR4 CORE	Not embedded	595900	4.5			0			
		Dielectric	Dielectric Prepreg	2.77598		PREPREG 3080		0	4.2			0.035			
		Dielectric	Dielectric Prepreg	5.55201		PREPREG 1651		0	4.2			0.035			
		Dielectric	Dielectric Prepreg	5.55201		PREPREG 1651		0	4.2			0.035			
4	L4	Conductor	Conductor	1.4	4	FR4 CORE	Not embedded	595900	4.5	5.00	75.737000	0			
		Dielectric	Dielectric Core	12		FR4 CORE		0	4.2			0.035			
5	L5	Conductor	Conductor	1.4	5	FR4 CORE	Not embedded	595900	4.5	5.00	75.737000	0			
		Dielectric	Dielectric Prepreg	5.55201		PREPREG 1651		0	4.2			0.035			
		Dielectric	Dielectric Prepreg	5.55201		PREPREG 1651		0	4.2			0.035			
		Dielectric	Dielectric Prepreg	2.77598		PREPREG 3080		0	4.2			0.035			
6	L6	Plane	Plane	1.4	6	FR4 CORE	Not embedded	595900	4.5			0			
		Dielectric	Dielectric Core	3		FR4 CORE		0	4.2			0.035			
7	L7	Conductor	Conductor	1.4	7	FR4 CORE	Not embedded	595900	4.5	5.00	43.781000	0			
		Dielectric	Dielectric Prepreg	1.95		PREPREG 1080		0	4.2			0.035			
8	BOTTOM	Conductor	Conductor	0.7	8	COPPER FOIL	Not embedded	595900	4.5	5.00	70.237000	0			
	SOLDERMASK_BOTTOM	Mask	Solder Mask	1		LIQUID PHO...		0	4			0.035			
		Surface							1			0			

Info Lock Embedded layers setup Unused pads suppression Refresh materials

Total thickness: **61.46 mil**

Total thickness without masks: 59.46 mil

Layers: 10

Conductor: 6

Plane: 2

Mask: 2

Stack up thickness total, matches value from the exported IPC-2581 data (see slide 8)

Import from IPC-2581 Rev B

A new dialog guides the user through the **Import** process.

Useful file info including Revision and Units (IPC-2581 support Inches, Millimetres and Microns)
No support for Mils / Thou

Speedstack 2018 Introduction

Import IPC-2581 Rev B

IPC-2581 File Information

Filename: C:\Program Files\Polar\Speedstack\Samples\xs_Test_stackup_modi

Revision: B

Units: MILLIMETER

Software Package (that generated the file)

Name: Allegro

Revision: allegro_17.2S004(8/25/2016)

Vendor: Cadence

Import

Cancel

Notes: 1

Import Options

☒ Assign IPC-2581 as Material Supplier

☒ Assign IPC-2581 Layer Name(s) as Material Type

☒ Calculate Upper Trace Widths (W2) using Default Etch Factor

Assign imported Loss Tangent to Notes field: [Note 1]

Display Options

To app

IPC-2581 CONSORTIUM

Speedstack Layer Number	Layer Name	Specification Name	Layer Function	Side	Thickness	TolPlus	TolMinus	Sequence	Material Description	Resin Content
	SOLDERMASK_TOP	SPEC_LAYER_SOLDERMASK_TOP	SOLDERMASK	TOP	0.02000	0.00000	0.00000	1	FR-4	
1	TOP	SPEC_LAYER_TOP	CONDUCTOR	TOP	0.04250	0.00000	0.00000	2	CU_17.5+25	
	DIELECTRIC_INDEX_3	SPEC_LAYER_DIELECTRIC_INDEX_3	DIELPREG	INTERNAL	0.15000	0.00000	0.00000	3	FR-4	
2	INT2	SPEC_LAYER_INT2	PLANE	INTERNAL	0.01750	0.00000	0.00000	4	CU_17.5	
	DIELECTRIC_INDEX_5	SPEC_LAYER_DIELECTRIC_INDEX_5	DIELPREG	INTERNAL	0.33000	0.00000	0.00000	5	FR-4	
3	INT3	SPEC_LAYER_INT3	PLANE	INTERNAL	0.01750	0.00000	0.00000	6	CU_17.5	
	DIELECTRIC_INDEX_7	SPEC_LAYER_DIELECTRIC_INDEX_7	DIELCORE	INTERNAL	0.10000	0.00000	0.00000	7	POLYIMIDE	
4	INT4	SPEC_LAYER_INT4	CONDUCTOR	INTERNAL	0.01750	0.00000	0.00000	8	CU_17.5	
	DIELECTRIC_INDEX_9	SPEC_LAYER_DIELECTRIC_INDEX_9	DIELPREG	INTERNAL	0.13000	0.00000	0.00000	9	FR-4	
	DIELECTRIC_INDEX_10	SPEC_LAYER_DIELECTRIC_INDEX_10	DIELCORE	INTERNAL	0.10000	0.00000	0.00000	10	POLYIMIDE	
5	INT5	SPEC_LAYER_INT5	PLANE	INTERNAL	0.01750	0.00000	0.00000	11	CU_17.5	
	DIELECTRIC_INDEX_12	SPEC_LAYER_DIELECTRIC_INDEX_12	DIELPREG	INTERNAL	0.33000	0.00000	0.00000	12	FR-4	
6	INT6	SPEC_LAYER_INT6	PLANE	INTERNAL	0.01750	0.00000	0.00000	13	CU_17.5	
	DIELECTRIC_INDEX_14	SPEC_LAYER_DIELECTRIC_INDEX_14	DIELPREG	INTERNAL	0.15000	0.00000	0.00000	14	FR-4	
7	BOTTOM	SPEC_LAYER_BOTTOM	CONDUCTOR	BOTTOM	0.04250	0.00000	0.00000	15	CU_17.5+25	
	SOLDERMASK_BOTTOM	SPEC_LAYER_SOLDERMASK_BOTTOM	SOLDERMASK	BOTTOM	0.02000	0.00000	0.00000	16	FR-4	
	STACKUP THICKNESS				1.50250					

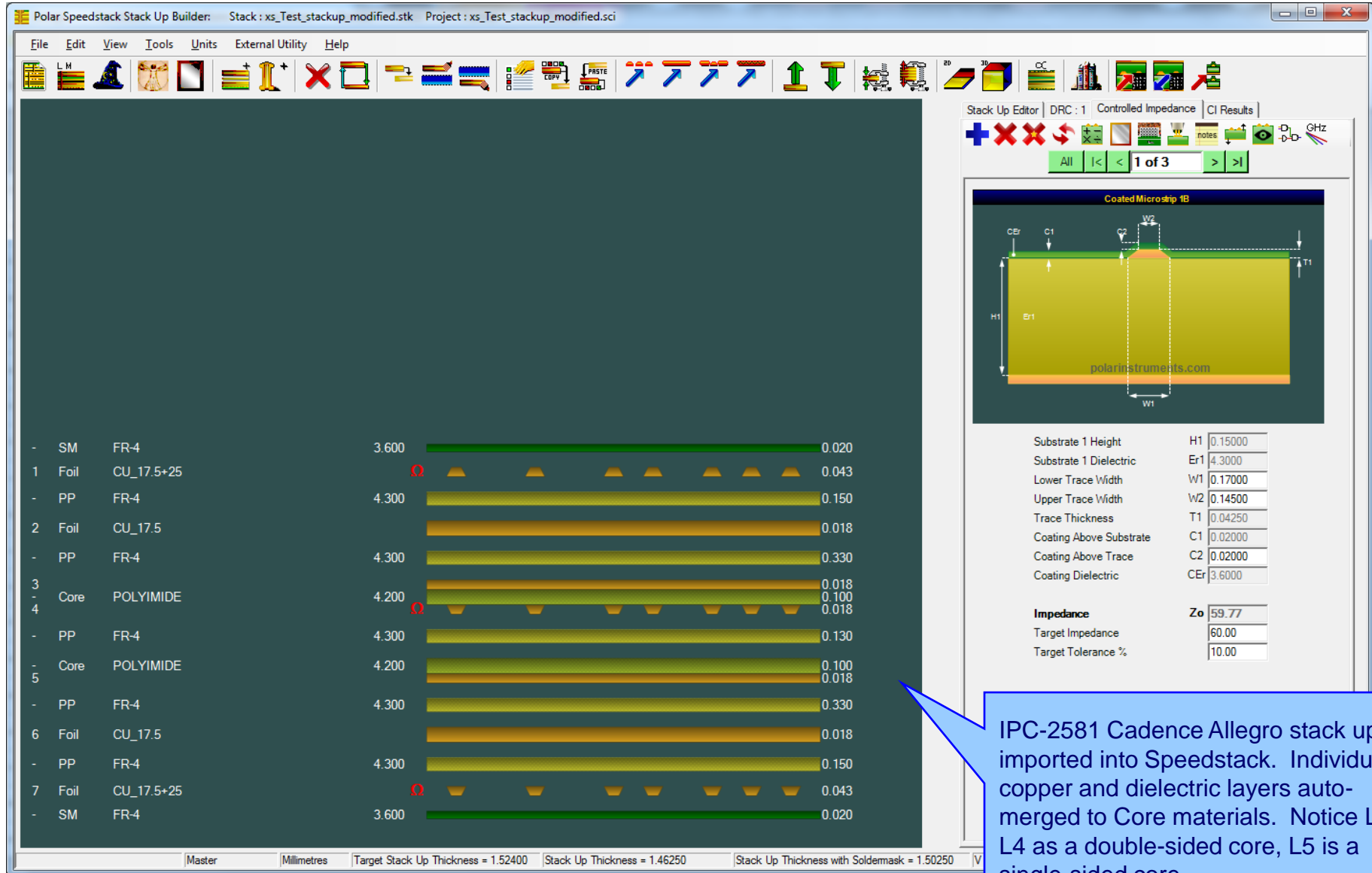
User-selectable options to control how the IPC-2581 data is allocated in Speedstack

Software Package details the application that generated the IPC-2581 file. In this case Cadence Allegro

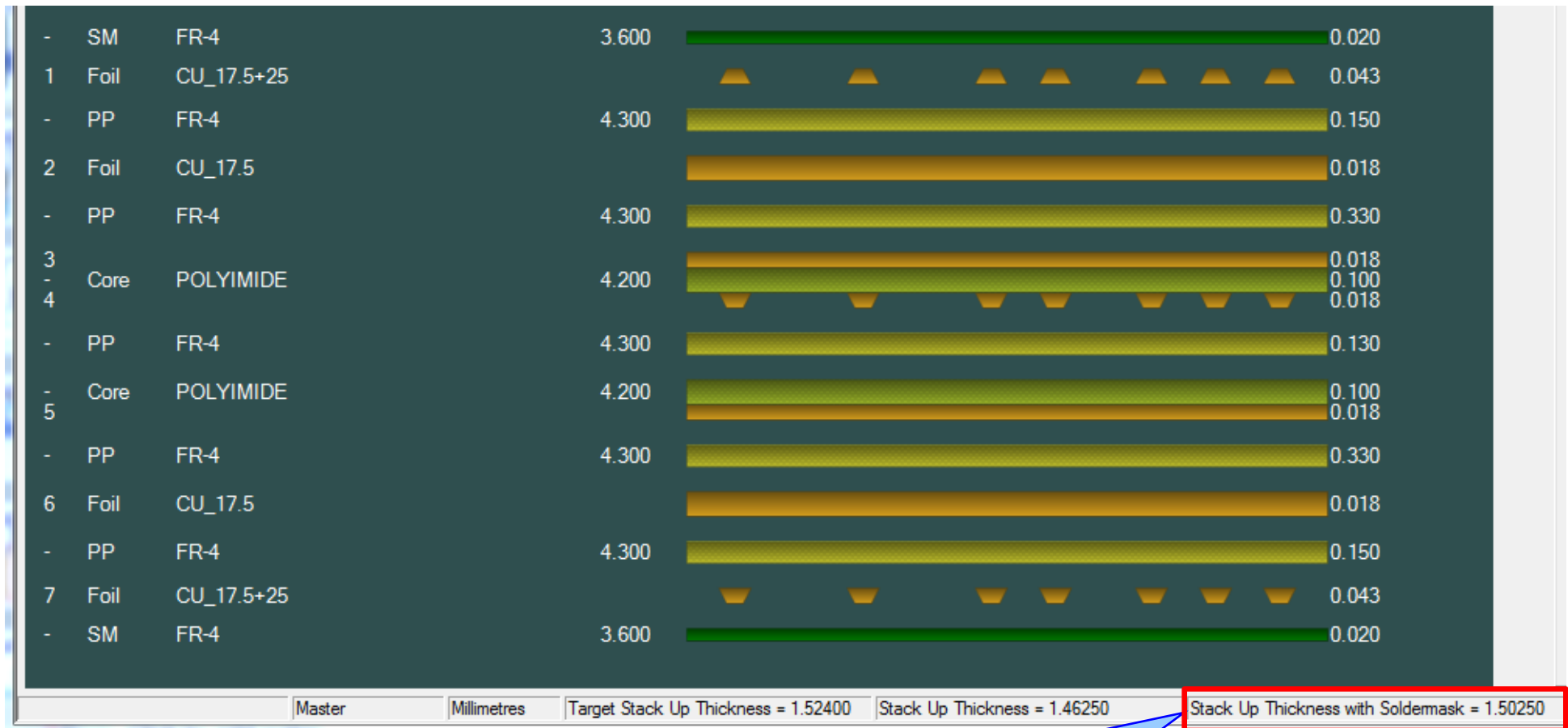
Stack up imported from IPC-2581 shown in data grid form. The Layer Function determines the layer / material type

Stack up thickness total


The Foil, Prepreg, Core and Solder Mask material data grid colours are determined by the Speedstack Configuration, so colour scheme familiar to users



IPC-2581 Cadence Allegro stack up imported into Speedstack. Individual copper and dielectric layers auto-merged to Core materials. Notice L3 / L4 as a double-sided core, L5 is a single-sided core



Some EDA tools define all Dielectric layers as Core materials within the IPC-2581 format. In reality the actual stack up is constructed from a combination of Core and Prepreg materials



Speedstack Layer Number	Layer Name	Specification Name	Layer Function	Side	Thickness	TolPlus	TolMinus	Sequence	Material Description	Resin Content
1	TOP	SPEC_LAYER_TOP	CONDUCTOR	TOP	0.001000	0.000000	0.000000	2	10Z_COPPER	
	DIELECTRIC_BELOW_TOP	SPEC_LAYER_DIELECTRIC_BELOW_...	DIELCORE	INTERNAL	0.005000	0.000000	0.000000	3	POLYIMIDE	
	DIELECTRIC_2_BELOW_T...	SPEC_LAYER_DIELECTRIC_2_BELO...	DIELCORE	INTERNAL						
2	NONAME_1	SPEC_LAYER_NONAME_1	PLANE	INTERNAL						
	DIELECTRIC_BELOW_NO...	SPEC_LAYER_DIELECTRIC_BELOW_...	DIELCORE	INTERNAL	0.039000	0.000000	0.000000	6		
3	NONAME_2	SPEC_LAYER_NONAME_2	PLANE	INTERNAL	0.001000	0.000000	0.000000	7		
	DIELECTRIC_BELOW_NO...	SPEC_LAYER_DIELECTRIC_BELOW_...	DIELCORE	INTERNAL	0.005000	0.000000	0.000000	8		
	DIELECTRIC_2_BELOW_...	SPEC_LAYER_DIELECTRIC_2_BELO...	DIELCORE	INTERNAL	0.005000	0.000000	0.000000	9		
4	BOTTOM	SPEC_LAYER_BOTTOM	CONDUCTOR	BOTTOM	0.001000	0.000000	0.000000	10		
	STACKUP THICKNESS				0.063000					

Set Layer Function to

Set Dielectric Constant / Loss Tangent values

- SIGNAL
- PLANE
- MIXED
- DIELCORE
- DIELPREG**
- DIELADHV
- SOLDERMASK

Using the right-click menu options it is possible to redefine / improve the imported IPC-2581 data prior to generating the stack up in Speedstack

Import IPC-2581 Rev B

IPC-2581 File Information

File Name

Revision

Units

Import

☒ A
 ☒ A
 ☒ C

Assign

Software Package (that generated the file)

Name

Revision

Vendor

Allegro

allegro_16.6S032(7/12/2014)

Cadence


Display Options

☒ All (Stack Up and Structure Data)
 ☐ Stack Up Data only
 ☐ Structure Data only

Import

Cancel

Notes: 0



To edit the data displayed below select the row, right-click menu and choose the appropriate function

Speedstack Layer Number	Layer Name	Specification Name	Layer Function	Side	Thickness	TolPlus	TolMinus	Sequence	Material Description	Resin Content
1	TOP	SPEC_LAYER_TOP	CONDUCTOR	TOP	0.001000	0.000000	0.000000	2	10Z_COPPER	
	DIELECTRIC_BELOW_TOP	SPEC_LAYER_DIELECTRIC_BELOW_...	DIELPREG	INTERNAL	0.005000	0.000000	0.000000	3	POLYIMIDE	
	DIELECTRIC_2_BELOW_T...	SPEC_LAYER_DIELECTRIC_2_BELO...	DIELPREG	INTERNAL	0.005000	0.000000	0.000000	4	POLYIMIDE	
2	NONAME_1	SPEC_LAYER_NONAME_1	PLANE	INTERNAL	0.001000	0.000000	0.000000	5	10Z_COPPER	
	DIELECTRIC_BELOW_NO...	SPEC_LAYER_DIELECTRIC_BELOW_...	DIELCORE	INTERNAL	0.039000	0.000000	0.000000	6	POLYIMIDE	
3	NONAME_2	SPEC_LAYER_NONAME_2	PLANE	INTERNAL	0.001000	0.000000	0.000000	7	10Z_COPPER	
	DIELECTRIC_BELOW_NO...	SPEC_LAYER_DIELECTRIC_BELOW_...	DIELPREG	INTERNAL	0.005000	0.000000	0.000000	8	POLYIMIDE	
	DIELECTRIC_2_BELOW_...	SPEC_LAYER_DIELECTRIC_2_BELO...	DIELPREG	INTERNAL	0.005000	0.000000	0.000000	9	POLYIMIDE	
4	BOTTOM	SPEC_LAYER_BOTTOM	CONDUCTOR	BOTTOM	0.001000	0.000000	0.000000	10	10Z_COPPER	
	STACKUP THICKNESS				0.063000					

Now the Layer Function has been correctly defined as Cores and Prepregs it is possible to generate the stack up

Polar Speedstack Stack Up Builder: Stack : stackup-tc-2.stk Project : stackup-tc-2.sci

File Edit View Tools Units External Utility Help

Stack Up Editor | DRC : 0 | Controlled Impedance | CI Results

Stack Up Information

Field	Value
Electrical Layer Count	4
Stack Up Cost	0.00
Copper Thickness	4.0000
Dielectric Thickness	59.0000
Solder Mask Thickness	0.0000
=====	=====
Target Stack Up Thickness	60.0000
Stack Up Thickness	63.0000
Stack Up Thickness with Soldermask	63.0000
=====	=====

Selected Item Information

The final stack up imported from IPC-2581 correctly defined as Foils, Cores and Prepregs

Layer	Type	Material	Thickness (Mils)	Thickness (Thous)
1	Foil	10Z_COPPER	1.000	1.000
-	PP	POLYIMIDE	4.300	5.000
-	PP	POLYIMIDE	4.300	5.000
2	Core	POLYIMIDE	4.300	1.000
3	Core	POLYIMIDE	4.300	39.000
-	PP	POLYIMIDE	4.300	1.000
-	PP	POLYIMIDE	4.300	5.000
-	PP	POLYIMIDE	4.300	5.000
4	Foil	10Z_COPPER	1.000	1.000

Master | Mils/Thous | Target Stack Up Thickness = 60.0000 | Stack Up Thickness = 63.0000 | Stack Up Thickness with Soldermask = 63.0000 | V : 18.08.26151

Eight new coplanar strips and waveguide structures are now supported

Structure Control

Number Of Signal Tracks

Single Trace

Differential

Offset Stripline 1B2A

Offset Coplanar Strips 1B2A

Offset Coplanar Waveguide 1B2A

Target Impedance 50.00

Target Tolerance % 10.0

Total of Structures Added 0

Primary Reference Plane 1

Secondary Reference Plane 3

Apply

Apply All

Advanced

Done

Cancel

Stack Up Editor | DRC : 1 | Controlled Impedance | CI Results

Stack Up Editor

Stack Up Thickness = 19.1000

Target Stack Up Thickness = 60.0000

Mils/Thous

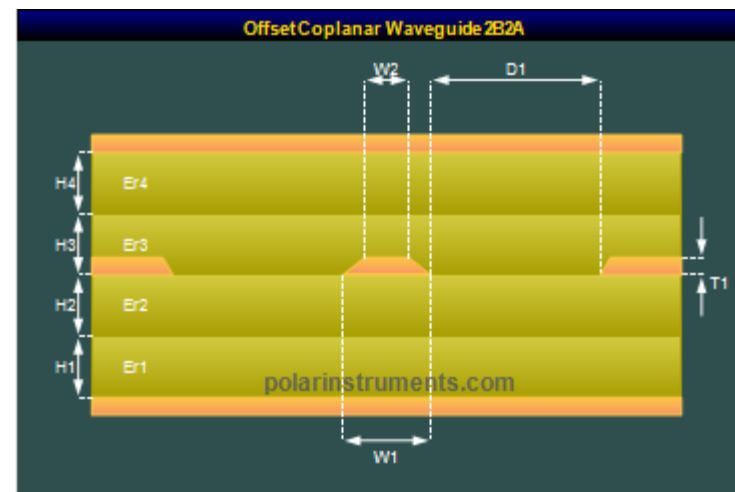
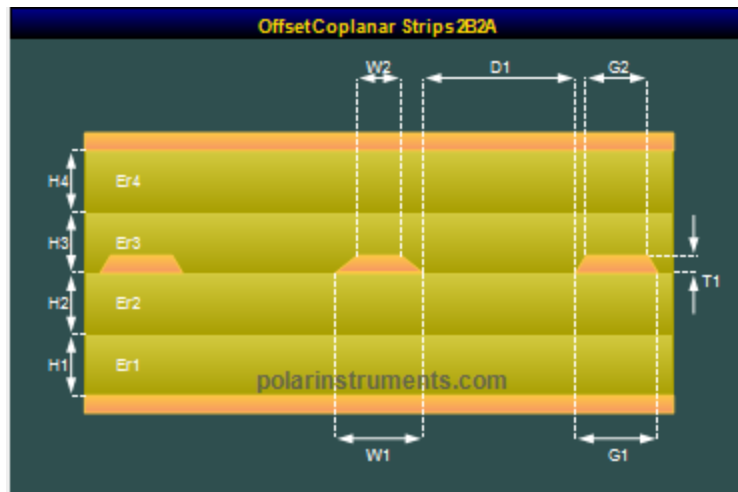
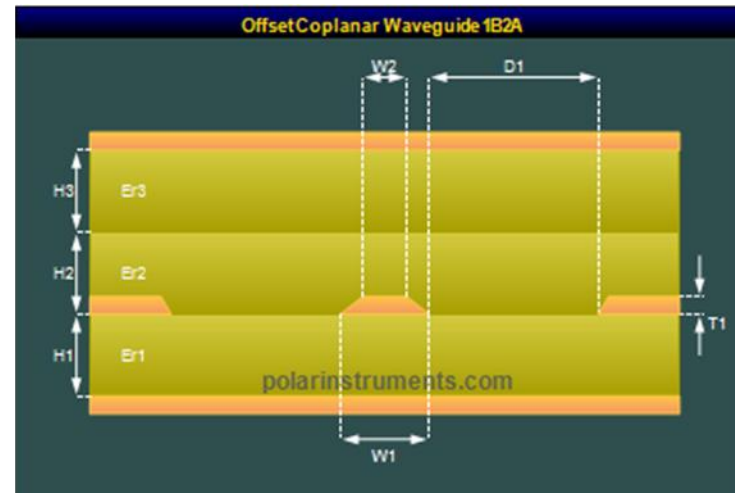
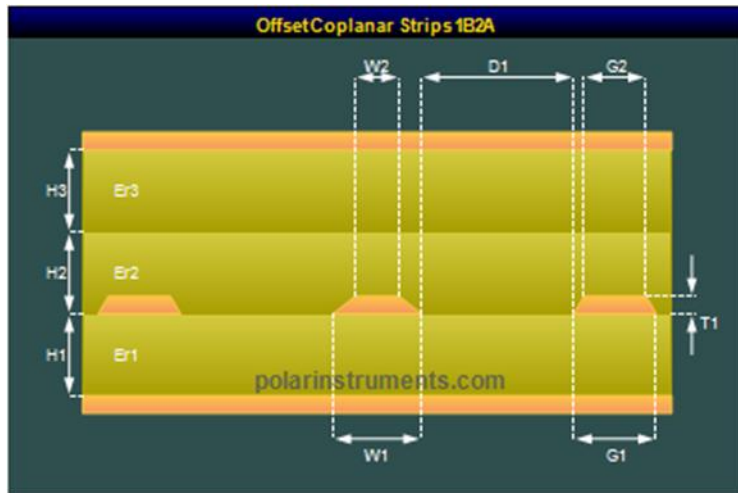
V: 18.08.26151

Layer	Material	Thickness (Mils/Thous)	Impedance (Ohms)
1	CLay	3.210	2.000
2	FC	3.200	0.700
3	Adh	3.100	4.000
4	FC	3.200	0.700
5	CLay	3.210	6.000
6	CLay	3.210	0.700
7	CLay	3.210	50.000
8	CLay	3.210	19.100

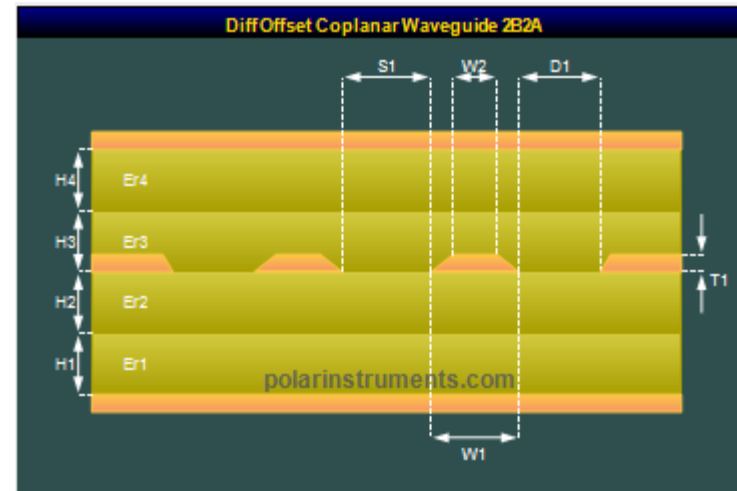
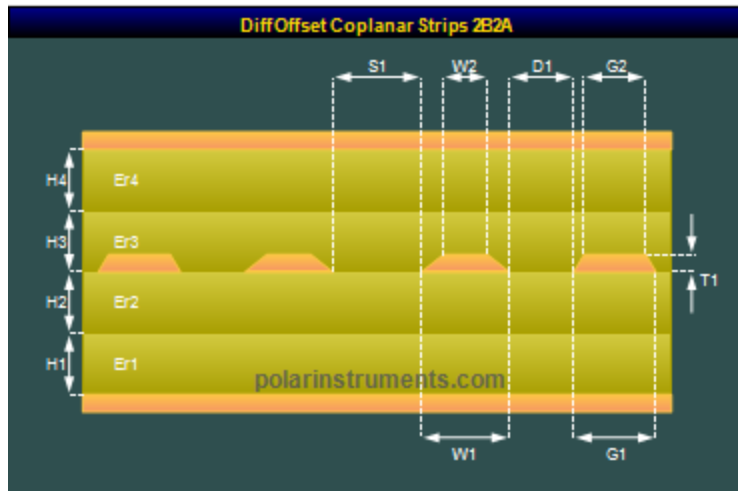
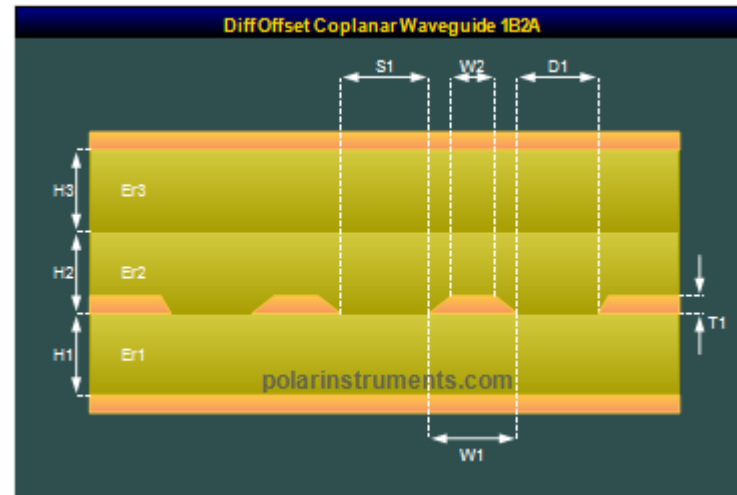
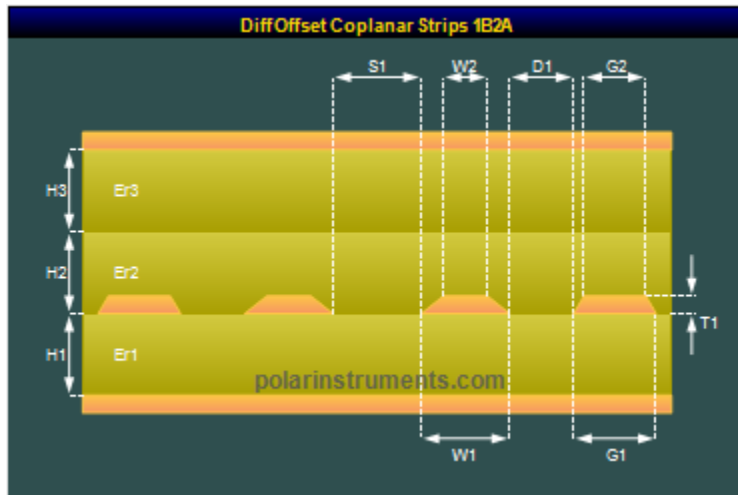
Parameter	Value
Substrate 1 Height	H1 6.0000
Substrate 1 Dielectric	Er1 3.2000
Substrate 2 Height	H2 3.7000
Substrate 2 Dielectric	Er2 3.1000
Substrate 3 Height	H3 4.0000
Substrate 3 Dielectric	Er3 3.2000
Lower Trace Width	W1 7.2227
Upper Trace Width	W2 6.2227
Lower Ground Strip Width	G1 100.0000
Upper Ground Strip Width	G2 99.0000
Ground Strip Separation	D1 10.0000
Trace Thickness	T1 0.7000

Impedance	Value
Target Impedance	50.00
Target Tolerance %	10.00

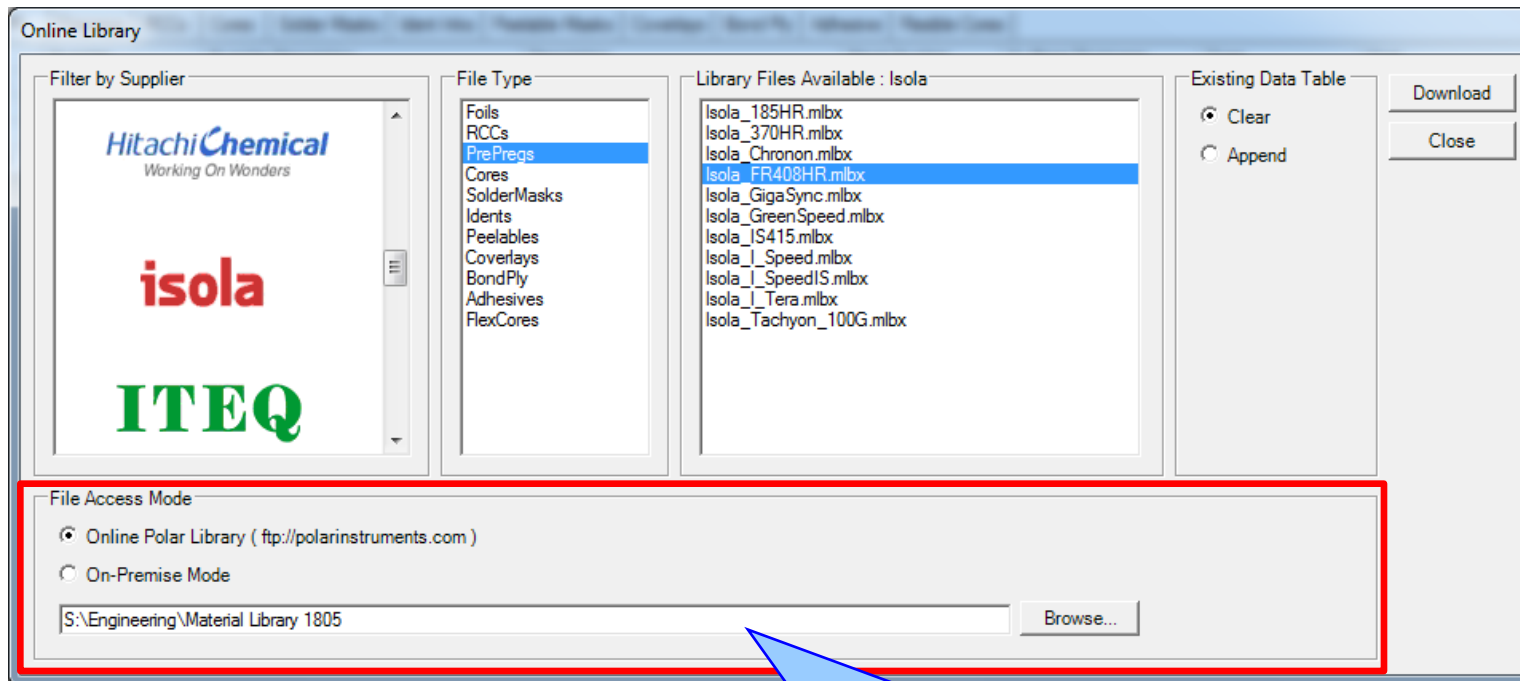
New coplanar structures supported: four new single-ended structures



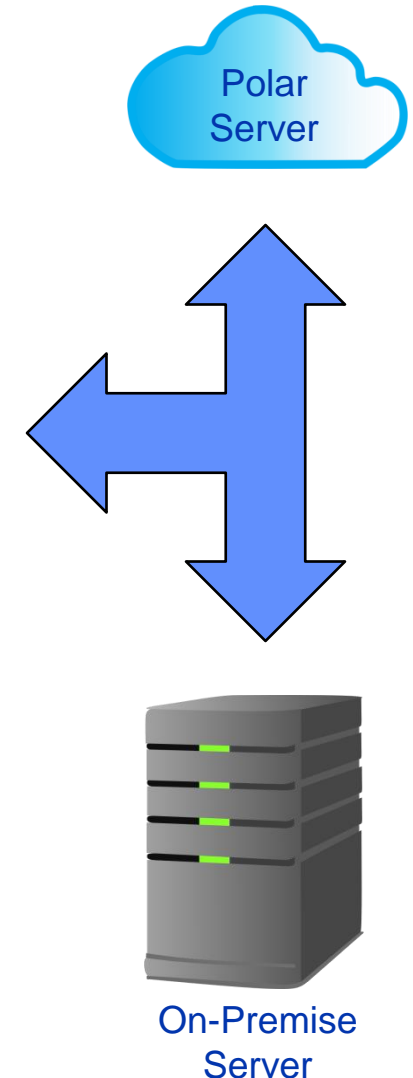
New coplanar structures supported: four new differential structures



Online Library – New On-Premise Mode

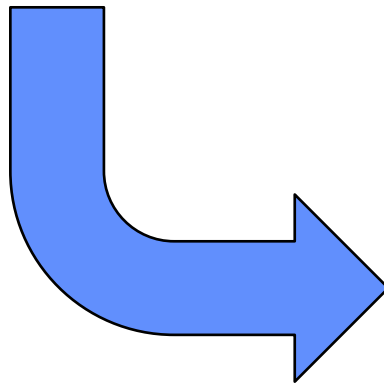
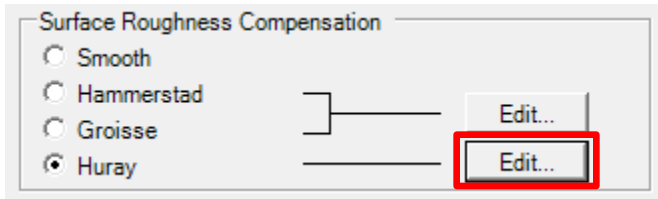


The Online Library can now access the latest material library data from either the Polar FTP Server or an On-Premise Server. The On-Premise Mode is ideal for those users where internal security policies prevent access to external FTP servers. Please contact your local Polar office for more information

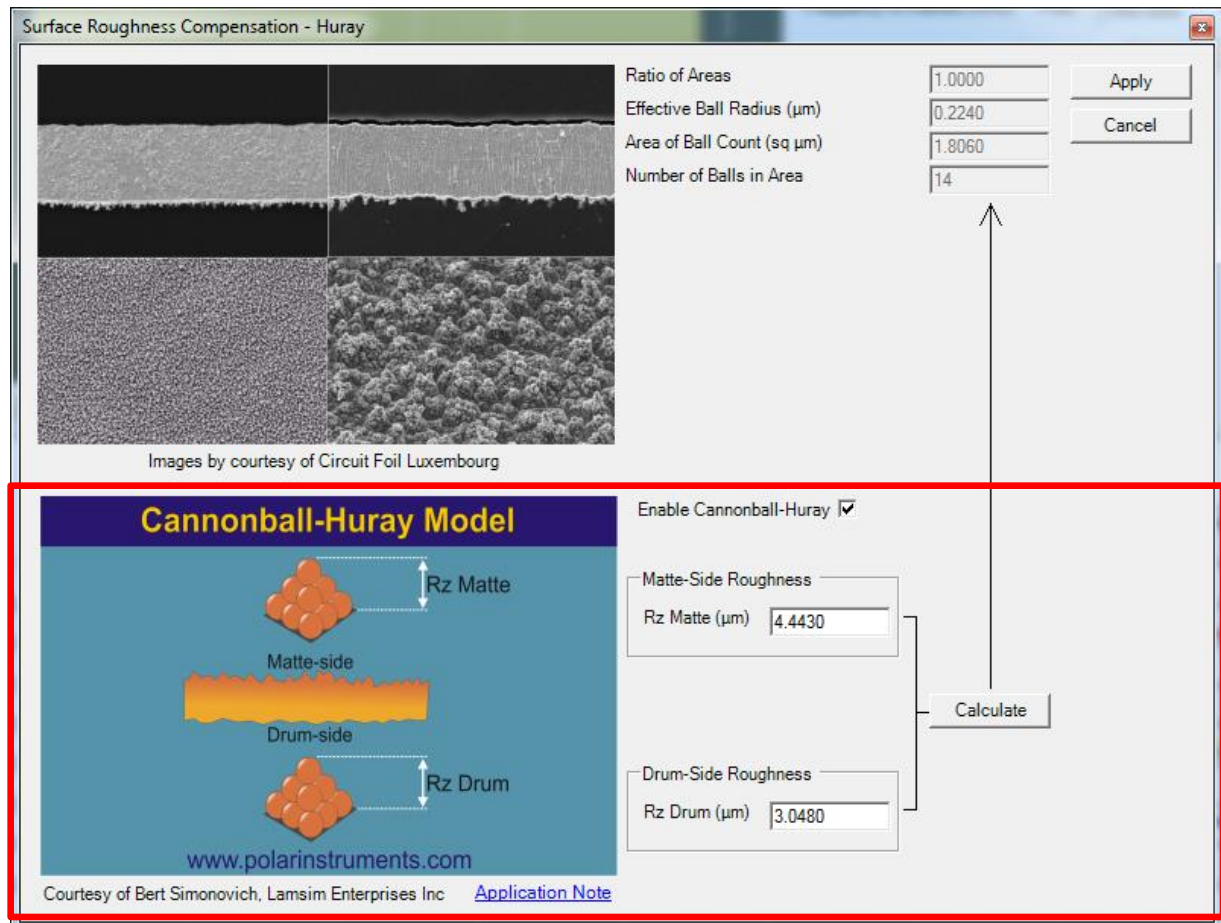


Speedstack v18.05 (May 2018)

Cannonball-Huray Surface Roughness Method



The Cannonball-Huray method has been added to Surface Roughness Compensation options. This requires the entry of Matte and Drum side Rz values



Cannonball-Huray Surface Roughness Method

Polar Si9000 PCB Transmission Line Field Solver - [C:\Program Files\Polar\Si9000\Untitled.Si9] [C:\Program Files\Polar\Si9000\Untitled.SIP]

File Edit Configuration Help

Surface Microstrip 1B
Surface Microstrip 2B
Coated Microstrip 1B
My Name 11 - [Coated Microst...]
Dual Coated Microstrip 1B
Fred - [Dual Coated Microst...]
Embedded Microstrip 1B1A
Embedded Microstrip 1B2A

Edge-Coupled Coated Microstrip 1B

Length of Line LL 101600.00
Trace Conductivity (S/m) TC 5.80E+07 Set...
Loss Tangent TanD 0.0195 GoalSeek
Rise Time (ps) Tr 10
Frequency Minimum (MHz) FMin 500.000
Frequency Maximum (GHz) FMax 10.000 Set...
Frequency Steps FSteps 20
☐ Auto Calc

Frequency Distribution
☐ Logarithmic ☒ Linear

Result Presentation
☒ Length of Line ☐ in ☐ m

Extended Substrate Data
☐ Constant Er / TanD Edit...
☒ Causally Extrapolate Er / TanD Edit...
☐ Multiple Er / TanD Edit...

Surface Roughness Compensation
Load Impedance (Ohms) 50.00

Graph Odd Mode Even Mode SPICE RLGC 4 Port S-Parameters - Graph 4 Port S-Parameters

Edge-Coupled

All Losses with Roughness - dB/line

Conductor Loss Dielectric Loss Attenuation

Lossless Calculation Frequency Dependence

Surface Roughness Compensation - Huray

Ratio of Areas 1.0000 Apply
Effective Ball Radius (μm) 0.2240 Cancel
Area of Ball Count (sq μm) 1.8060
Number of Balls in Area 14 Smoother Rougher

Images by courtesy of Circuit Foil Luxembourg

Cannonball-Huray Model

Enable Cannonball-Huray ☒

Matte-Side Roughness
Rz Matte (μm) 4.4430

Drum-Side Roughness
Rz Drum (μm) 3.0480

Calculate

www.polarinstruments.com

Courtesy of Bert Simonovich, Lamsim Enterprises Inc [Application Note](#)

The Cannonball-Huray method has also been introduced to the Si9000e. The bi-directional copy / paste interface between Speedstack and Si9000e allows for the quick transfer of structure parameters between products – the new Cannonball-Huray parameters are now supported

Online Material Library Enhancements

C:\Program Files\Polar\Speedstack\Samples\Speedstack Imperial.mlbx

EXIT [Icons]

Foils | Prepregs | RCCs | Cores | Solder Masks | Ident Inks | Peelable Masks | Coverlays | Bond Ply | Adhesive | Flexible Cores

Supplier	Supplier Description	Description	Stock Number	Dielectric Base Thickness	Dielectric Finished Thickne	Dielectric Constant	Resin Content	T _g
ITEQ	IT-958G-1037-2ml	PrePreg 1037	IT-958G-1037-01	2	2	2.99	73	17
ITEQ	IT-958G-1037-2.2ml	PrePreg 1037	IT-958G-1037-02	2.2	2.2			
ITEQ	IT-958G-106-2ml	PrePreg 106	IT-958G-106-01	2	2			
ITEQ	IT-958G-106-2.3ml	PrePreg 106	IT-958G-106-02	2.3	2.3			
ITEQ	IT-958G-1067-2.5ml	PrePreg 1067	IT-958G-1067-01	2.5	2.5			
ITEQ	IT-958G-1067-2.9ml	PrePreg 1067	IT-958G-1067-02	2.9	2.9			
ITEQ	IT-958G-1078-2.8ml	PrePreg 1078	IT-958G-1078-01	2.8	2.8			
ITEQ	IT-958G-1078-3.1ml	PrePreg 1078	IT-958G-1078-02	3.1	3.1			
ITEQ	IT-958G-1078-3.4ml	PrePreg 1078	IT-958G-1078-03	3.4	3.4	3.1	68	17
ITEQ	IT-958G-1078-3.7ml	PrePreg 1078	IT-958G-1078-04	3.7	3.7		70	17
ITEQ	IT-958G-1080-2.8ml	PrePreg 1080	IT-958G-1080-01	2.8	2.8		62	17

New ITEQ core and prepreg materials have been added to the Online Library

Online Library

Filter by Supplier

isola

ITEQ

LG Chem

File Type

Foils

RCCs

PrePregs

Cores

SolderMasks

Idents

Peelables

Coverlays

BondPly

Adhesives

FlexCores

Library Files Available : ITEQ

ITEQ_IT_140.mlbx

ITEQ_IT_140G.mlbx

ITEQ_IT_140TC.mlbx

ITEQ_IT_150.mlbx

ITEQ_IT_150G.mlbx

ITEQ_IT_170GRA1.mlbx

ITEQ_IT_180.mlbx

ITEQ_IT_958G.mlbx

ITEQ_IT_968.mlbx

Existing Data Table

☒ Clear

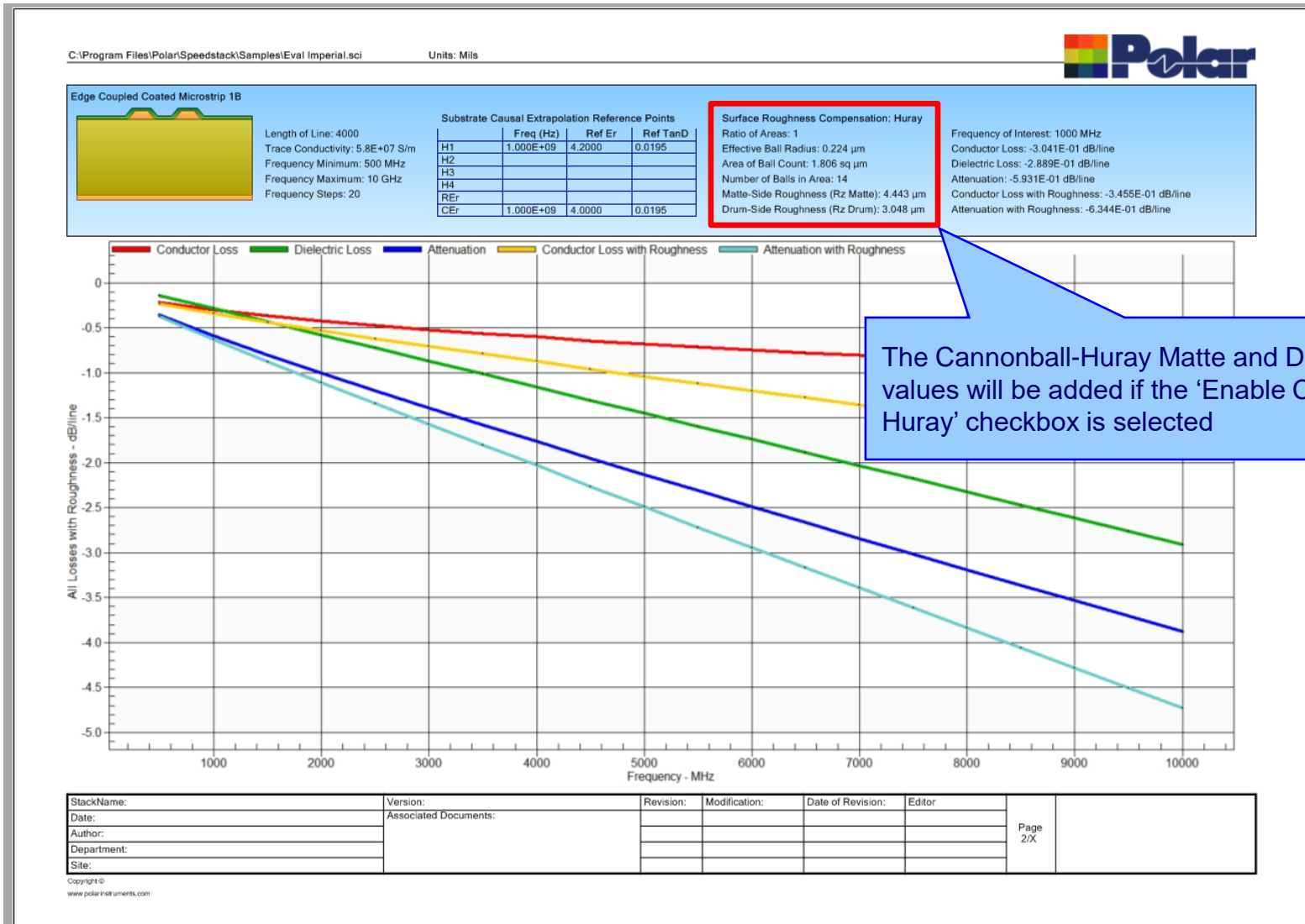
☐ Append

Download

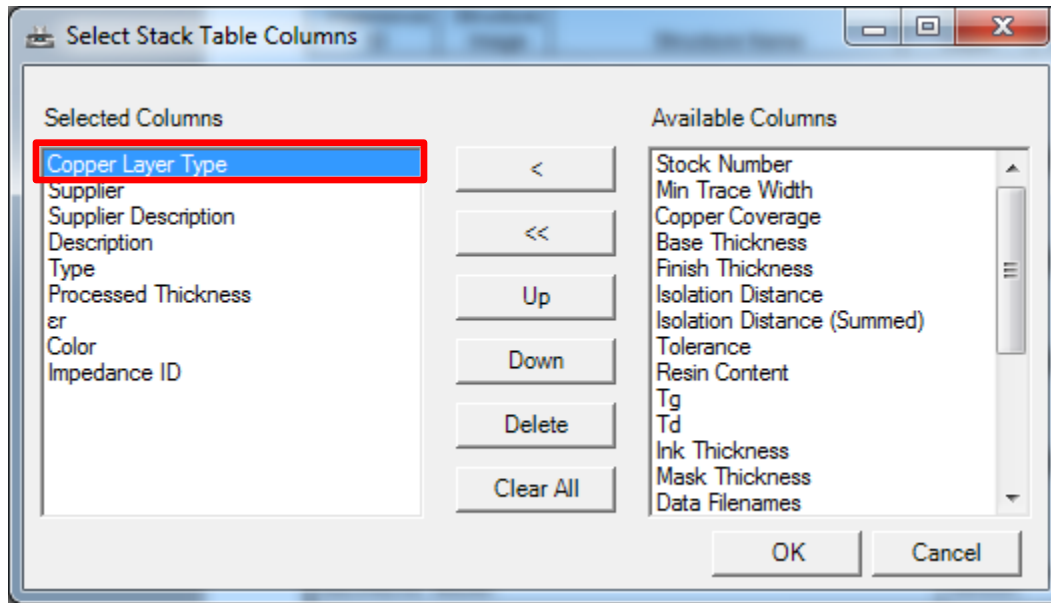
Close

Click on a material row to edit it

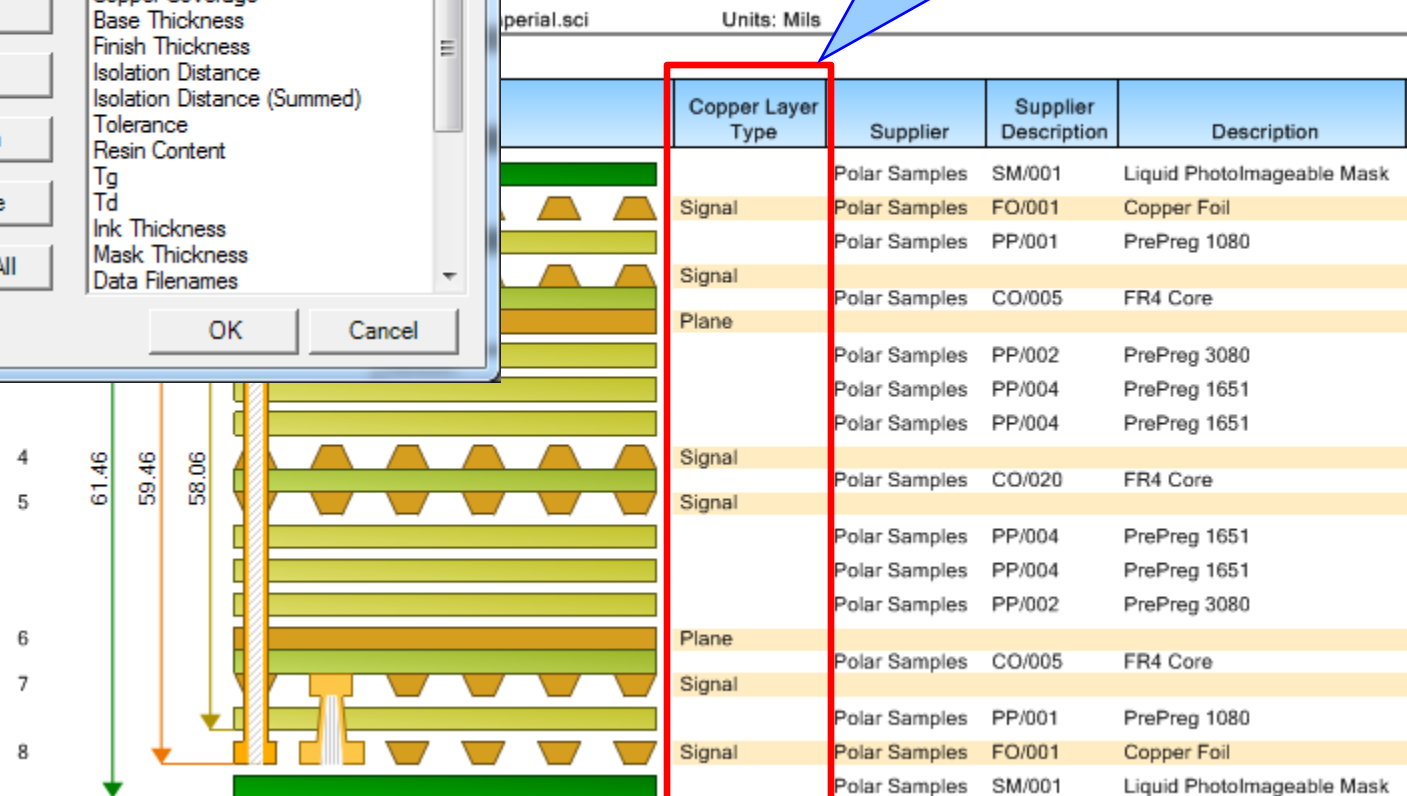
Speedstack – Technical Report enhancements



Speedstack – Technical Report enhancements

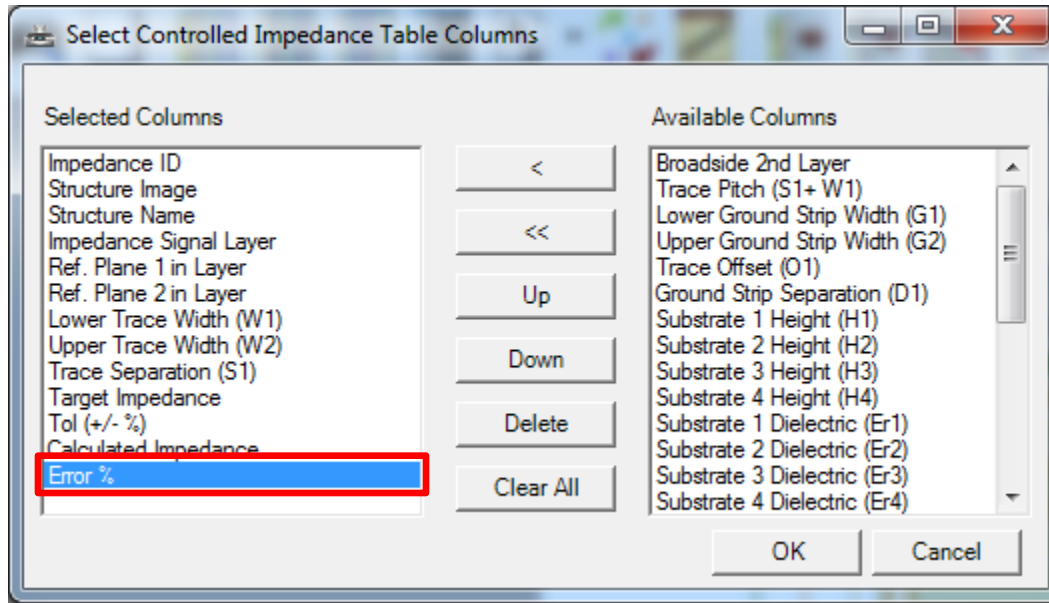


In addition to the graphical stack up image, copper layer types can be determined by a new selectable column







Copper Thickness = 9.800 | Dielectric Thickness = 49.660 | Solder Mask Thick

Speedstack – Technical Report enhancements

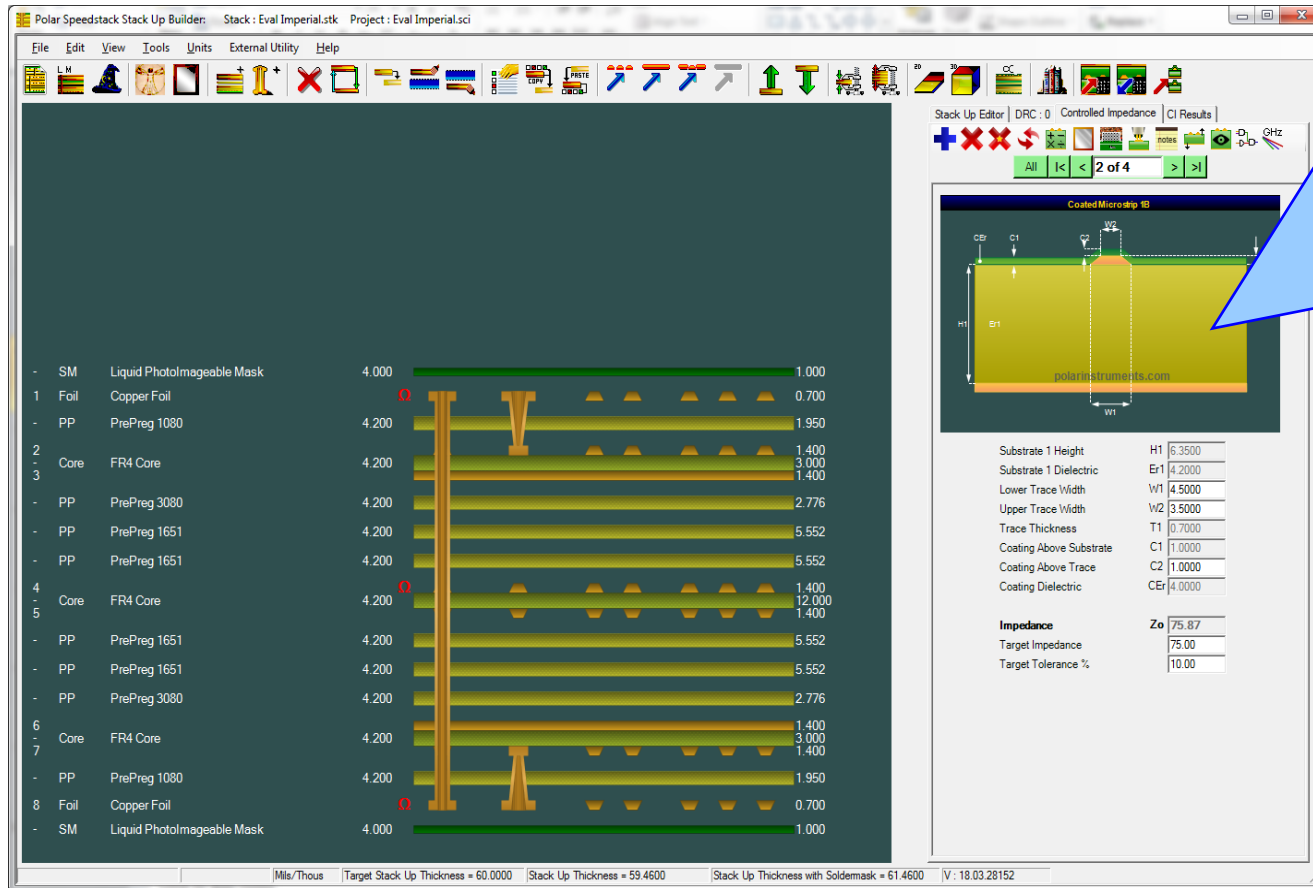


New selectable impedance table 'Error %' field. Print the Error % between the Target and Calculated Impedance

Substrate 4 Dielectric (D4)													
<div>OKCancel</div>													
ID	Image	Structure Name	Layer	In Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Target Impedance	Tol (+/- %)	Calculated Impedance	Error %	
1		Edge Coupled Coated Microstrip 1B	1	3	0	8.500	7.500	8.115	100.000	10.000	100.350	0.3	
2		Coated Microstrip 1B	1	3	0	4.500	3.500	0.000	75.000	10.000	75.870	1.2	
3		Edge Coupled Offset Stripline 1B1A	4	3	6	7.250	6.250	8.500	100.000	10.000	101.280	1.3	
4		Coated Microstrip 1B	8	6	0	4.500	3.500	0.000	75.000	10.000	75.870	1.2	

Speedstack v18.03 (March 2018)

Speedstack – Frequency Dependent Loss Calculations



In order to calculate frequency dependent loss it is necessary to know the following critical information regarding the transmission line structure:

- Material properties including dielectric constant and loss tangent
- Conductor properties such as trace conductivity and surface roughness
- Frequency range that the transmission line structure will operate

Once this information has been gathered it is possible to run a detailed analysis of the transmission line structure for both controlled impedance and insertion loss

Speedstack – Frequency Dependent Loss Calculations

Stack Up Editor | DRC : 0 | Controlled Impedance | CI Results

+

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notes

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👁

🔌

GHz

All | | < 2 of 4 > | > |

Substrate 1 Height	H1	6.3500
Substrate 1 Dielectric	Er1	4.2000
Lower Trace Width	W1	4.5000
Upper Trace Width	W2	3.5000
Trace Thickness	T1	0.7000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Dielectric	CEr	4.0000

Impedance

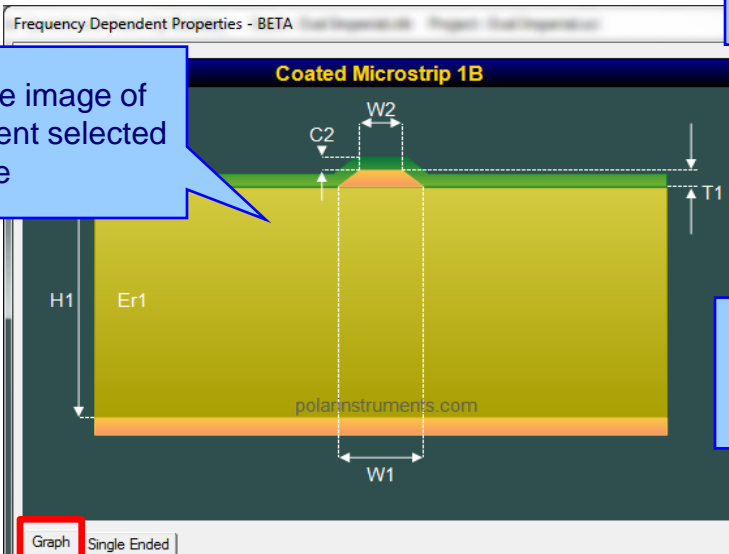
Target Impedance	Zo	75.87
Target Tolerance %		75.00
		10.00

Each structure that has been added to the stack up now has a set of Frequency Dependent Properties that are accessible using this new icon.

Selecting this icon will load the following dialog.

Result presentation, show plot and table of results in preferred units.

Structure image of the current selected structure



User-specifiable frequency range.

Length of Line LL 1000.0000
Trace Conductivity (S/m) TC 5.800E+07
Frequency Minimum (MHz) FMin 500.0000
Frequency Maximum (GHz) FMax 10.0000
Frequency Steps FStep 20
Frequency of Interest (MHz) F 1000.0000

Result Presentation

Length of Line ☐ / in ☒ / m

Substrate Causal Extrapolation Reference Points

☒ Set Er values from Stack Up materials

	Freq (Hz)	Ref Er	Ref TanD
H1	1.000E+09	4.2000	0.0195
H2			
H3			
H4			
REr			
CEr	1.000E+09	4.0000	0.0195

Surface Roughness Compensation

☐ Smooth ☒ Hammerstad ☐ Grosse ☐ Huray

Print Settings

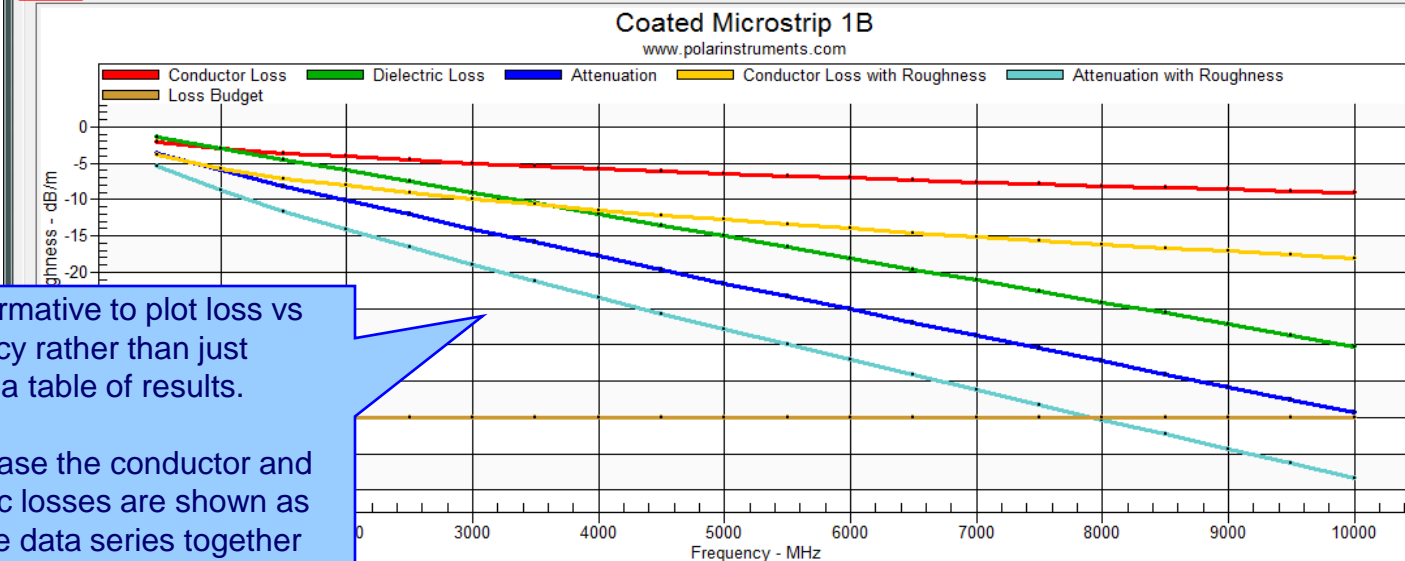
☒ Include Loss Graph for this structure

Dielectric constant and loss tangent properties for each substrate dielectric / region

Surface roughness compensation model. Hammerstad, Grosse and Huray methods supported

It is informative to plot loss vs frequency rather than just present a table of results.

In this case the conductor and dielectric losses are shown as separate data series together with total attenuation



Graph Settings

Display Series: All Losses

Loss Budget (dB): -40.0000

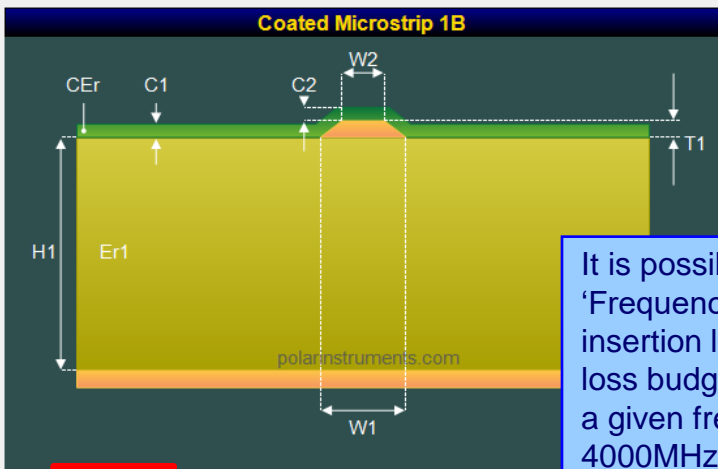
Picked Data Point Information

Frequency (MHz): 10000.000
Attenuation with Roughness (dB): -48.315

Buttons: Maximise, Print, Export

The plot is interactive. It is possible to select data points and drill down to the underlying loss data

Frequency Dependent Properties - BETA



Coated Microstrip 1B

Length of Line LL: 1000.0000
 Trace Conductivity (S/m) TC: 5.800E+07
 Frequency Minimum (MHz) FMin: 500.0000
 Frequency Maximum (GHz) FMax: 10.0000
 Frequency Steps FStep: 20
 Frequency of Interest (MHz) Freq: 4000.0000

Calculate

Result Presentation
☐ Length of Line ☐ / in ☒ / m

Substrate Causal Extrapolation Reference Points
☒ Set Er values from Stack Up materials

	Freq (Hz)	Ref Er	Ref TanD
H1	1.000E+09	4.2000	0.0195
H2			
H3			
H4			
REr			
CEr	1.000E+09		

Surface Roughness Comp
☐ Smooth
☒ Hammerstad
☐ Groisse
☐ Huray

Print Settings
☒ Include Loss Graph for this structure report

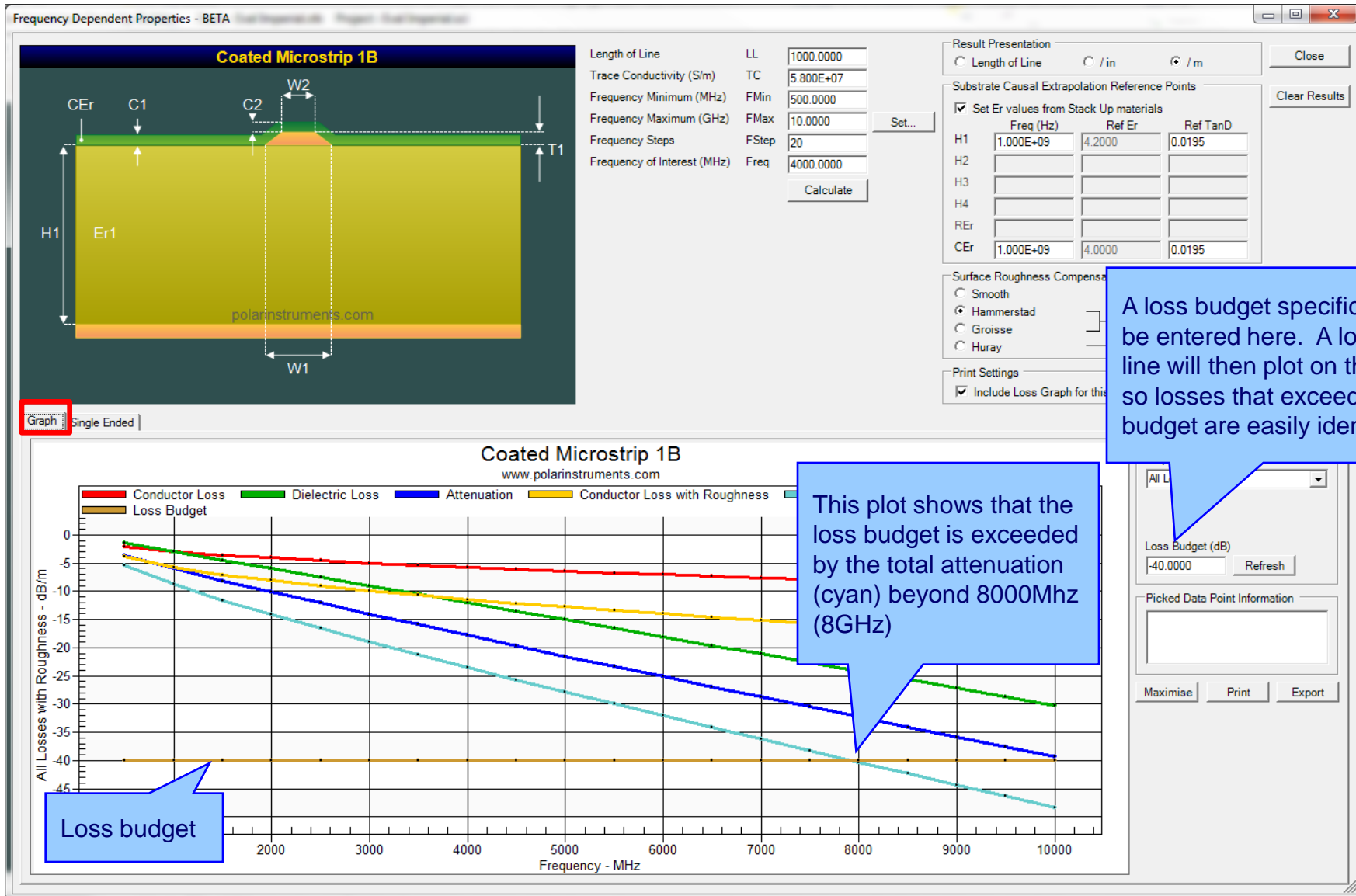
Graph: Single Ended

	Frequency Hz	Impedance Real Ohms	Impedance Imaginary Ohms	Impedance Magnitude Ohms	Inductance H/m	Resistance Ohms/m	Capacitance F/m	Conductance S/m	Skin Depth m	Conductor Loss dB/m	Dielectric Loss dB/m	Attenuation dB/m	Conductor Loss With Roughness dB/m	Attenuation With Roughness dB/m	Mo Phi Vel m/s
▶	5.000E+08	7.656E+01	-2.857E-01	7.656E+01	4.717E-07	3.750E+01	8.050E-11	4.510E-03	2.955E-06	-2.127E+00	-1.499E+00	-3.627E+00	-3.933E+00	-5.432E+00	1.6
	1.000E+09	7.656E+01	-2.997E-03	7.656E+01	4.683E-07	5.312E+01	7.988E-11	9.023E-03	2.090E-06	-3.013E+00	-3.000E+00	-6.013E+00	-5.795E+00	-8.796E+00	1.6
	1.500E+09	7.661E+01	1.237E-01	7.661E+01	4.667E-07	6.525E+01	7.952E-11	1.354E-02	1.706E-06	-3.699E+00	-4.504E+00	-8.202E+00	-7.208E+00	-1.171E+01	1.6
	2.000E+09	7.664E+01	2.192E-01	7.664E+01	4.656E-07	7.255E+01	7.926E-11	1.805E-02	1.478E-06	-4.111E+00	-6.008E+00	-1.012E+01	-8.064E+00	-1.407E+01	1.6
	2.500E+09	7.668E+01	2.714E-01	7.668E+01	4.650E-07	8.101E+01	7.906E-11	2.257E-02	1.322E-06	-4.587E+00	-7.515E+00	-1.210E+01	-9.034E+00	-1.655E+01	1.6
	3.000E+09	7.672E+01	3.101E-01	7.672E+01	4.645E-07	8.865E+01	7.890E-11	2.708E-02	1.207E-06	-5.018E+00	-9.024E+00	-1.404E+01	-9.906E+00	-1.893E+01	1.6
	3.500E+09	7.676E+01	3.403E-01	7.676E+01	4.642E-07	9.568E+01	7.876E-11	3.160E-02	1.117E-06	-5.413E+00	-1.053E+01	-1.595E+01	-1.071E+01	-2.124E+01	1.6
	4.000E+09	7.680E+01	3.648E-01	7.680E+01	4.639E-07	1.022E+02	7.864E-11	3.611E-02	1.045E-06	-5.780E+00	-1.204E+01	-1.782E+01	-1.145E+01	-2.349E+01	1.6
	4.500E+09	7.683E+01	3.852E-01	7.683E+01	4.636E-07	1.084E+02	7.854E-11	4.063E-02	9.851E-07	-6.125E+00	-1.356E+01	-1.968E+01	-1.215E+01	-2.570E+01	1.6
	5.000E+09	7.686E+01	4.025E-01	7.686E+01	4.634E-07	1.142E+02	7.845E-11	4.515E-02	9.346E-07	-6.451E+00	-1.507E+01	-2.152E+01	-1.280E+01	-2.787E+01	1.6
	5.500E+09	7.688E+01	4.175E-01	7.689E+01	4.633E-07	1.197E+02	7.836E-11	4.966E-02	8.911E-07	-6.761E+00	-1.658E+01	-2.334E+01	-1.343E+01	-3.001E+01	1.6
	6.000E+09	7.691E+01	4.306E-01	7.691E+01	4.631E-07	1.250E+02	7.827E-11	5.418E-02	8.532E-07	-7.057E+00	-1.810E+01	-2.515E+01	-1.402E+01	-3.212E+01	1.6
	6.500E+09	7.693E+01	4.422E-01	7.693E+01	4.630E-07	1.30	7.818E-11	5.871E-02	8.113E-07	-7.348E+00	-1.961E+01	-2.695E+01	-1.459E+01	-3.421E+01	1.6
	7.000E+09	7.695E+01	4.536E-01	7.695E+01	4.629E-07	1.34	7.809E-11	6.319E-02	7.708E-07	-7.643E+00	-2.112E+01	-2.874E+01	-1.514E+01	-3.637E+01	1.6

It is possible to specify a 'Frequency of Interest' as some insertion loss requirements / loss budget specifications are for a given frequency. In this case 4000MHz (4GHz)

Frequency dependent results shown as a data table

The 'Frequency of Interest' result is highlighted in the data table



Speedstack – Material and Surface Roughness properties

Substrate Causal Extrapolation Reference Points

☒ Set Er values from Stack Up materials

	Freq (Hz)	Ref Er	Ref TanD
H1	1.000E+09	4.2000	0.0195
H2			
H3			
H4			
REr			
CEr	1.000E+09	4.0000	0.0195

In order to accurately calculate Dielectric Loss it is important to understand the material / substrate properties.

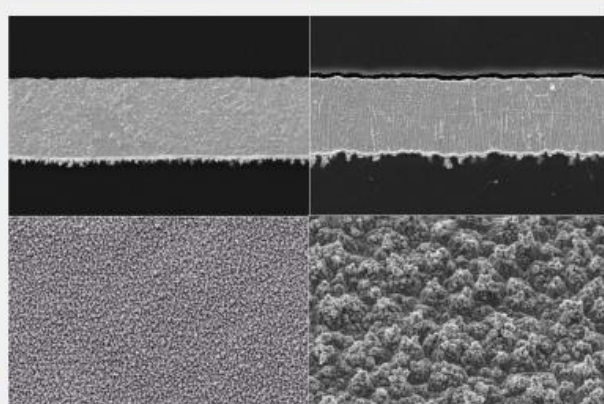
These substrate properties including dielectric constant (ϵ_r) and loss tangent ($\tan \delta$) are specified here for each structure substrate region.

Speedstack causally extrapolates ϵ_r and $\tan \delta$ over the specified frequency range using the Svensson-Djordjevic method, hence the ability to specify the extrapolation reference points for each substrate region. The reference point data is usually available from the material supplier data sheet.

Surface Roughness Compensation

☐ Smooth
☐ Hammerstad
☐ Grosse
☒ Huray

Surface Roughness Compensation - Huray - BETA



Ratio of Areas:
 Effective Ball Radius (μm):
 Area of Ball Count ($\text{sq } \mu\text{m}$):
 Number of Balls in Area:

Images by courtesy of Circuit Foil Luxembourg

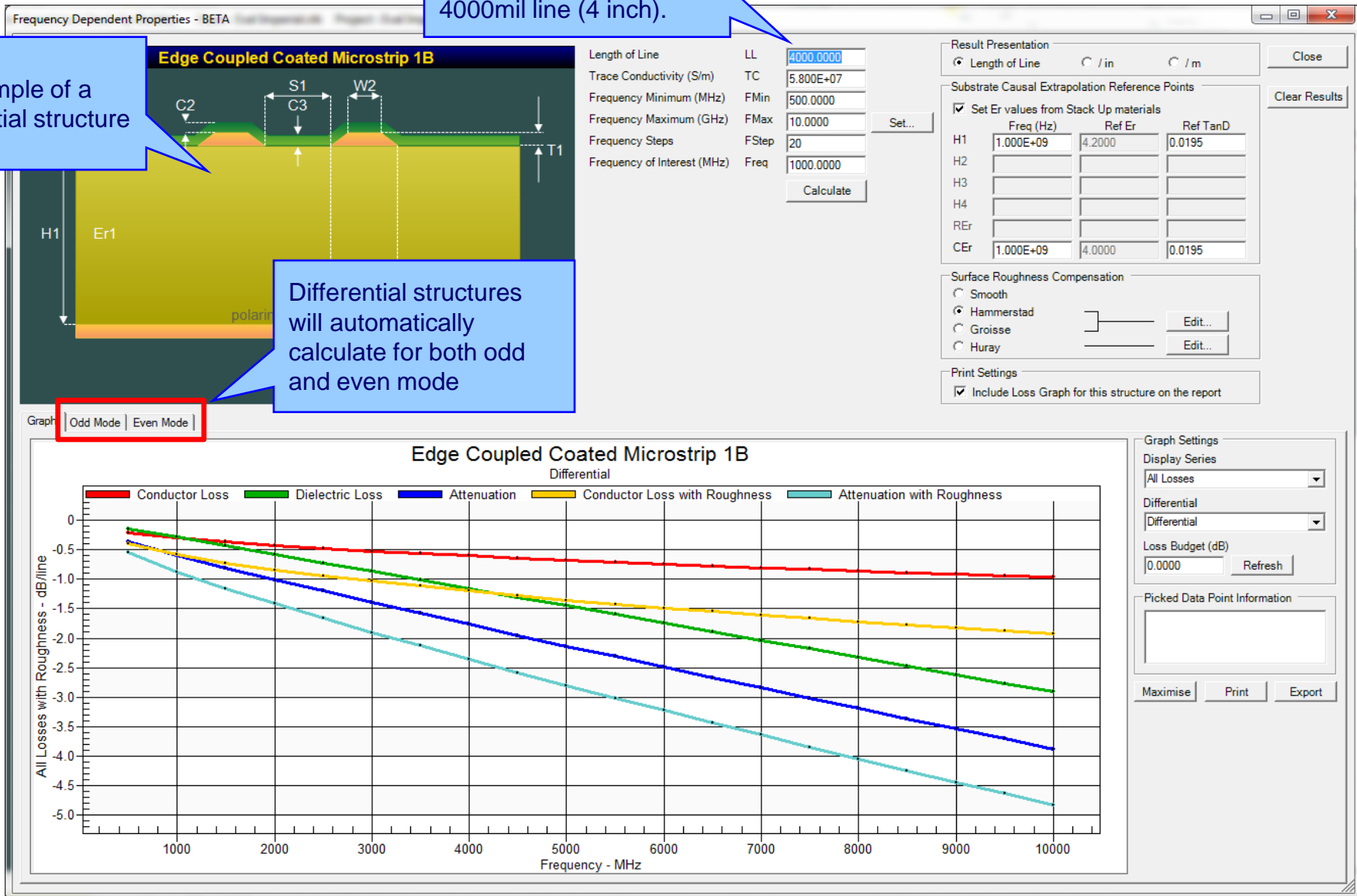
In order to accurately calculate Conductor Loss it is necessary to specify the surface roughness parameters.

Speedstack supports three different roughness models: Hammerstad, Grosse and Huray. In this example the Huray method is used, the dialog prompts for the required roughness parameters.

Result presentation, losses shown for a 4000mil line (4 inch).

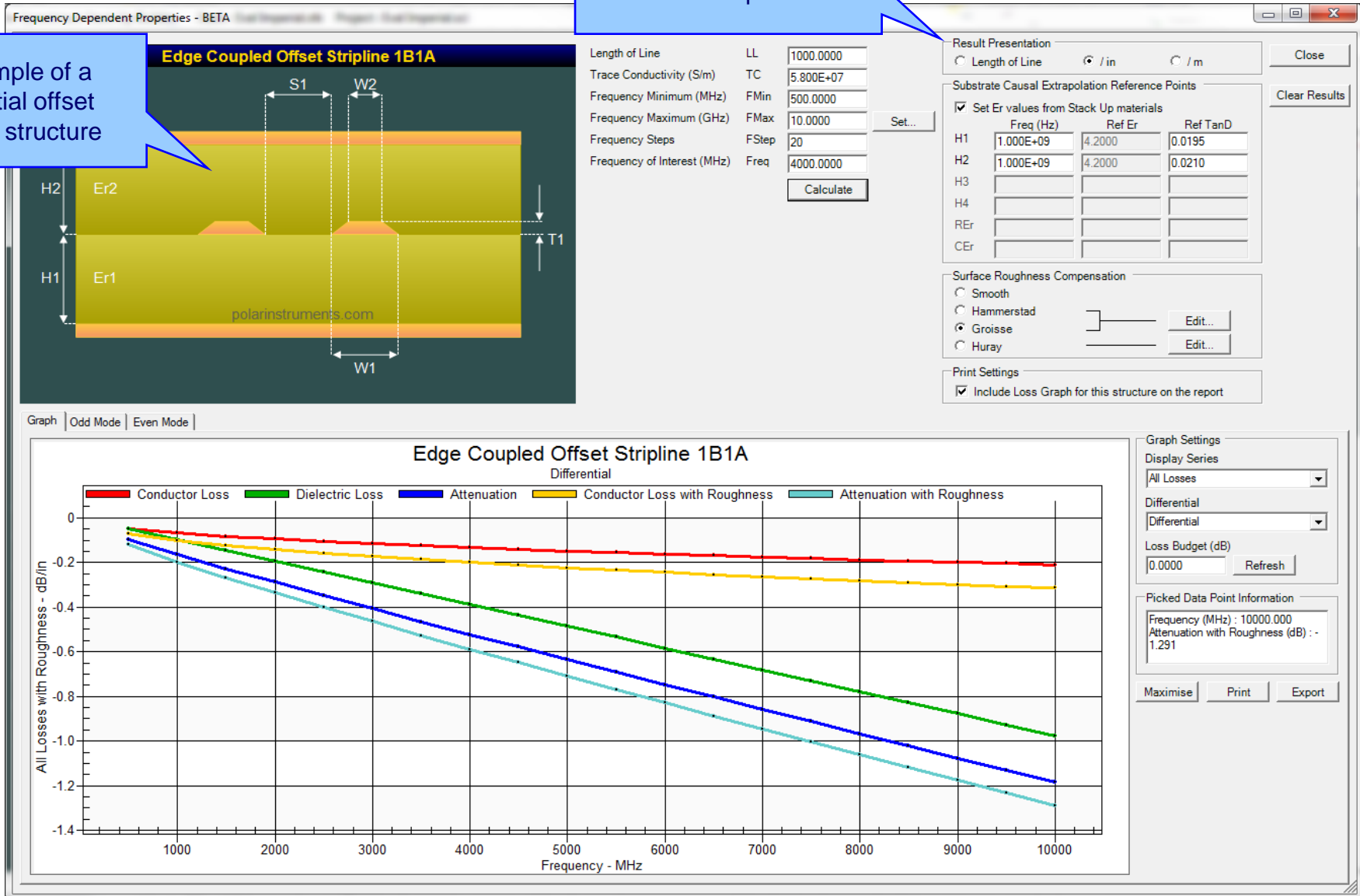
An example of a differential structure

Differential structures will automatically calculate for both odd and even mode

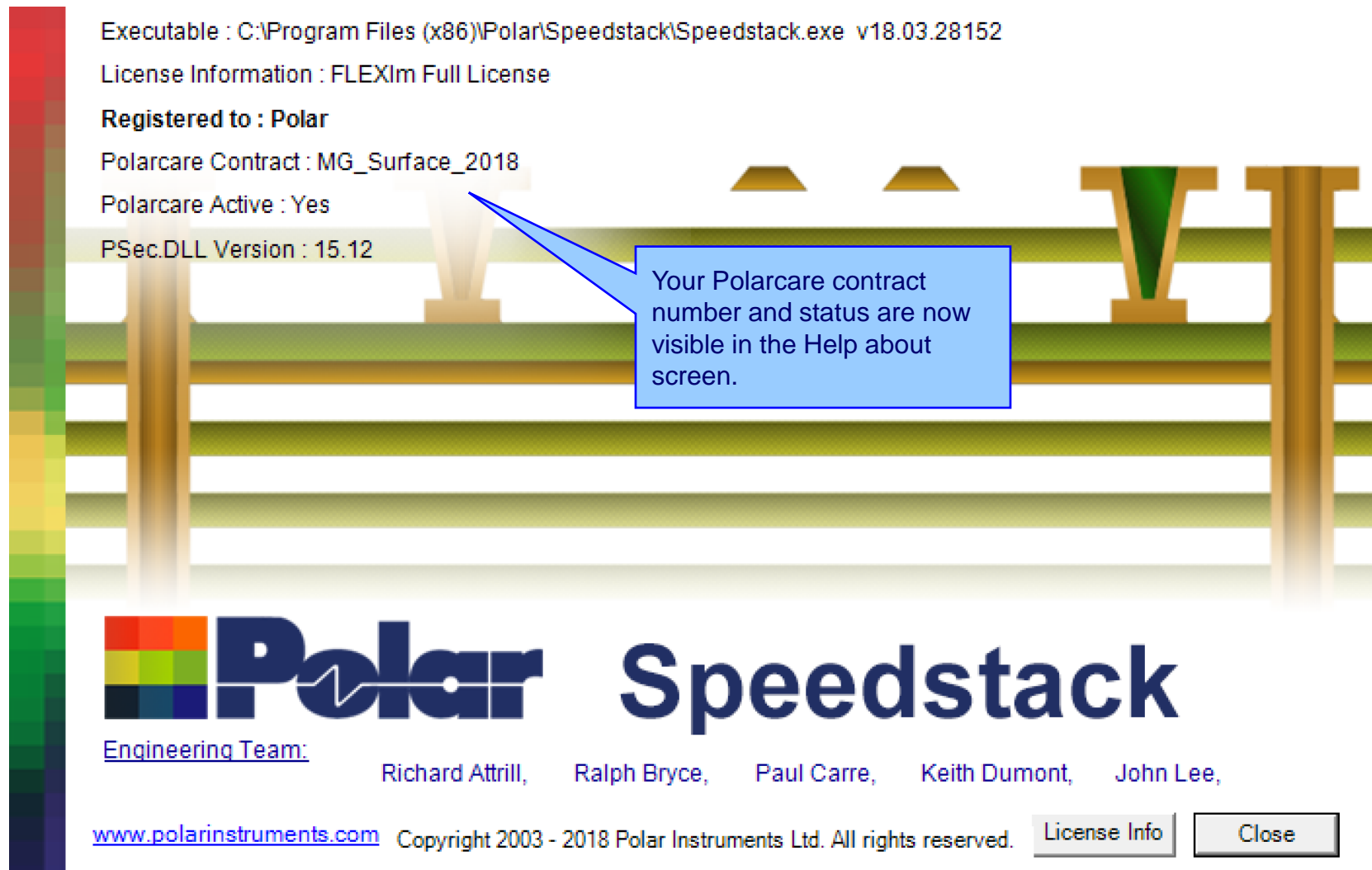


Result presentation,
losses shown per inch

An example of a
differential offset
stripline structure

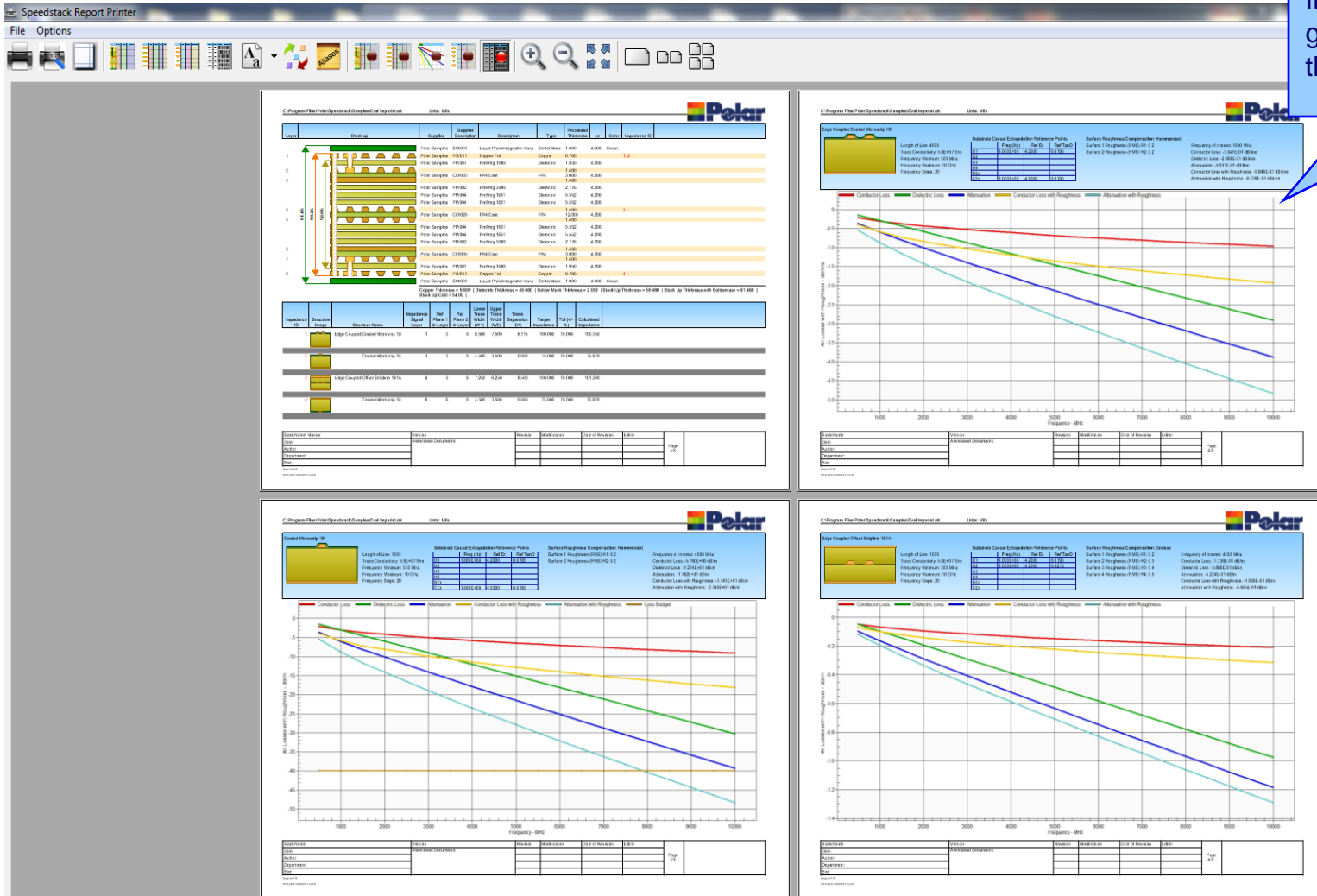


Speedstack – Contacting Polar for support

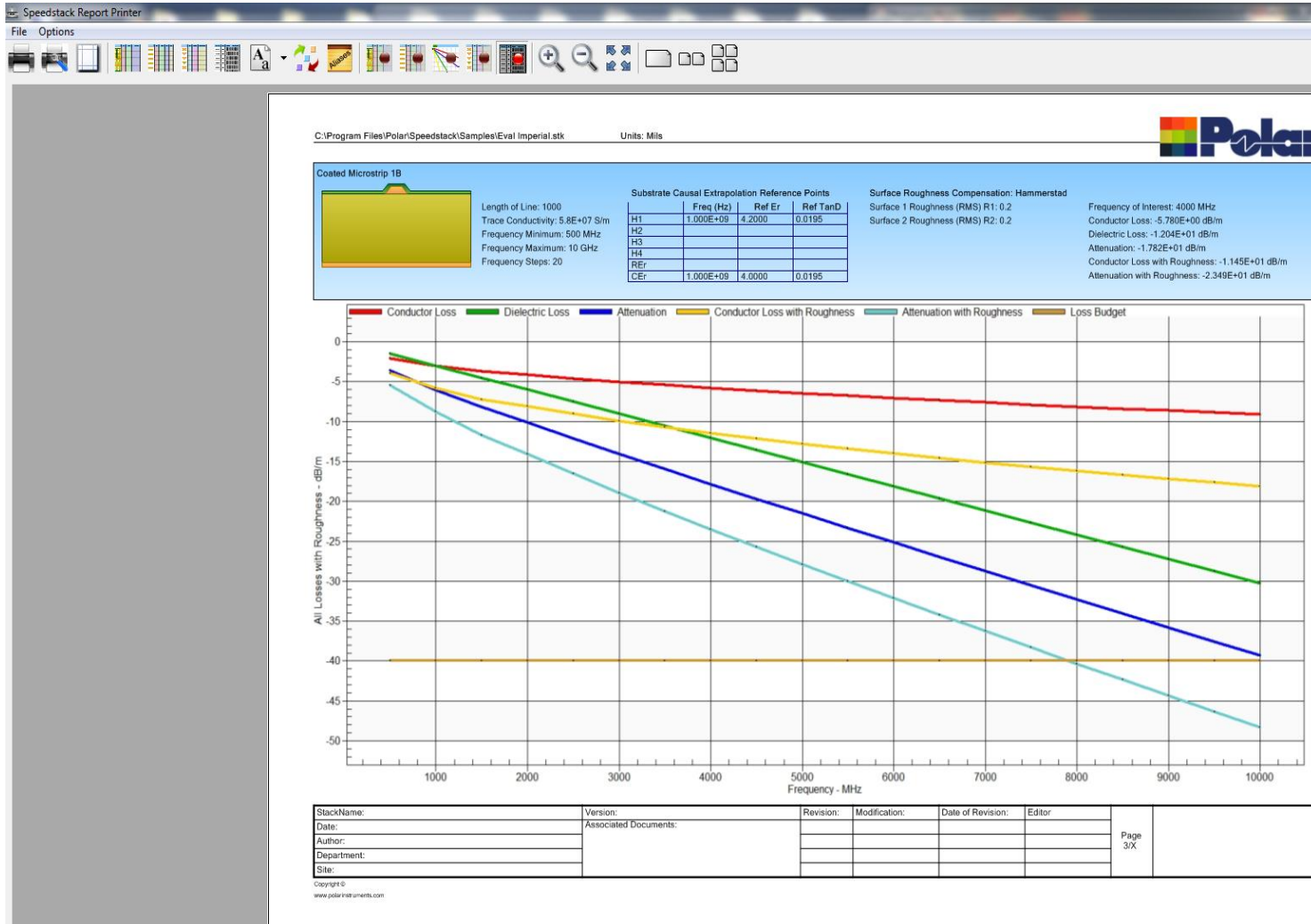


Speedstack – Technical Report enhancements

Informative loss vs frequency graphs have been added to the technical report



Speedstack – Technical Report enhancements



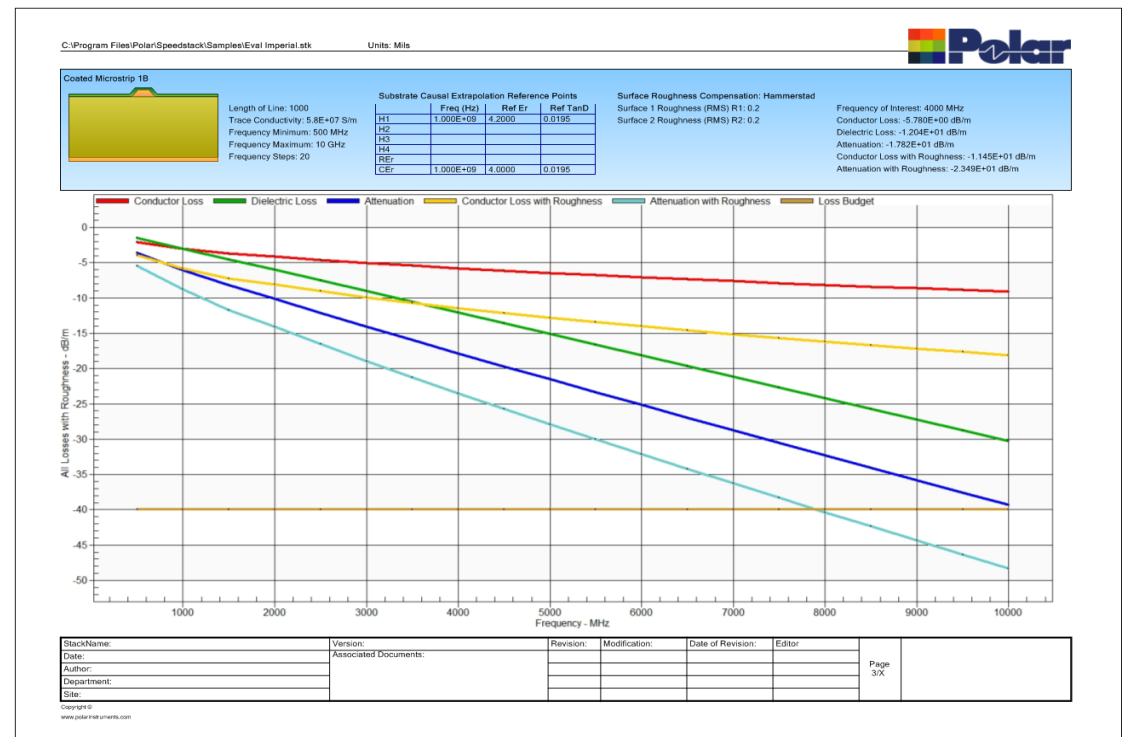
An example of the loss vs frequency graph

Speedstack – Technical Report enhancements

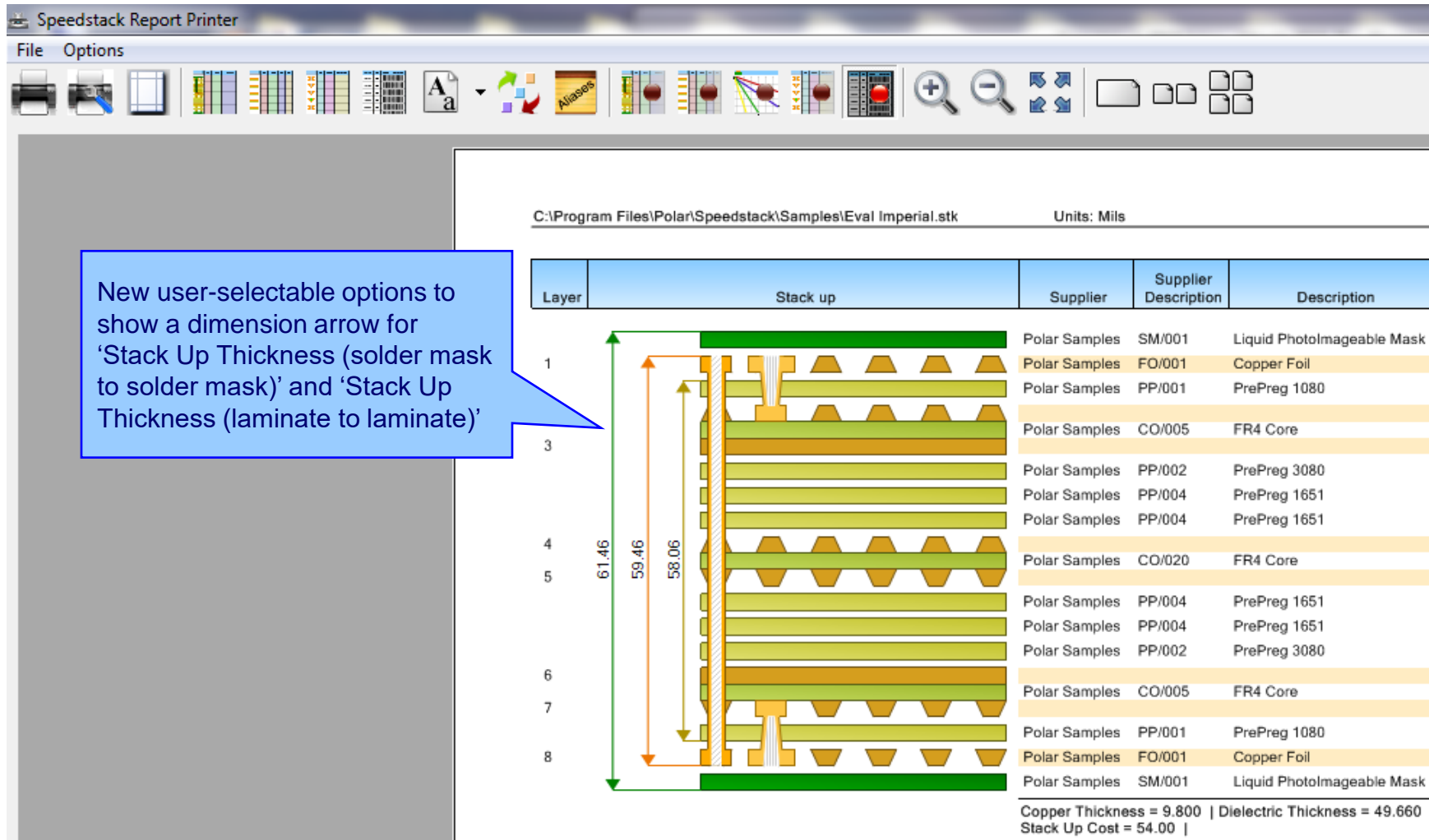
Print Settings

☒ Include Loss Graph for this structure on the report

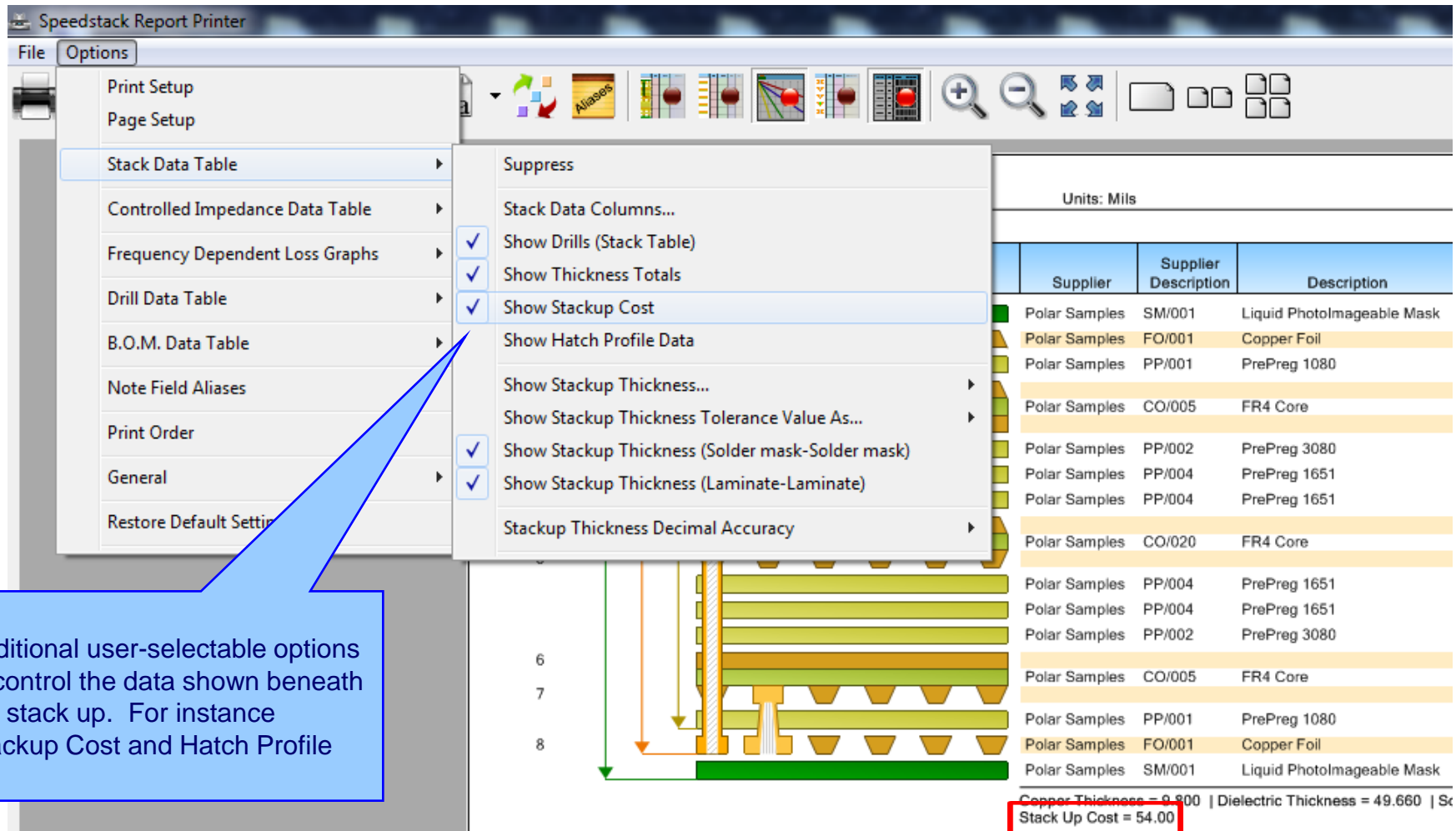
'Include Loss Graph for this structure on the report' checkbox allows the user to nominate which structures will contain a separate loss graph page



Speedstack – Technical Report enhancements



Speedstack – Technical Report enhancements



Speedstack Report Printer

File Options

Print Setup
Page Setup
Stack Data Table
Controlled Impedance Data Table
Frequency Dependent Loss Graphs
Drill Data Table
B.O.M. Data Table
Note Field Aliases
Print Order
General
Restore Default Settings

Suppress
Stack Data Columns...
☒ Show Drills (Stack Table)
☒ Show Thickness Totals
☒ Show Stackup Cost
Show Hatch Profile Data
Show Stackup Thickness...
Show Stackup Thickness Tolerance Value As...
☒ Show Stackup Thickness (Solder mask-Solder mask)
☒ Show Stackup Thickness (Laminate-Laminate)
Stackup Thickness Decimal Accuracy

Units: Mils

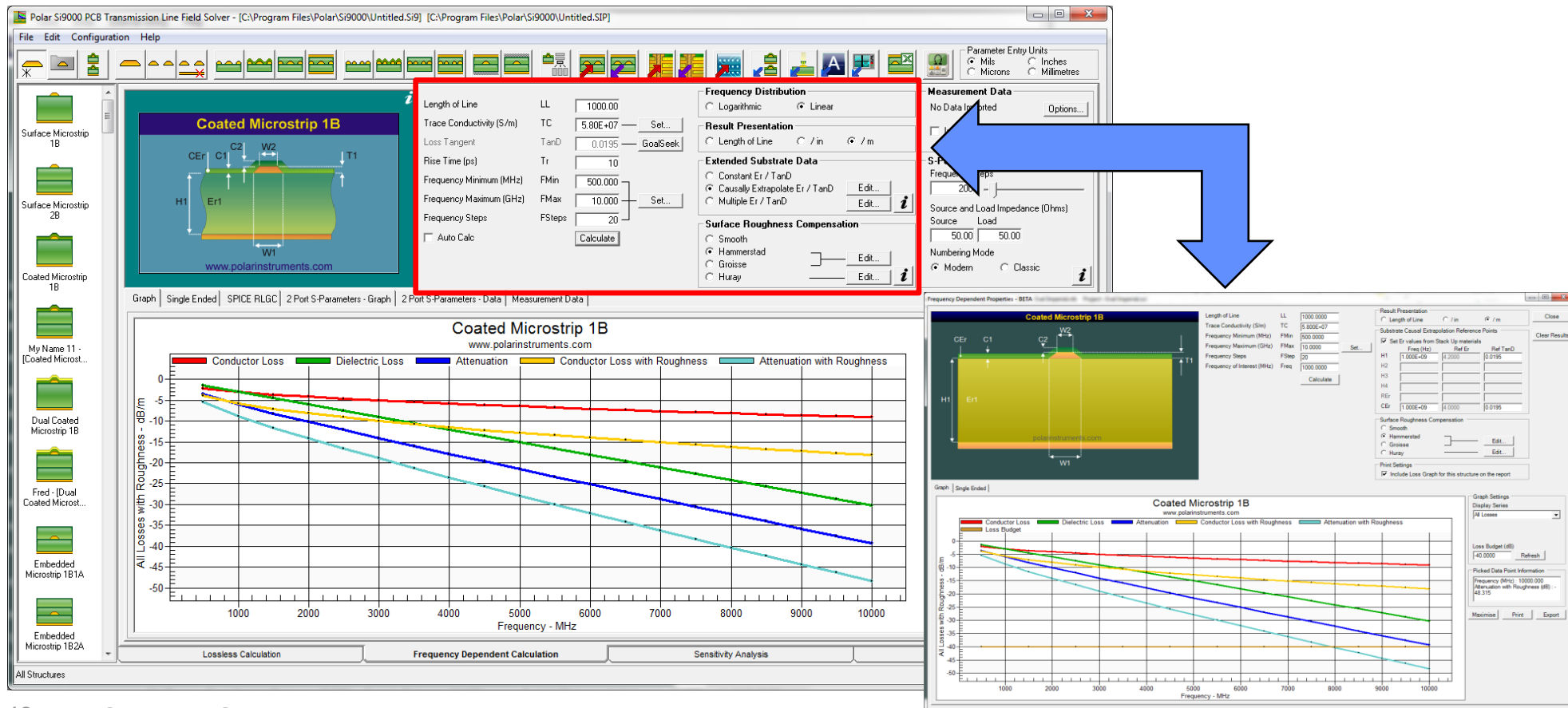
Supplier	Supplier Description	Description
Polar Samples	SM/001	Liquid Photolamable Mask
Polar Samples	FO/001	Copper Foil
Polar Samples	PP/001	PrePreg 1080
Polar Samples	CO/005	FR4 Core
Polar Samples	PP/002	PrePreg 3080
Polar Samples	PP/004	PrePreg 1651
Polar Samples	PP/004	PrePreg 1651
Polar Samples	CO/020	FR4 Core
Polar Samples	PP/004	PrePreg 1651
Polar Samples	PP/004	PrePreg 1651
Polar Samples	PP/002	PrePreg 3080
Polar Samples	CO/005	FR4 Core
Polar Samples	PP/001	PrePreg 1080
Polar Samples	FO/001	Copper Foil
Polar Samples	SM/001	Liquid Photolamable Mask

6
7
8

Copper Thickness = 0.000 | Dielectric Thickness = 49.660 | S
Stack Up Cost = 54.00

Additional user-selectable options to control the data shown beneath the stack up. For instance Stackup Cost and Hatch Profile

Importantly Speedstack 2018 allows comprehensive bidirectional copy and paste from Speedstack into Si9000e including all the relevant loss tangent, roughness and roughness method along with frequencies of interest.



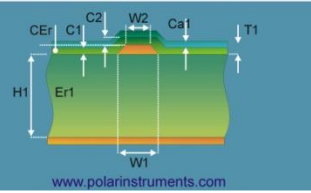
- IMPORTANT NOTE:

- Please contact your local Polar office for information regarding evaluation and upgrading.

- As noted earlier – there are significant changes “under the hood” in both Speedstack, its associated Si8000m / Si9000e field solvers and FlexNet license management – it is important you discuss these especially if you are running a network or WAN license.

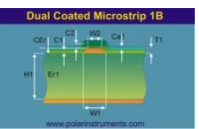
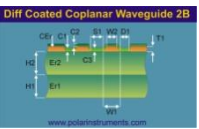
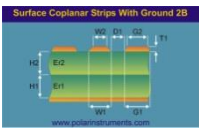
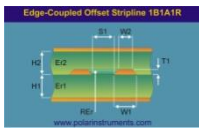
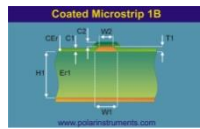
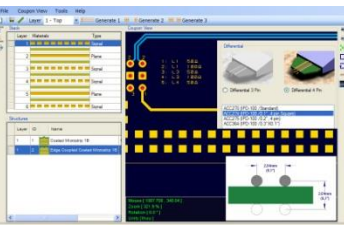
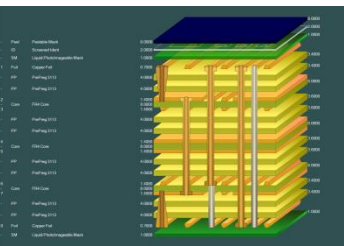
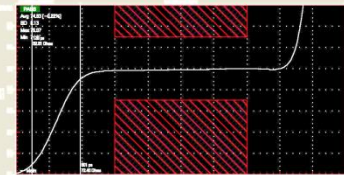
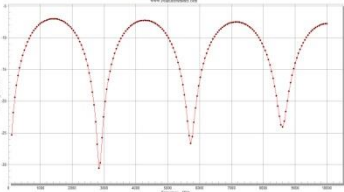


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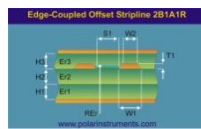
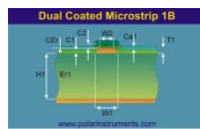
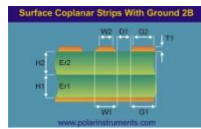
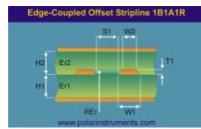
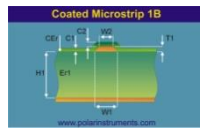
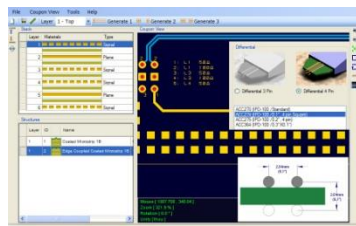
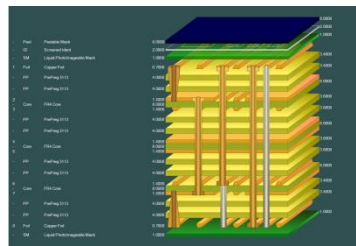
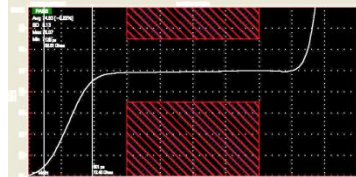
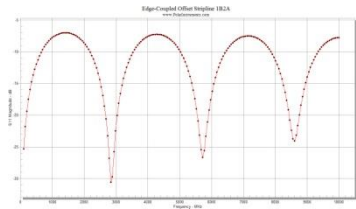
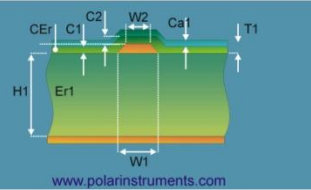


Thank you





Impedance calculation



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