

Speedstack 2019 Introduction

Summary of 2019 what's new Richard Attrill / John Lee – July 2019 (Rev 3)





Introducing Speedstack 2019

Welcome to a preview of what's new in Speedstack 2019 editions.

We have introduced a number of new features that have been requested through our Polarcare software maintenance service.

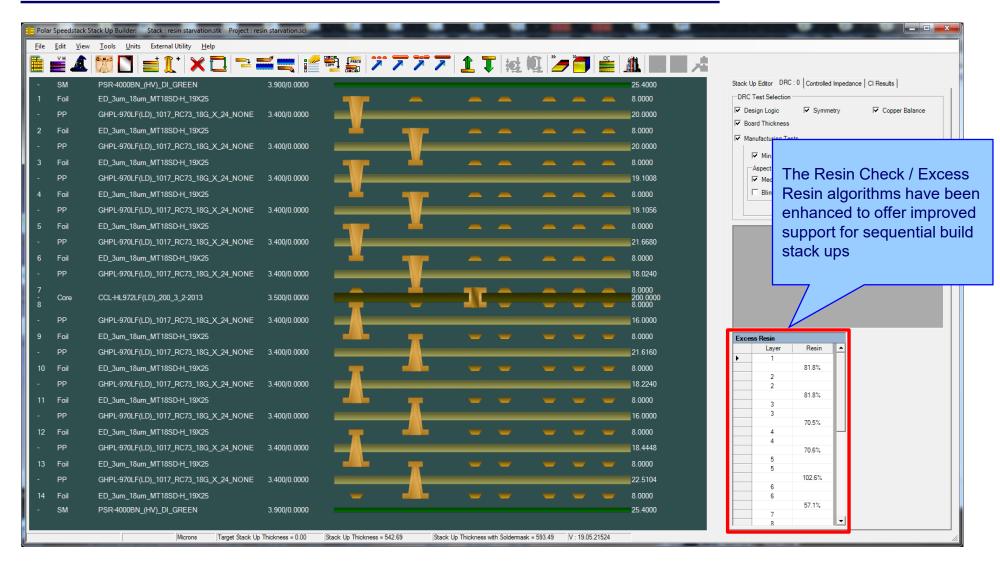
If you would like to have a web-based demonstration please contact your local Polar office, details are shown on the last slide of this presentation.



Speedstack v19.05

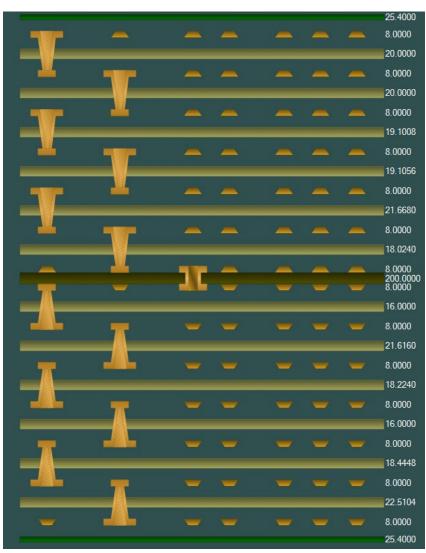


DRC Resin Check / Excess Resin enhancements





DRC Resin Check / Excess Resin enhancements



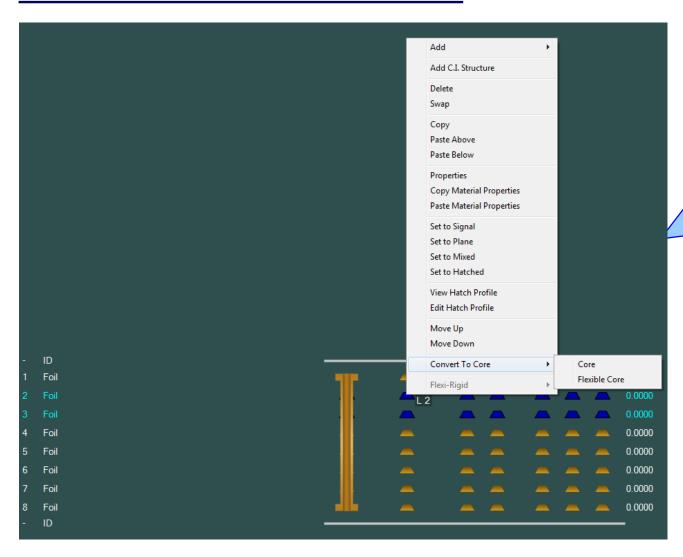
Excess Resin						
	Layer	Resin				
•	1					
		81.8%				
	2					
	2					
		81.8%				
	3					
	3					
		70.5%				
	4					
	4					
		70.6%				
	5					
	5					
		102.6%				
	6					
	6					
		57.1%				
	7					
	8		▼			

Sequential builds require multiple press cycles to achieve the final stack up.

The new Resin Check / Excess Resin algorithms determine the order in which the materials are pressed together and return useful resin percentage information that can be used to determine potential de-lamination problems.



Convert to Core enhancements

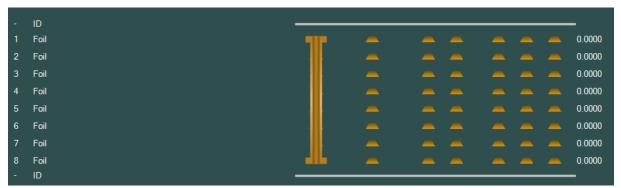


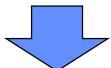
When importing stack up data from some CAD / CAM systems only the electrical layers are defined. In this example an eight layer design has been imported.

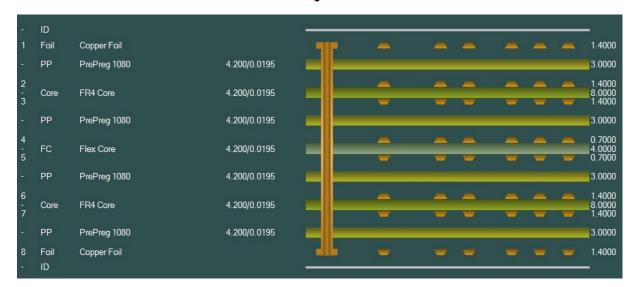
Speedstack allows the user to quickly convert two adjacent electrical layers into Core or Flexible Core materials using the 'Convert to Core' function.



Convert to Core enhancements



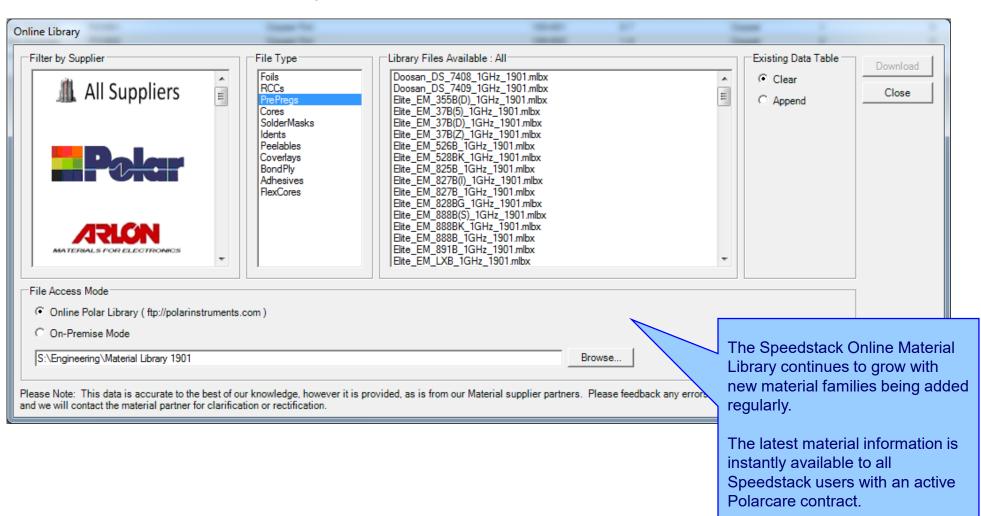




Using 'Convert to Core' alongside other Speedstack editing functions, a simple electrical layer only stack up can be quickly converted into a useful fully defined stack up containing full definitions of foils, prepreg and core materials.



Online Material Library





Printing: Sort impedance structures per layer by type

Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Target Impedance	Tol (+/- %)	Calculated Impedance
1		Edge Coupled Coated Microstrip 1B	1	3	0	8.500	7.500	8.115	100.000	10.000	100.350
2		Coated Microstrip 1B	1	3	0	4.500	3.500	0.000	75.000	10.000	75.870
3		Coated Microstrip 1B	1	3	0	11.476	10.476	0.000	50.000	10.000	49.520
4		Edge Coupled Coated Microstrip 1B	1	3	0	12.542	11.542	10.000	85.000	10.000	85.220

The order that the structures are added to the stack up is the default print order:

- 1. Differential 100 ohms
- 2. Single-Ended 75 ohms
- 3. Single-Ended 50 ohms
- 4. Differential 85 ohms

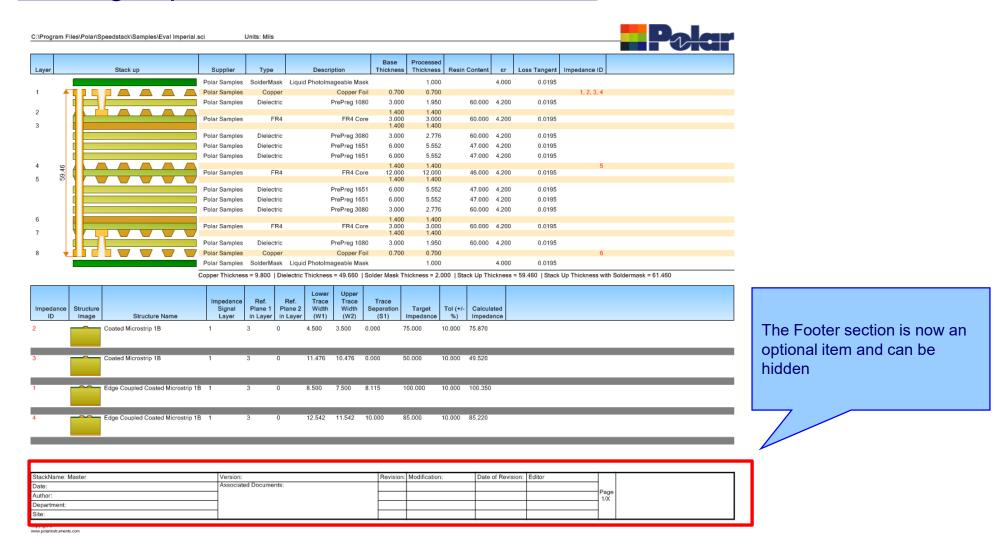
Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Target Impedance	Tol (+/- %)	Calculated Impedance
2		Coated Microstrip 1B	1	3	0	4.500	3.500	0.000	75.000	10.000	75.870
3		Coated Microstrip 1B	1	3	0	11.476	10.476	0.000	50.000	10.000	49.520
1		Edge Coupled Coated Microstrip 1B	1	3	0	8.500	7.500	8.115	100.000	10.000	100.350
4		Edge Coupled Coated Microstrip 1B	1	3	0	12.542	11.542	10.000	85.000	10.000	85.220

New option to sort structures by type has been included with v19.05:

- 1. Single-Ended 75 ohms
- 2. Single-Ended 50 ohms
- 3. Differential 100 ohms
- 4. Differential 85 ohms

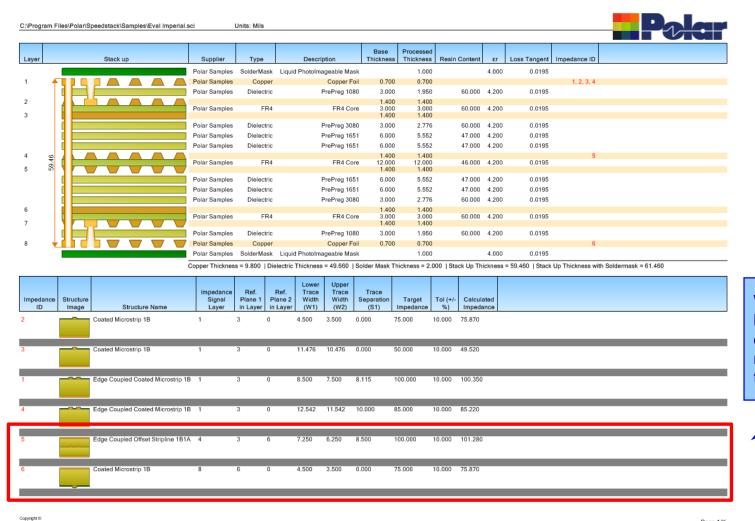


Printing: Option to hide the footer section





Printing: Option to hide the footer section



When the Footer section is hidden the space is used for other data, often reducing the number of pages required for the technical report

Page 1/X

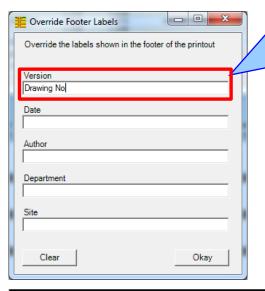




Printing: Customisable footer section

Support for longer stack up names

StackName: POLAR SET2DIL MWPD1636					
Version: A	Associated Documents:	Revision:	Modification:	Date of Revision:	Editor
Date: 22/01/2014		Α	L2/L3 Core Changed	23/10/2016	R Attrill
Author: R Attrill (Polar)		В	Solder Mask Mod	20/05/2019	J Lee
Department: Engineering					
Site: Waterlooville					



Override footer labels using your own company naming conventions.

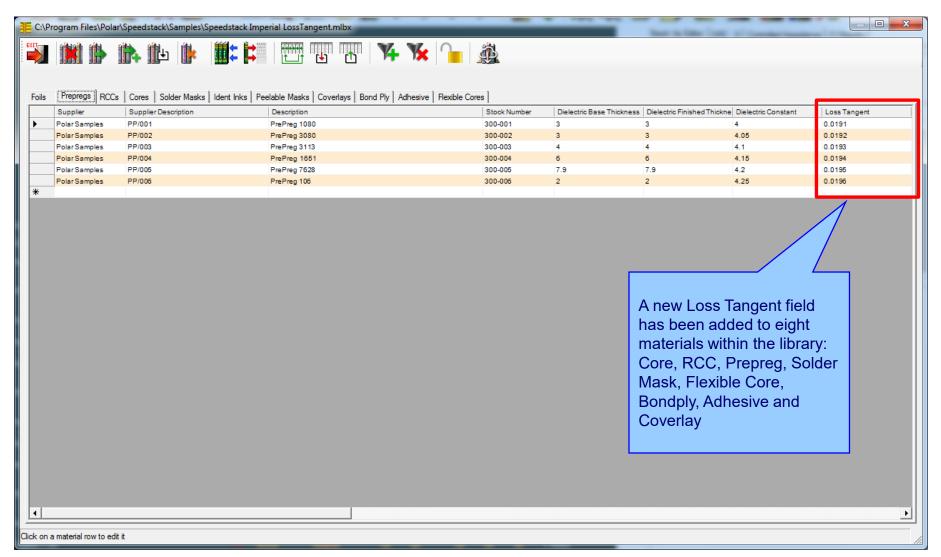
In this example Version has been replaced with Drawing No.

StackName: POLAR SET2DIL MWPD1636					
Drawing No: A	Associated Documents:	Revision:	Modification:	Date of Revision:	Editor
Date: 22/01/2014		A	L2/L3 Core Changed	23/10/2016	R Attrill
Author: R Attrill (Polar)		В	Solder Mask Mod	20/05/2019	J Lee
Department: Engineering					
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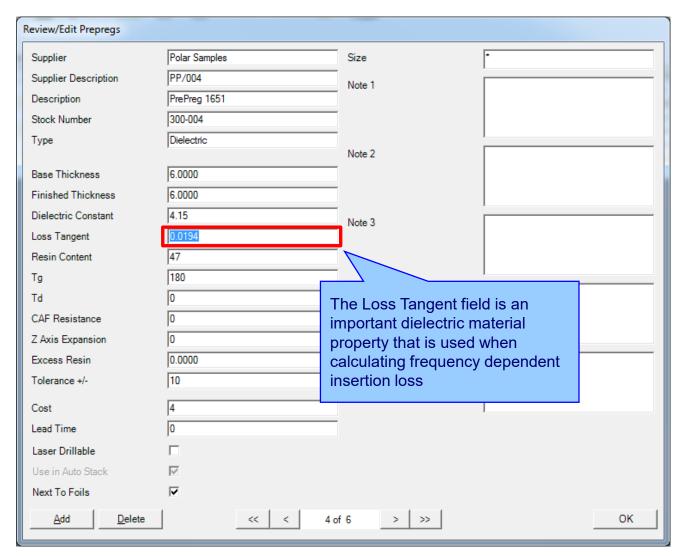


Speedstack v19.01 (January 2019)

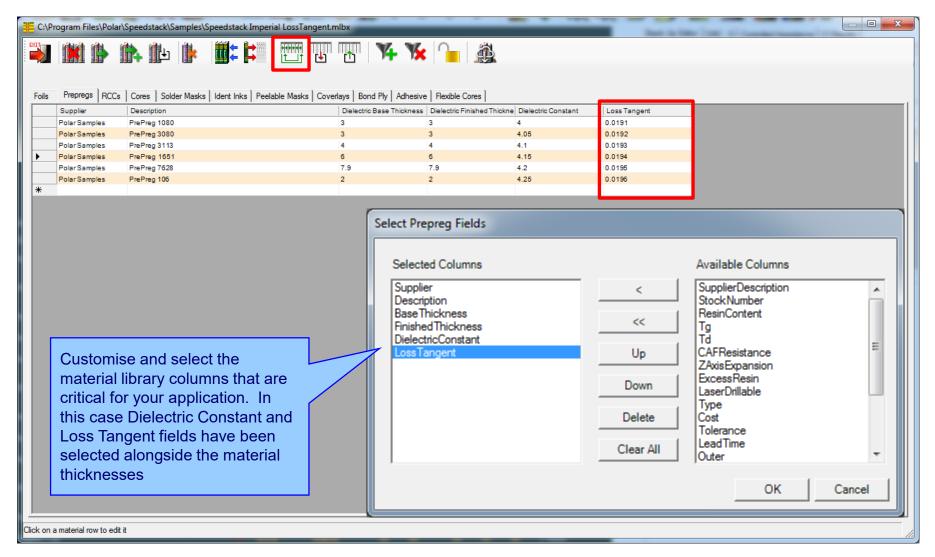




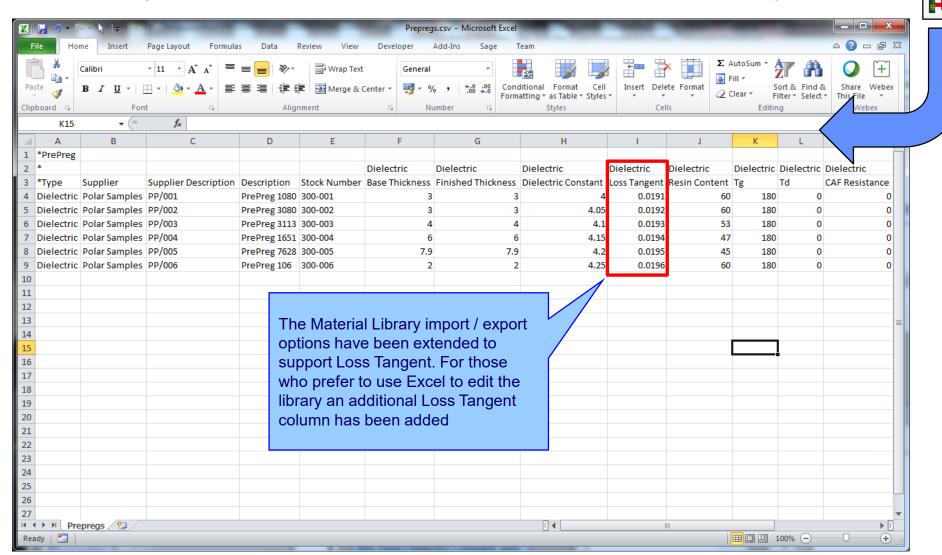






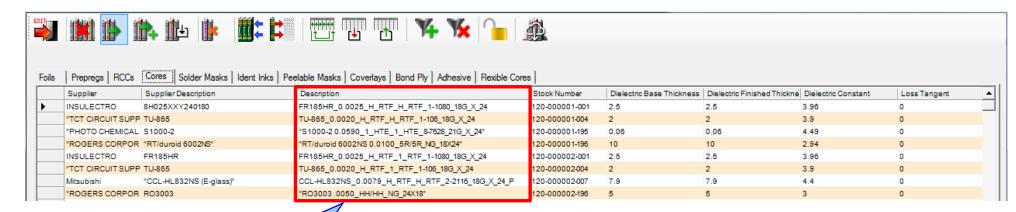








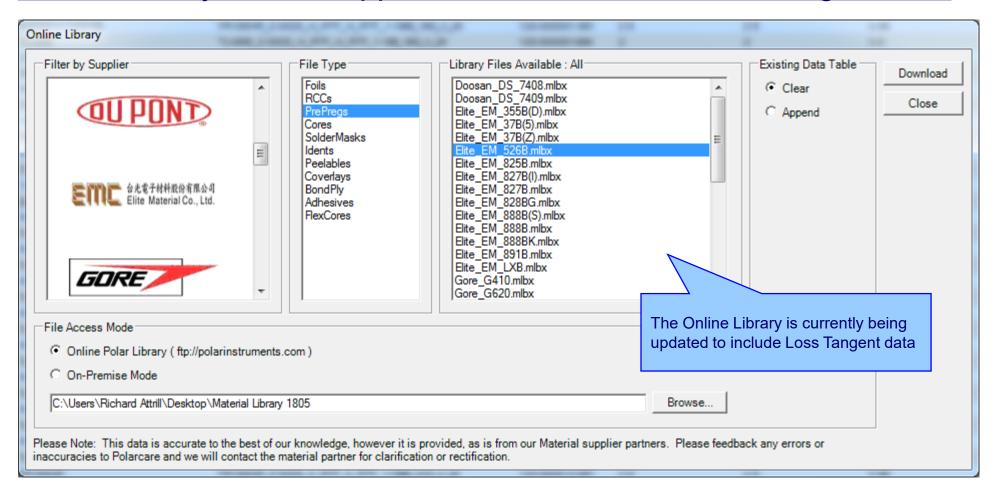
Description column width has been increased



More detailed material descriptions can now be viewed without needing to adjust the column widths

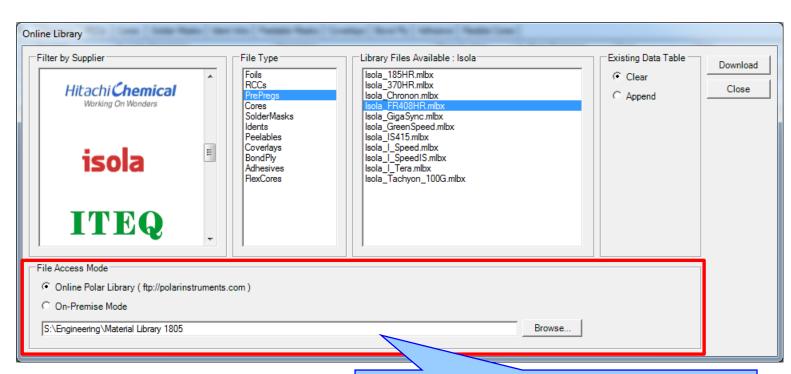


Online Library - Now supports libraries contain Loss Tangent data





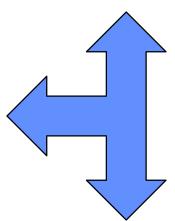
Online Library – On-Premise Mode has been enhanced



The Online Library can access the latest material library data from either the Polar FTP Server or an On-Premise Server.

The On-Premise Mode is ideal for those users where internal security policies prevent access to external FTP servers. Further enhancements have been made when no access to the Polar FTP Server is allowed



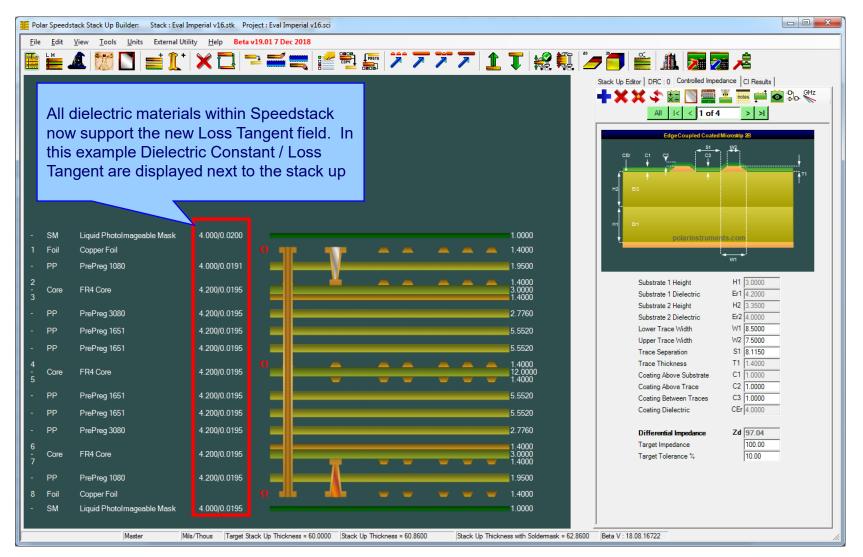




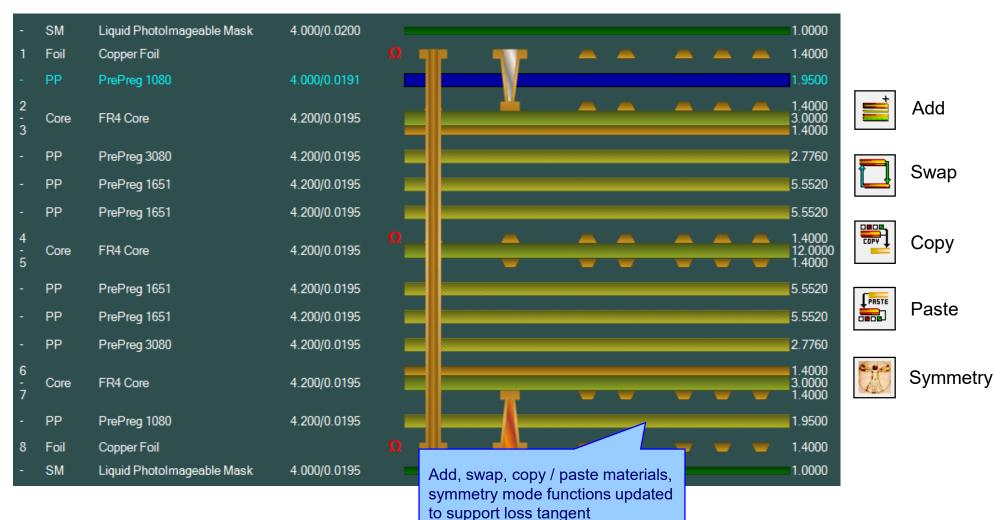
On-Premise Server

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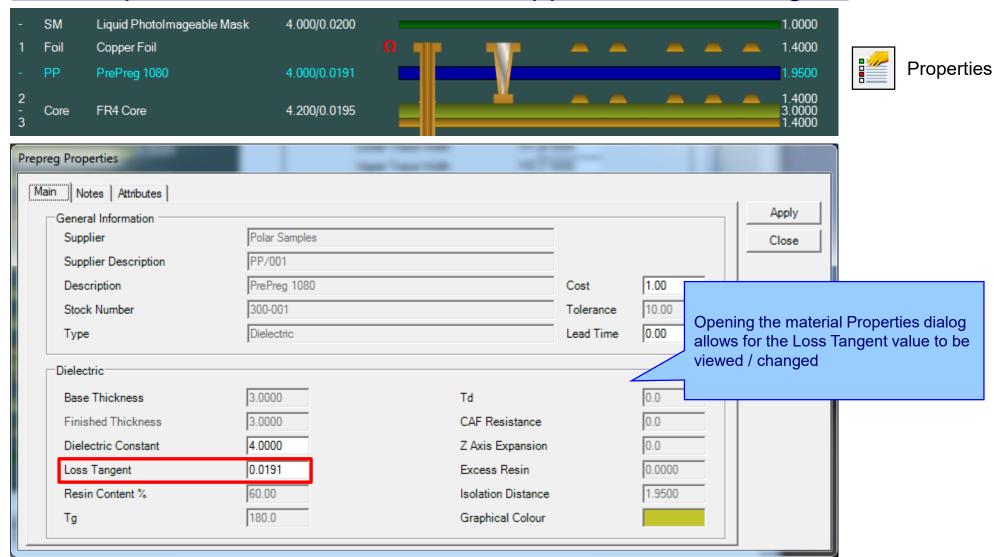




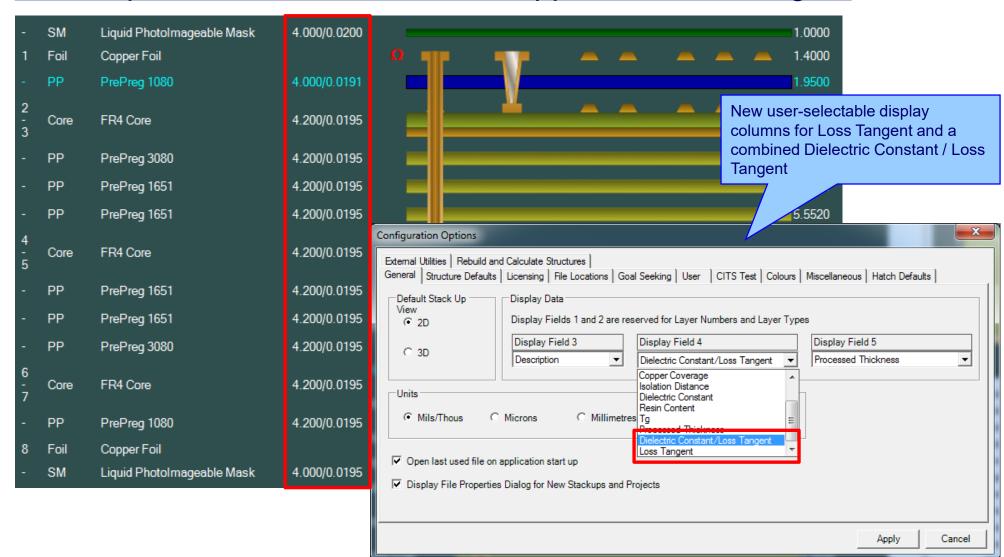






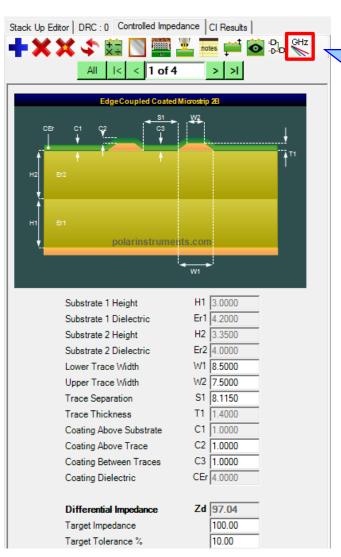








Frequency Dependent Calculation Enhancements (Speedstack Si)

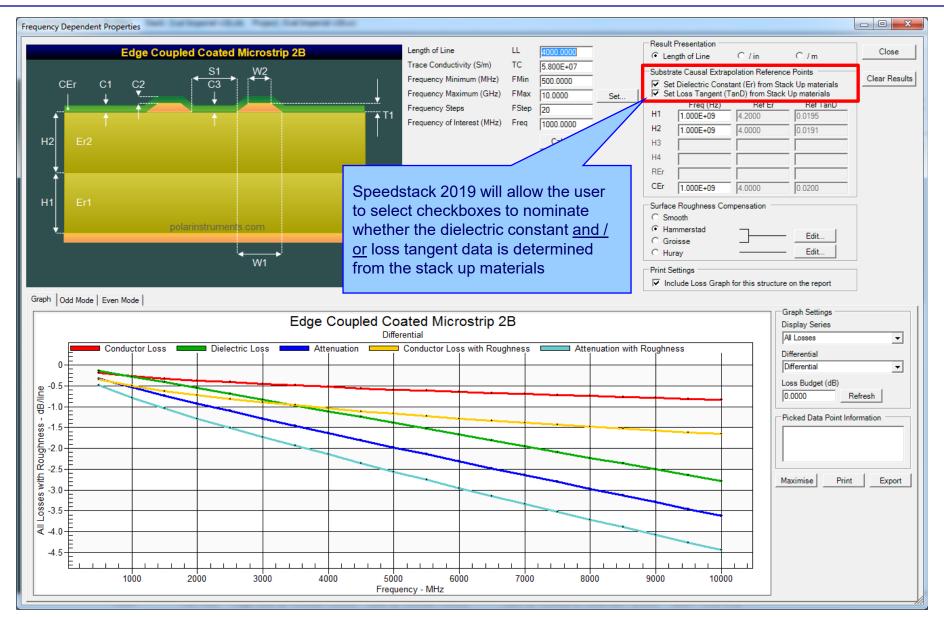


In order to accurately calculate frequency dependent loss it is necessary to know the critical information regarding the transmission line structure.

Speedstack 2019 will now use the dielectric constant and loss tangent data from the stack up

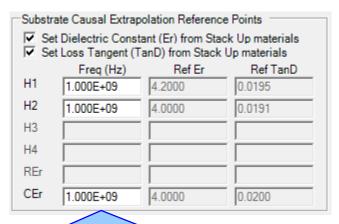


Speedstack 2019 Introduction





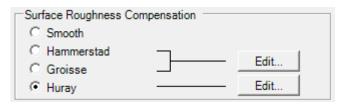
Speedstack – Material and Surface Roughness properties

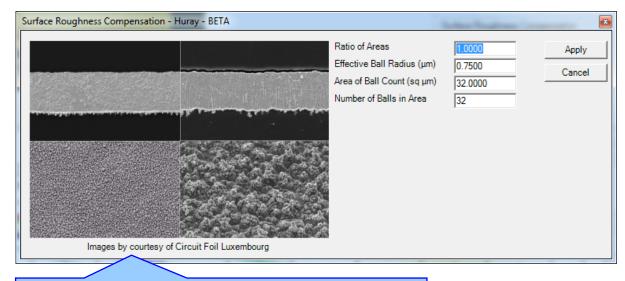


In order to accurately calculate Dielectric Loss it is important to understand the material / substrate properties.

These substrate properties including dielectric constant (Er) and loss tangent (TanD) are specified here for each structure substrate region.

Speedstack causally extrapolates Er and TanD over the specified frequency range using the Svensson-Djordjevic method, hence the ability to specify the extrapolation reference points for each substrate region. The reference point data is usually available from the material supplier data sheet and can be added to the Speedstack material library. The checkbox options will automatically populate these fields from the stack up materials.



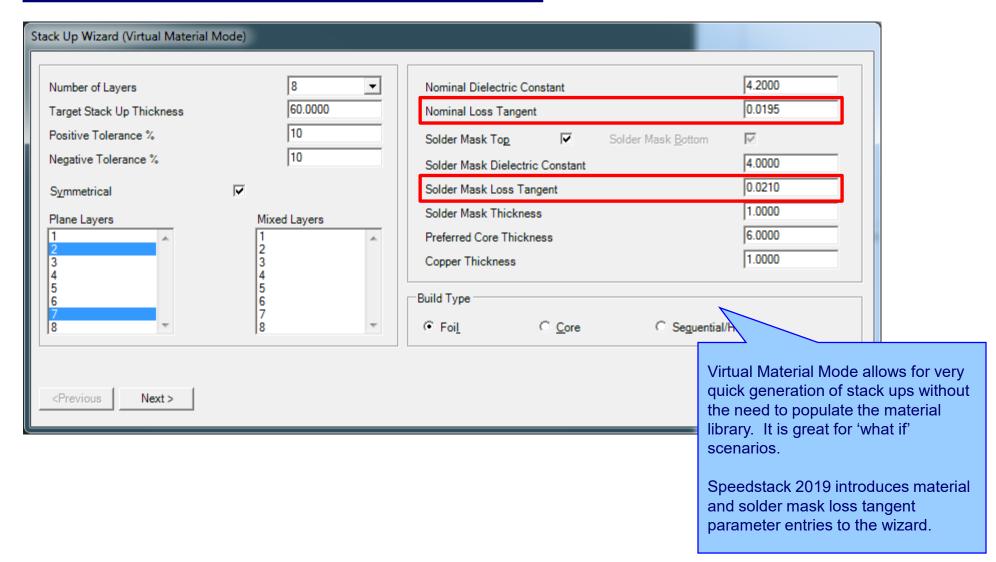


To accurately calculate Conductor Loss it is necessary to specify the surface roughness parameters.

Speedstack supports multiple roughness models: Hammerstad, Groisse, Huray and Cannonball-Huray. In this example the Huray method is used, the dialog prompts for the required roughness parameters.

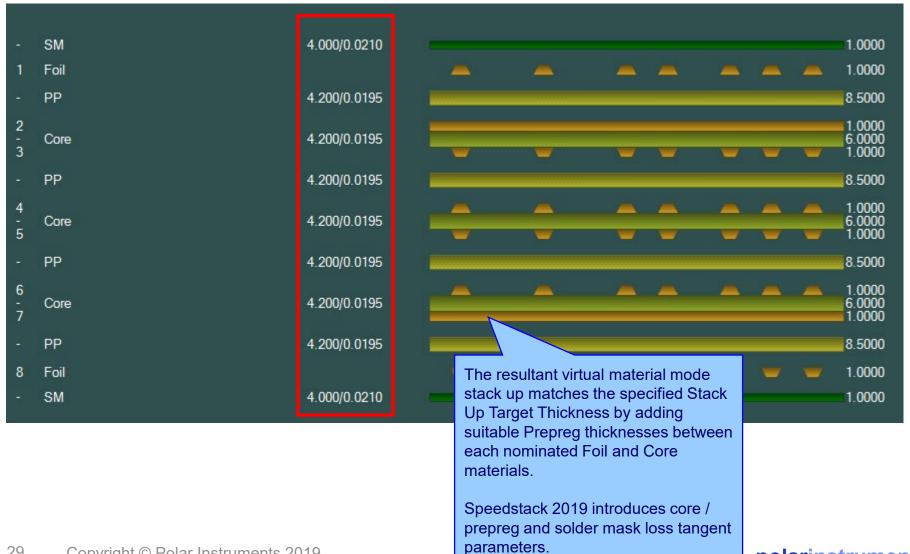


Virtual Material Mode enhancements



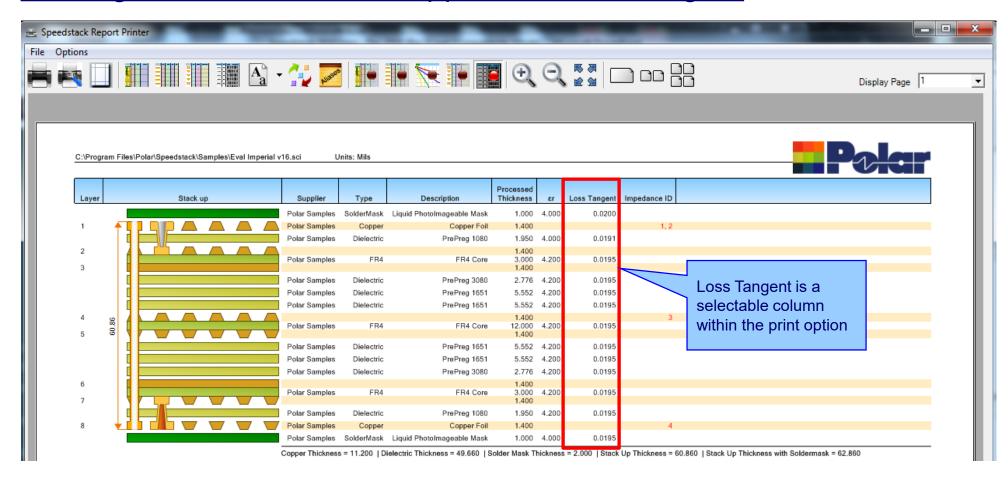


Virtual Material Mode enhancements



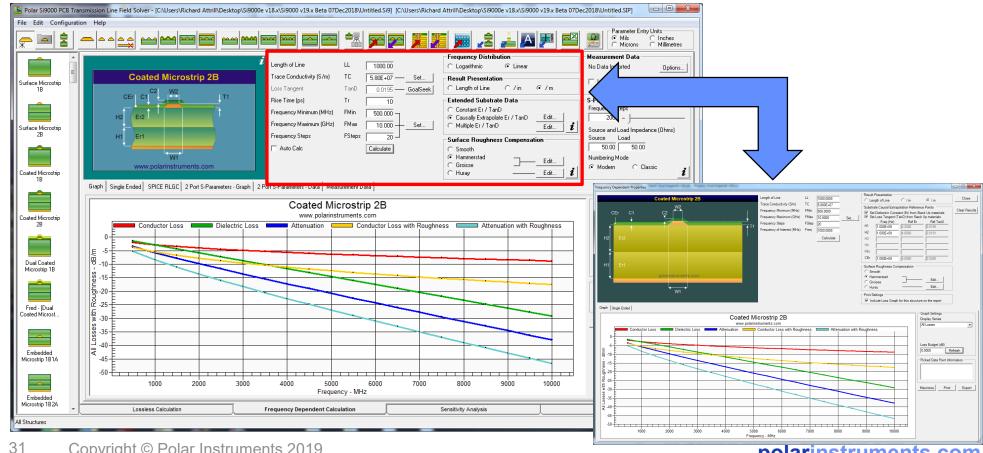


Printing Enhancements - Support for Loss Tangent



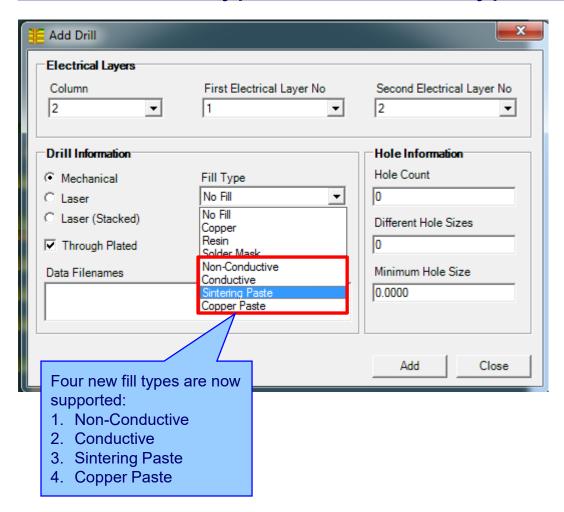


Speedstack 2019 allows comprehensive bidirectional copy and paste from Speedstack into Si9000e including all relevant loss tangent, roughness and roughness method parameters along with frequencies of interest.



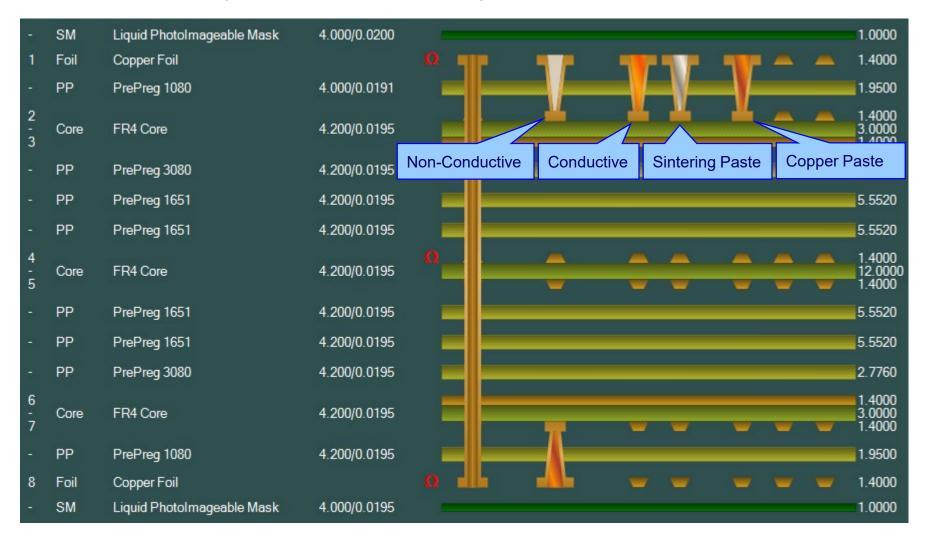


<u>Drill / Via Fill Types – Four new types added</u>



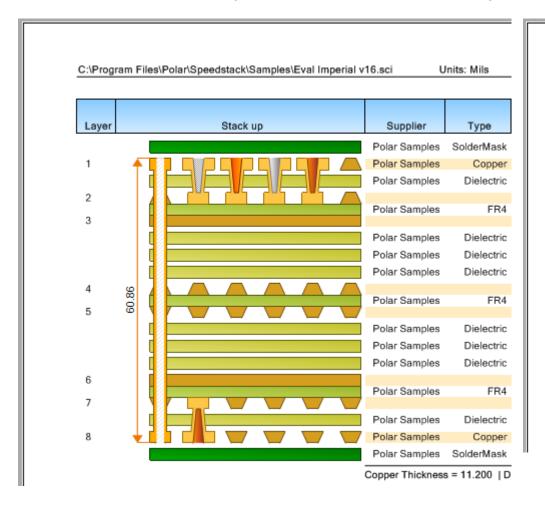


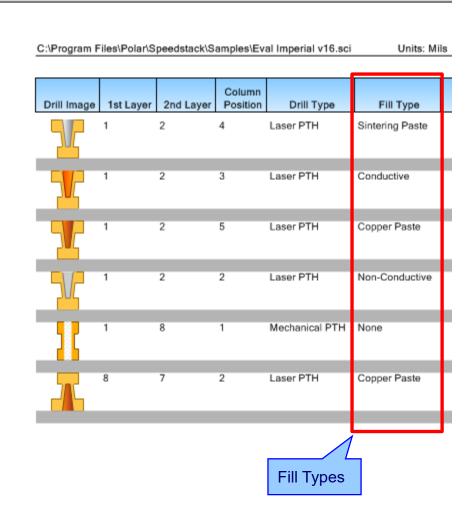
<u>Drill / Via Fill Types – Four new types added</u>





<u>Drill / Via Fill Types – Four new types added</u>







The following Import / Export options have been updated to support new fields introduced with Speedstack 2019:

- XML STKX v16.00 and SSX v6.00 import / export options
- IPC-2581 Rev B import / export options
- CSV export option
- Gerber export option
- **DXF** export option

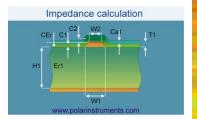
Impedance and Insertion Loss Calculations:

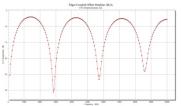
- New amalgamation algorithm now amalgamates multiple substrates to a single substrate for both dielectric constant and loss tangent
- Modifications implemented to support causal surface roughness

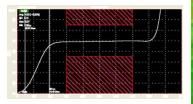
Rigid-Flex Improvements. When introducing air gaps into a sub-stack that previously had contiguous materials it is now possible to reassign this sub-stack to one that contains mini-stacks, by using the 'Reset Mini-Stack Settings' option from the Navigator menu. This is especially useful when designing 'book-binder' or 'doublet' rigid-flex constructions

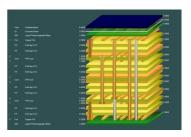
Ucamco Interface. The File menu 'Save and Continue' and 'Save and Quit' options now support the SSX v6.00 file format



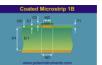




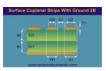


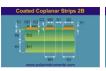




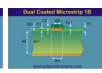


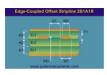










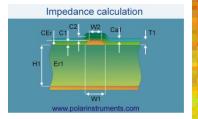


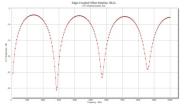
Thank you

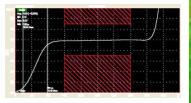


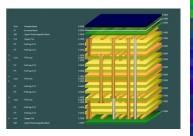
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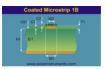






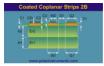




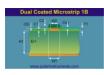


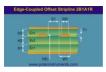












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