









Coated Microstrip 1B Edge-Coupled Offset Striptine 1BAIR Surface Coplaner Strips With Ground 2B Coated Coplaner Strips 2B Diff Coated Coplaner Waveguide 2B Dual Coated Microstrip 1B Edge-Coupled Offset Striptine 2BIA Coated Coplaner Strips 2B Diff Coated Coplaner Waveguide 2B Dual Coated Microstrip 1B Edge-Coupled Offset Striptine 2BIA Coated Coplaner Strips 2B Diff Coated Coplaner Waveguide 2B Dual Coated Microstrip 1B Edge-Coupled Offset Striptine 2BIA Coated Coplaner Strips 2B Diff Coated Coplaner Waveguide 2B Dual Coated Microstrip 1B Edge-Coupled Offset Striptine 2BIA Coated Coplaner Strips 2B Diff Coated Coplaner Waveguide 2B Dual Coated Microstrip 1B Edge-Coupled Offset Striptine 2BIA Coated Coplaner Strips 2B Diff Coated Coplaner Strips 2B Diff Coated Coplaner Waveguide 2B Diff Coated Coplaner Waveguide 2B Diff Coated Coplaner Strips 2B Diff Coated Coplaner Waveguide 2B Diff Coated Coplaner Strips 2B Dif

Si9000e 2021 – 2023 Preview

Richard Attrill – September 2023 (Rev 5)



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Si9000e v23.09.21 (September 2023)



New Frequency of Interest option added





New Frequency of Interest option added



- Selecting Apply to Current Structure will place those frequency values with the current selected structure so the next time the structure is calculated the results for each specified frequency will be placed on the main dialog, giving immediate feedback of the results at those frequency values.
- Selecting Apply to All Structures will place those same nominated frequency values on all structures in the Si9000e, including those structures that exist in a Project.
- In this example we have keyed in the four Delta-L 4.0 frequencies of 4GHz, 8GHz, 12.89GHz and 16GHz



New Frequency of Interest option added





Si9000e v23.08.02 (August 2023)



New Export to Touchstone Format for Multiple Length of Lines





Si9000e v23.06.01 (June 2023)













araph Udd Mode Even Mode SPILE HLIGU 4 Port S-Parameters - Graph 4 Port S-Parameters - Oata Mixed Mode S-Parameters - Graph Mixed Mode S-Parameters - Oata Crosstalk Measurement Data																	
Frequency Hz	Impedance Real Ohms	Impedance Imaginary Ohms	Impedance Magnitude Ohms	Inductance H/line	Resistance Ohms/line	Capacitance F/line	Conductance S/line	Skin Depth m	Smooth Conductor Loss dB/line	Dielectric Loss dB/line	Smooth Attenuation dB/line	Conductor Loss with Roughness dB/line	Attenuation with Roughness dB/line	Modal Phase Velocity m/s	Alpha Np/line	Alpha dB/line	Beta rad/line
5.000E+08	3.161E+01	-3.664E-01	3.161E+01	5.955E-09	7.989E-01	5.964E-12	3.653E-04	2.955E-06	-9.873E-02	-4.717E-02	-1.459E-01	-1.128E-01	-1.599E-01	1.348E+08	1.841E-02	-1.599E-01	5.921E-01
1.000E+09	3.138E+01	-2.268E-01	3.138E+01	5.869E-09	1.253E+00	5.964E-12	7.307E-04	2.090E-06	-1.399E-01	-9.376E-02	-2.337E-01	-1.792E-01	-2.730E-01	1.358E+08	3.142E-02	-2.730E-01	1.176E+00
1.500E+09	3.126E+01	-1.675E-01	3.126E+01	5.827E-09	1.660E+00	5.964E-12	1.096E-03	1.706E-06	-1.715E-01	-1.403E-01	-3.118E-01	-2.391E-01	-3.794E-01	1.363E+08	4.368E-02	-3.794E-01	1.757E+00
2.000E+09	3.119E+01	-1.330E-01	3.119E+01	5.799E-09	2.043E+00	5.964E-12	1.461E-03	1.478E-06	-1.982E-01	-1.867E-01	-3.849E-01	-2.957E-01	-4.824E-01	1.366E+08	5.554E-02	-4.824E-01	2.337E+00
2.500E+09	3.113E+01	-1.097E-01	3.113E+01	5.779E-09	2.410E+00	5.964E-12	1.827E-03	1.322E-06	-2.217E-01	-2.331E-01	-4.548E-01	-3.501E-01	-5.832E-01	1.368E+08	6.714E-02	-5.832E-01	2.916E+00
3.000E+09	3.109E+01	-9.260E-02	3.109E+01	5.763E-09	2.766E+00	5.964E-12	2.192E-03	1.207E-06	-2.429E-01	-2.795E-01	-5.224E-01	-4.028E-01	-6.823E-01	1.370E+08	7.856E-02	-6.823E-01	3.495E+00
3.500E+09	3.105E+01	-7.937E-02	3.105E+01	5.750E-09	3.112E+00	5.964E-12	2.557E-03	1.117E-06	-2.624E-01	-3.259E-01	-5.883E-01	-4.543E-01	-7.802E-01	1.372E+08	8.982E-02	-7.802E-01	4.072E+00
4.000E+09	3.102E+01	-6.871E-02	3.102E+01	5.739E-09	3.452E+00	5.964E-12	2.923E-03	1.045E-06	-2.806E-01	-3.723E-01	-6.529E-01	-5.047E-01	-8.770E-01	1.373E+08	1.010E-01	-8.770E-01	4.650E+00
4.500E+09	3.100E+01	-5.988E-02	3.100E+01	5.730E-09	3.785E+00	5.964E-12	3.288E-03	9.851E-07	-2.976E-01	-4.187E-01	-7.163E-01	-5.543E-01	-9.730E-01	1.374E+08	1.120E-01	-9.730E-01	5.227E+00
5.000E+09	3.097E+01	-5.241E-02	3.097E+01	5.721E-09	4.114E+00	5.964E-12	3.653E-03	9.346E-07	-3.138E-01	-4.650E-01	-7.788E-01	-6.032E-01	-1.068E+00	1.375E+08	1.230E-01	-1.068E+00	5.803E+00
5.500E+09	3.095E+01	-4.597E-02	3.095E+01	5.714E-09	4.437E+00	5.964E-12	4.019E-03	8.911E-07	-3.291E-01	-5.114E-01	-8.405E-01	-6.515E-01	-1.163E+00	1.376E+08	1.339E-01	-1.163E+00	6.379E+00
6.000E+09	3.094E+01	-4.034E-02	3.094E+01	5.707E-09	4.757E+00	5.964E-12	4.384E-03	8.532E-07	-3.438E-01	-5.577E-01	-9.015E-01	-6.992E-01	-1.257E+00	1.377E+08	1.447E-01	-1.257E+00	6.955E+00
6.500E+09	3.092E+01	-3.536E-02	3.092E+01	5.702E-09	5.073E+00	5.964E-12	4.750E-03	8.197E-07	-3.579E-01	-6.040E-01	-9.619E-01	-7.464E-01	-1.350E+00	1.377E+08	1.555E-01	-1.350E+00	7.531E+00
7.000E+09	3.091E+01	-3.091E-02	3.091E+01	5.696E-09	5.387E+00	5.964E-12	5.115E-03	7.899E-07	-3.714E-01	-6.503E-01	-1.022E+00	-7.931E-01	.3.4495.00	J., . 1 9705 / 00	. 3.FEDE A4.	. 1 442E-DQ	. 0.1005.00L
7.500E+09	3.089E+01	-2.691E-02	3.089E+01	5.691E-09	5.697E+00	5.964E-12	5.480E-03	7.631E-07	-3.845E-01	-6.967E-01	-1.081E+00	-8.395E-01	C	ony Result	s to Clipbo	ard (for F	xcel)
8.000E+09	3.088E+01	-2.327E-02	3.088E+01	5.686E-09	6.005E+00	5.964E-12	5.846E-03	7.389E-07	-3.971E-01	-7.430E-01	-1.140E+00	-8.855E-01	-	copy results to clipboard (for excel)			
8.500E+09	3.087E+01	-1.995E-02	3.087E+01	5.682E-09	6.310E+00	5.964E-12	6.211E-03	7.168E-07	-4.093E-01	-7.893E-01	-1.199E+00	-9.311E-01	-1.720E+00	1.380E+08	1.981E-01	-1.720E+00	9.831E+00
9.000E+09	3.086E+01	-1.690E-02	3.086E+01	5.678E-09	6.613E+00	5.964E-12	6.576E-03	6.966E-07	-4.212E-01	-8.356E-01	-1.257E+00	-9.764E-01	-1.812E+00	1.380E+08	2.086E-01	-1.812E+00	1.041E+01
9.500E+09	3.085E+01	-1.409E-02	3.085E+01	5.674E-09	6.914E+00	5.964E-12	6.942E-03	6.780E-07	-4.328E-01	-8.819E-01	-1.3155 0	-1.021E+00	-1.903E+00	1.381E+08	2.191E-01	-1.903E+00	1.098E+01
1.000E+10	3.084E+01	-1.148E-02	3.084E+01	5.671E-09	7.213E+00	5.964E-12	7.307E-03	6.609E-07	-4.441E-01	-9.282E-01	_+00	-1.066E+00	-1.994E+00	1.381E+08	2.296E-01	-1.994E+00	1.155E+01

The Conductor Loss with Roughness results data is also shown alongside the other field solver results.

The complete set of results can be exported to third-party tools like Excel using the right-click menu | Copy Results to Clipboard

<u>Project Graphing Enhancements – now supports structures within</u> the Project with varying Length of Line

Other enhancements

• FlexNet Publisher / FLEXIm v11.19.0.0 supported

Si9000e v22.09.01 (September 2022)

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Enhancements to the Import Polar CITS Datalog File option

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Whilst working with controlled impedance designs it is often desirable to compare the reality of the measurement data against the modelled structure.

'Closing the loop' between the predicted and actual measured results has a number of benefits for both the design and fabrication environments. It allows for fine tuning of the structure parameters in future manufacturing batches, statistical analysis and improved overall process control.

This capability within the Polar's Si8000m / Si9000e field solver products allows the user to quickly import measurement data directly from the industry-standard Polar Controlled Impedance Test System (CITS).

If you are a design customer using the Si8000m / Si9000e and would like to use this feature, please request the Polar CITS Datalog File from your fabricator.

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Import CITS Datalog File option – feature recap

Step 2 : Select Data	a Log Record	Each test record type found in the data
Data Log Records	Description - L01, Layer - 1, Nominal Impedance - 60.00	log file is listed in the drop down. In this
Project Structure	Description - L01, Layer - 1, Nominal Impedance - 60.00 Description - L03 Layer - 3 Nominal Impedance - 60.00	case there are four tests.
Description	Description - L08, Layer - 8, Nominal Impedance - 60.00	
Nominal Impedance	60.00 Tol+ % 10.00 Tol- % 10.00	📕 Polar Si9000 PCB Tr
		File Edit Configura
Step 2 : Select Data	a Log Record	
Data Log Records	Description - L01, Layer - 1, Nominal Impedance - 60.00	
Project Structure	L1 60 ohms (1)	
Description	L1 60 ohms (1) L3 60 ohms (2)	L1 60 ohms (1)
Nominal Impedance	L6 60 ohms (3)	
ch one of the four m	nodelled	L3 60 ohms (2)
es from the Project a data log test reco	group and simply	
he structure from th	le Project	
re dropdown		16 50 abres (3)
	Fou	r structures loaded into
	the	

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Measurement Data:

The CITS Data Log data may also be viewed in a data grid layout. This is especially useful for viewing the Result data (Pass / Fail)

Graph Analysis (Line) Analysis (Bar) Measurement Data

Result	Index Board Serial		Date	Time	Average	SD	Maximum	Minimum	Station	Description	Layer	Nominal	Tol+ %	Tol- %	Instrument	Serial No
Passed	1	- 24	05/02/13	12:48	60.8	0.8	61.9	59.56	_TEST STATION 1_	L01		1 60	10	1	CITS880	17581
Passed	2	29	05/02/13	12:50	61.77	0.95	63.21	59.93	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	3	17	05/02/13	12:51	63.01	0.94	64.48	61.68	_TEST STATION 1_	L01		1 60	10	10	CITS880	17581
Passed	4	- 39	05/02/13	12:52	63.22	1.07	64.62	61.29	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	5	8	05/02/13	12:59	63.93	0.95	65.32	62.2	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	6	10	05/02/13	13:00	61.17	0.89	62.69	59.63	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	7	32	05/02/13	13:01	62.38	0.88	63.58	60.72	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	8	21	05/02/13	13:01	62.37	0.82	63.88	60.98	_TEST STATION 1_	L01		1 60	10	10	CITS880	17581
Passed	9	4	05/02/13	13:02	63.35	0.68	64.41	61.75	_TEST STATION 1_	L01		1 60	10	10	CITS880	17581
Passed	10	- 33	05/02/13	13:03	61.81	0.78	62.95	60.09	_TEST STATION 1_	L01		1 60	10	10	CITS880	17581
Passed	11	18	05/02/13	13:03	60.22	0.62	61.48	59.09	_TEST STATION 1_	L01		1 60	10	10	CITS880	17581
Passed	12	3	05/02/13	13:04	60.54	0.75	62.1	59.19	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	13	15	05/02/13	13:05	61.46	0.73	62.83	60.12	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	14	2	05/02/13	13:05	60.09	0.67	61.24	58.57	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	15	23	05/02/13	13:06	61.01	0.78	62.4	59.69	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	16	5	05/02/13	13:07	61.05	0.63	62.14	59.49	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	17	6	05/02/13	13:07	61.54	0.8	62.98	60.11	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	18	76	05/02/13	13:08	62.49	0.92	63.44	60.32	_TEST STATION 1_	L01		1 60	10	10	D CITS880	17581
Passed	19	11	05/02/13	13:09	61.79	0.83	63.08	60.37	_TEST STATION 1_	L01		1 60	10	10	CITS880	17581
Passed	20	- 31	05/02/13	13:09	60.25	0.65	61.37	58.85	_TEST STATION 1_	L01		1 60	10	10	CITS880	17581
Passed	21	12	05/02/13	13:10	62.01	0.69	63.24	60.65	_TEST STATION 1_	L01		1 60	10	10	CITS880	17581
Passed	22	7	05/02/13	13:11	63.08	1.13	64.89	60.84	_TEST STATION 1_	L01		1 60	10	10	CITS880	17581
Passed	23	19	05/02/13	13:11	61.63	0.72	62.81	60 19	TEST STATION 1	1.01		1 60	10	11	011111111111111111111111111111111111111	17581

New Manually Set Y-Axis option for the All Losses plot

New Manually Set Y-Axis option for the All Losses plot

Enhancements to the Import Touchstone Format option

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Si9000e v22.04 (April 2022)

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New Differential Via Calculation capability

📕 Polar Si9000 PCB Transmission Line Field Solver - [C:\Program Files (x86)\Polar\Si9000\Untitled.Si9] [C:\Program Files (x86)\Polar\Si9000\Untitled.SIP] \times File Edit Configuration Help Parameter Entry Units 📥 🗛 🗩 Ż Mils <u>--</u>--C Inches O Microns O Millimetres Tolerance Minimum Maximum + - 9 Substrate 1 Height H1 8.5000 8.5000 8.5000 0.0000 Calculate Edge-Coupled Coated Microstrip 1B Substrate 1 Dielectric Er1 4.2000 🕂 : <u>- 20</u>00 4.2000 Calculate Edge-Coupled Lower Trace Width W1 Surface Microst. 5.0000 ÷ ± 0.000 CEr <u></u>_T1 Upper Trace Width W2 4.0000 The new Via Checks toolbar option. Trace Separation S1 2.2810 -Trace Thickness T1 H1 Er1 1.2000 -Edge-Coupled Surface Microst Coating Above Substrate C1 This Differential Via Calculation is now 1.0000 - 1 Coating Above Trace C2 1.0000 part of a new tabbed Via Checks W1 Coating Between Traces C3 1.0000 www.polarinstruments.com dialog accessible from the toolbar. It CEr **Coating Dielectric** 4.2000 🗧 Edge-Coupled Coated Microst also contains the Via Stub Check and Notes: (First 5 lines will print) Interface Style Add your comments here Via Pad / Anti Pad Coaxial Calculation Differential Impedance Zdiff 85.02 C Standard Extended that were previously present on the Edge-Coupled Coated Microst. G.S Convergence main interface Fine (Slower) C Coarse (Faster) Tolerance Mode Edge-Coupled Dual Coate. Absolute Percentage (%) Parameter Snap Edge-Coupled Auto Calc Dual Coate.. Snap Edge-Coupled Embedded Mi.. Edge-Coupled Embedded Mi. Lossless Calculation Sensitivity Analysis Frequency Dependent Calculation Differential Structures

New Differential Via Calculation

📕 Via Checks			×
Via Stub Check Via Pad / Anti-Pad Calculation Differential Via Calculation			
Differential Via Calculation	Anti-Pad Style C Horizontal Oval Anti-Pad	Round / Oblong Anti-Pad	Close
Round Anti-Pad (APW = APH) Oblong Anti-Pad DD APW Www.polarinstruments.com	Drill Diameter (t) Via Pitch (S) Anti-Pad Width (b) Anti-Pad Height (W') Dielectric Constant (Dkz) Dielectric Anisotropy (%)	DD 15.0000	
Please refer to the parameters in parentheses when reading <u>Application Note</u> Courtesy of Bert Simonovich, Lamsim Enterprises Inc Note: The model works for a simple differential pair structure with no pads and set there will not be sufficient excess capacitance from the planes so the accuracy w	Differential Impedance Effective Dielectric Constant veral planes throughout the fill suffer. When plage	Zdiff 84.88 DkEff 4.4430 ere is, say, only a 4 or 6 layer st ad like modern designs it will be	Enter via structure parameters by either keying the dimension values or use sliders to gauge the impact of
Calculation	results are presented here		varying each parameter

New Differential Via Calculation

New Differential Via Calculation

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1 / 9 | - 100% + | 🗊 🚸 AP8204.pdf ₽. ē A Practical Alternative to 3D Via Modeling You are a backplane designer and have been assigned to engineer a new high-speed, multi-gigabit serial link architecture from several line cards to multiple fabric switch cards across a backplane. These links must operate at 6GB/s day one and be 10GB/s (IEEE 802.3KR) ready for product evolution. The schedule is tight, and you need to come up with a backplane architecture to allow the rest of the program to progress on schedule. **HLD** Plan You come up with a concept you think will work, but the backplane is thick with over 30 layers. There are

You come up with a concept you think will work, but the backplane is thick with over 30 layers. There are some long traces over 30 inches and some short traces of less than 2 inches between card slots. There is strong pressure to reuse the same connector you used in your last design, but your gut tells you its design may not be good enough for this higher speed application.

Finally, you are worried about the size and design of the differential via footprint used for the backplane connectors because you know they can be devastating to the quality of the received signal. You want to maximize the routing channel through the connector field, which requires you to shrink the anti-pad dimensions, so the tracks will be covered by the reference planes, but you can't easily quantify the consequences on the via of doing so.

You have done all you can think of. based on experience. to make the vias as transparent as possible without

Si9000e v22.03 (March 2022)

New Surface Roughness Compensation Preset Values option

Polar Si9000 PCB Transmission Line Field Solver - [C:\Program Files (x86)\Polar\Si9000\Untitle								
File Edit Configuration Help								
	Parameters							
	Structures							
	Loss Budgets							
	Surface Roughness Compensation Preset Values							
Surface Mic	Hatch	Surface Roughness Compensation Preset \	/alues Configuration			×		
1B	Startup Mode	Surface Roughness compensation reserv	and configuration			^		
	Si Excel Interface	- Surface Roughness Compensation Preset Value:	s			1		
	Irack Resistance Calculator (IRC)		-		r			
Surface Mic	Graph Style	Description	BMS (μm)	Rz (μm)	Add Entry	Apply		
28	Solver Accuracy	Smooth Copper Laminate Side	2 2500	1,5000				
	Save Current Parameter Settings as Defaults	Smooth Conner Oxide Side	2 3500	1 6000	Delete Entry	Cancel		
	License Options	Bough Conner Laminate Side	8 2500	7,5000				
Coated Mic	Language Settings	Bough Copper Daile Side	5 2500	4,5000	Edit Entry			
			0.2000	4.0000				
	Add your comments here							
		1						
A new e	entry has been added to the							
Configu	ration menu to manage a tabl	le of						
Surface	Roughness Preset Values							
compos	red of Description PMS and /	or						
Device								
Rz valu	es							

New Surface Roughness Compensation Preset Values option

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New Surface Roughness Compensation Preset Values option

Surface Roughness Compensation - Huray		Select Surface Roughness Compensation Preset Values			×
Barren and Ba	atio of Areas	Surface Roughness Compensation Preset Values]
	Kaatiya Dall Dadiya (r	Description	RMS (μm)	Rz (μm)	Select
	riective ball nadius (j	Smooth Copper Laminate Side	2.2500	1.5000	Cancel
The Capponball Huray dialog has been	rea of Ball Count (sq	Rough Copper Laminate Side	2.3500	7.5000	
undated with the addition of '<<' ontions to	umber of Balls in Area	Rough Copper Oxide Side	5.2500	4.5000	
select the required Surface Roughness					
Preset Values					
Once chosen the roughness preset item					
Description and Rz value are passed back to					
the surface roughness dialog.					
Images by courtesy of Circuit Foil Law					
Cannonball-Huray Model	hable Cannonball-Hui				
Rz Matte	Matte-Side Houghness				
	Hz Matte (µm)				
Matte-side S	Smooth Copper Lamin	ate Side			
Drum side		- Calculate			
Rz Drum	Jrum-Side Roughness				
	Hz Drum (μm)	I.6000			
www.polarinstruments.com	Smooth Copper Oxide	Side			
Courtesy of Bert Simonovich, Lamsim Enterprises Inc Application Note					

Si9000e v22.02 (February 2022)

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Track Resistance Calculator (TRC Plus) enhancements

📕 Polar Si9000 PCB Transmission Line Field Solver - [C:\Program Files (x86)\Polar\Si9000\Untitled.Si9] [C:\Program Files (x86)\Polar\Si9000\Untitled.SIP] \times File Edit Configuration Help Parameter Entry Units 📥 🗛 🟓 2 🧝 Ê Mils C Inches Microns Millimetres Tolerance Minimum Maximum + - 1 Substrate 1 Height H1 2.5000 ÷ ± 0.0000 2.5000 2.5000 Calculate **Coated Microstrip 1B** Substrate 1 Dielectric Er1 4.2000 ÷ ± 0.0000 4.2000 4.2000 Calculate Surface Microstrip Lower Trace Width W1 1B 3.9752 ÷ ± 0.0000 3.9752 3.9752 CEr T1 Upper Trace Width W2 2.9752 ± ± 0.0000 2.9752 2.9752 Calculate The optional TRC Plus calculator Trace Thickness T1 0.7000 ± ± 0.0000 0.7000 0.7000 Calculate includes a number of Coating Above Substrate C1 1.0000 ÷ ± 0.0000 1.0000 1.0000 H1 Er1 Surface Microstrip 2B Coating Above Trace C2 1.0000 + ± 0.0000 1.0000 1.0000 enhancements including new Coating Dielectric CEr 4.2000 ± ± 0.0000 4.2000 4.2000 graphing capability. W1 www.polarinstruments.com Impedance Ζo 50.00 50.00 50.00 (Calculate) Coated Microstrip Selecting this toolbar option will Notes: (First 5 lines will print) More ... Interface Style Add your comments here pass the current structure C Standard Extended dimensions to the TRC Plus in My Name 1 G.S Convergence [Coated Microst. order to calculate the track Fine (Slower) resistance Coarse (Faster) Tolerance Mode Dual Coated Microstrip 1B Absolute Percentage (%) Parameter Snap Fred - IDual Auto Calc Coated Microst. Snap Embedded Microstrip 1B1A Embedded Microstrip 1B2A Lossless Calculation Frequency Dependent Calculation Sensitivity Analysis Single-Ended Structures

Track Resistance Calculator (TRC Plus) enhancements

Track Resistance Calculator (TRC Plus) enhancements

Si9000e v21.09 (Sept 2021)

Project Graphing – Introduction (requires the Si Projects feature)

It is often useful to compare the results from similar structures, especially with frequency dependent calculations where changing just one or two parameters can have significant impact.

Until now the Si9000e Quick Solver graphing has focused on a single structure, for instance the All Losses graph will display a single plot that includes multiple data series for the same structure.

The new Project Graphing option calculates all the results for a group of structures contained in the Project and then plots the selected data series (total attenuation, conductor loss or dielectric loss etc) on the same graph.

A single graph that combines results from multiple structures is useful in a number of ways. Comparing the impact of different dielectric materials, different roughness, sensitivity analysis for lossy calculations and many more uses.

Project Graphing

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Si9000e 2021 - 2023 Preview

Si9000e 2021 – 2023 Preview

Project Graphing – Summary

- The new Graphing option for Si Projects provides useful plots that contain data from multiple structures
- There are numerous uses for this type of option comparing the impact of different dielectric materials, different roughness, sensitivity analysis for lossy calculations and more
- 'What if' scenarios where one structure in the project would use the current design parameters and the second structure would contain a modified set based on a newer material. The plots comparing the original versus the new material will instantly show the impact
- Useful to both fabricators and design companies

(requires the Si Projects feature)

When using the Sensitivity Analysis option it is often useful to examine the calculated results in more details. It is now possible to auto-create a Project containing structures based upon the Sensitivity Analysis results data.

The following slides provide further details:

Si9000e 2021 – 2023 Preview

File Edit Configuration Help \frown \frown - 2 Substrate 1 Height H1 5.0000 H1=5.0000 W1=8.4360 Zo=49.99 Substrate 1 Dielectric Er1 4.2000 ÷ H1=3.0000 Lower Trace Width W1 W1=4.70.. 8.4360 **T1** CEr C1 Upper Trace Width W2 7.4360 🕂 Trace Thickness T1 1.2000 Coating Above Substrate C1 1.0000 ÷ H1 Er1 H1=4.0000 W1=6.56. Coating Above Trace C2 1.0000 **Coating Dielectric** CEr 4.2000 ÷ W1 www.polarinstruments.com Impedance Zo 49.99 Notes: (First 5 lines will print) Interface Style Add your comments here C Standard Extended H1=6.0000 W1=10.33.. G.S Convergence Fine (Slower) C Coarse (Faster) Tolerance Mode H1=7.0000 W1=12.25.. Absolute C Percentage (%) Parameter Snap H1=8.0000 Auto Calc W1=14.16.. Snap H1=9.0000 W1=16.09.. H1=10.0000 W1=18.03.. Lossless Calculation Frequency Dependent Calculation Project

📕 Polar Si9000 PCB Transmission Line Field Solver - [C:\Program Files (x86)\Polar\Si9000\Untitled.Si9] [C:\Program Files (x86)\Polar\Si9000\Untitled.SIP]

Save the newly created project to the Si Project file format (.SIP) so that it can be recalled at a later date.

- As separate structure in a Project it is now possible to examine the results in a lot more detail than when in sensitivity analysis
- Lossy calculations can be performed and compared
- As a Project the structure data can be stored as a .SIP file and recalled later
- Useful to both fabricators and design companies

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Surface Roughness Goal Seek option

📕 Surface Roughness Goal Seek	×
Step 1 : Enter Total Attenuation from measurement Freq (Hz) dB / LL Total Attenuation (S21 / SDD21) 2.50E+10 -1.2400	<u>Step 1</u> Key in or pick the total attenuation (S21 / SDD21) at a given frequency from the insertion loss measurement dat
Step 2 : Calculate Dielectric and Conductor Loss dB / LL Dielectric Loss Conductor Loss with Roughness (Total Attenuation - Dielectric Loss)	Step 2 Calculate the dielectric loss for the frequency entered from the current structure parameters. Subtracting this calculated dielectric loss from the total attenuation will leave the target conductor loss
Cannonball-Huray Rz (μm) 2.2729 Calculate >> Surface Roughness: 2.2729 Conductor Loss with Roughness: -0.6451 Setup Goal Seek Parameters Min Max < T1/2	 Step 3 Use the Si9000 Goal Seek algorithm to vary the surface roughness until it matches the required value to achieve the conductor loss as calculated in Step 2. In this example a Surface Roughness of 2.2729 μm is required

Surface Roughness Goal Seek option

Track Resistance Calculator (TRC Plus)

Track Resistance Calculator (TRC Plus)

1. Interactive track material image.

Clicking on a track parameter label will highlight the associated Track Dimension field (text box). Enter data into the active field.

Double-clicking anywhere on the image will bring up the Materials Editor.

2. Material selection and properties Select the material via the drop-down list.

Fields coloured in light-blue are not directly editable but the field values can be in the Materials Editor.

Fields coloured in light-green are editable by the user. For example, Operating Temperature will determine a material's resistivity at that temperature, which in turn will be applied in calculating the track resistance.

3. Units

Switch to your preferred units by clicking the associated option button – imperial units include Mils (Thou) and Inches; for metric units choose Microns (Micrometres) or Millimetres.

4. Track or trace dimensions

Enter or change track dimensions in the Track Dimensions in the chosen units.

5. Resistance result

Calculation of the track resistance. The result should update immediately upon any changes to the editable (light-green) fields.

6. Voltage Drop calculation result

The calculated Voltage Drop is displayed in the VD (Volts) text box

Other enhancements

- Monte Carlo Analysis. New option added to export the Iterations / Results to Clipboard (for Excel), accessible from the right-click menu
- Causally Extrapolated Substrate Data. New option added to export the Results to Clipboard (for Excel), accessible from the right-click menu

Si9000e v21.04 (April 2021)

Monte Carlo Analysis maximum iteration increased to 9000

Import from Atlas enhanced to support measurement data to 50GHz

Si9000e v21.01 (January 2021)

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Monte Carlo support added for Dual Coated structures

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Other enhancements

• FlexNet Publisher / FLEXIm v11.17.2.0 supported

Thank you for viewing this Si9000e 2021 – 2023 preview. If you have questions we would be delighted to help you. Your local contact information is contained on the following slide

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