IST Testing – Introductory FAQ's

1. What is IST Testing?

a. **IST is an accelerated stress test method used to evaluate the integrity of the Printed Wiring Board (PWB) interconnect structure.**
b. **IST stands for Interconnect Stress Testing.**
c. **IST creates a thermal cycle that stresses a specifically designed coupon, while simultaneously monitoring the plated through holes (PTH's) and internal interconnects (Post) electrical integrity.**
d. **A test that tests the PTH and the Post at the same time. A test method that measure the integrity of different areas of the same structure.**
e. **An objective test whose results are timely, repeatable, reproducible and unique.**
f. **IST stops the testing (stress) at exactly the time of failure (10%)**
g. **Testing temperatures can be raised to 260C (Lead Free)**
h. **IST automatically produces data that helps determine the PWB's ability to withstand the rigors of assembly, rework and the end use environment.**
i. **IST gives a critical evaluation of a boards quality and insight to the possible modes of failure.**
j. **IST is an IPC approved (TM-650 2.6.26) test method.**
k. **IST is rapidly growing acceptance by most major OEMs, CEM and PWB manufacturers as a definitive method for the measurement of PWB interconnect integrity.**

2. How Does IST testing work?

a. **IST works on the principle of a rapid thermal cycle between ambient (21^0C) and 150^0 C followed by forced air cooling back to ambient.**
b. **As the coupon thermal cycles, changes in circuit resistance are monitored. An increase of 10% is considered a failure and testing stops.**
c. **The Test Vehicle – the Coupon**
    i. **The test is dependant on the design of a coupon that reflects the boards attributes including critical hole size, copper weights, layer counts, interconnection types etc.**
    ii. **The coupon is designed with two discrete circuits, power and sense. The power circuit is used to heat the coupon and test post integrity. The sense circuit is measured to monitor resistance changes in the PTH or PTV (plated through via). The sense circuit does not receive significant power. On the power circuit there is no power applied to the central zone (middle portion) of the PTH or PTV.**

iii. **Ideally the total resistance of the coupon must fall within a range of 300 to 1000 micro-ohms. To achieve this requirement line width are defined by the test equipment needs. This requirement will permit testing of future products to achieve lead-free temperature extremes (235 C).**
iv. **There are a number of coupon designs available. PWB recommends the use of a generic design file that is flexible and useful in most applications. However there a number of existing designs that represent existing PWB strategies. Generic coupons have dual sense and dual power circuits allowing the greatest test flexibility.**
v. **There are a number specialized coupon designs available on PWBs, website for specific requirements.**
vi. **Custom designs can be developed for testing unique applications within the PWB.**

d. **The Test**
   i. **The power circuit generally heats the coupon to 150^0 using DC current. At the same time the resistance of the sense circuit is monitored.**
   ii. **The test is generally run until resistance in either circuit increases by greater than 10% or 1000 cycles are completed.**
   iii. **The sense circuit is designed to facilitate the measurement of low-level changes in resistance during thermal cycling.**
   iv. **A 10% increase in resistance is considered a failure and the test is stopped before too much damage is created, reducing the ability to detect root causes.**

e. **The Data**
   i. **The system displays the resistance activity graphs in real time, showing individual thermal cycles and accumulated cycle data.**
   ii. **Data analysis is simplified using automated graphing tools throughout each cycle. Additional data collection is completed on the upper stages of heating and the lower stages of cooling.**
   iii. **Data collected during the test includes the number of cycles to failure or finish, resistance of each circuit, resistance at both high and low temperature.**
   iv. **Evaluation of the data can indicate the mode of failure and the integrity of the circuit.**
   v. **The results are compared to historical (baseline) of similar products. This gives a quantification of how performance compares to an industry, customer, or internal requirement.**

3. Why do we perform IST?

a. **The main reason OEM, CEM and PWB fabricators are adopting IST, as the preferred method of PWB testing, is the savings in cost and time. IST costs less to complete accelerated stress testing, and, at the same time, is a more comprehensive test that is representative of the board reliability during assembly, rework, and the end use environments.**
b. **IST is an objective/comprehensive test method with repeatable and reproducible results.**
c. **IST tests hundreds of hole and interconnections so statistically the tests are more representative of the quality of the board.**
d. **IST testing stops before catastrophic failure and damage is created. This allows for thermal imaging to be used to find the failing area and permits a cross section evaluation of the exact failure location within the coupon.**
e. **Other Test method have significant limitation**
    i. **Cross section analysis is work intensive and requires skilled preparation and subjective evaluations. It is limited to random and not statistically relevant sample size.**
    ii. **Solder float tests are limit to evaluation for delamination and not representative of today's assembly environment. There is the burden of having to use toxic lead.**
    iii. **Thermal Cycling is more expensive and slower and does not allow the advantage of differentiating between PTH and post interconnect failures.**

4. What are the Benefits?

a. **Quick Time to Results –**
    i. **IST allows accelerated testing in a timeframe when the need to know is critical.**
    ii. **Faster than thermal cycling, (at least 6X faster than HATS)**
b. **IST removes ambiguity in results.**
c. **Results reflect the quality of hundreds of PTH and interconnections so the likelihood of finding random and latent quality issues is probable.**
d. **The test allows a much closer emulation the assembly, rework and end use environments, including the lead free temperature levels.**
e. **IST stops before catastrophic failure, so a critical evaluation of the underlying defect can be made.**
f. **The combination of IST and thermal imaging greatly improves the users ability to find and evaluate failure modes.**

5. What are the Applications for IST Testing

a. **Organizations**
    i. **OEMs – Impact studies, Vendor qualification and capability**
    ii. **CEMs – Impact of assembly and rework, vendor capability**
    iii. **PWB Fabricators – Baseline, Monitoring, troubleshooting**
    iv. **PWB Supply Industry – New product introduction, R & D**
b. **Time sensitive analysis – Quick comprehensive results in 4 days or less - Line Down, MRB, Trouble Shooting, Acceptance Testing**
c. **Quality Assurance/Quality Control, incoming, MRB, CAR systems.**
d. **Impact Studies – Assembly, rework, technology or design changes**
e. **New Technology Introduction**
f. **Product Integrity Studies**
g. **Product Baselining, capability and evaluation of design change.**
h. **Research and Development, DoE studies**
i. **Quality evaluations of product, process, vendors and suppliers.**
j. **Material or chemical characterization.**
k. **Prescreening and acceptance testing,**
l. **Vendor/Supplier evaluation, approval, qualification and monitoring.**
m. **Trouble shooting product or processes.**
n. **In-house quality evaluations, product and process monitoring.**
o. **Companies are using IST results to demonstrate their outstanding quality and reliability.**

6. What is the IST Process?

a. **Establish what are the objectives or needs for accelerated testing.**
    i. **Determine what information you would like to gather from the test. For example one may want to learn about the integrity of blind and buried vias and the impact of a new material, process or procedure.**
    ii. **Define a test plan that meets the requirements (we can help).**
    iii. **OEMs, CEMs, or vendors may have test plans available.**
b. **Establish the parameters that are to be tested.**
    i. **Characterize the PWBs for hole size, copper weight, dielectric thickness, material type, types of interconnections, etc.**
    ii. **In DOE exercises variables in process, procedures, or material may be tested.**
    iii. **Establish the type of PWB including interconnects (micro-vias, buried vias) non-sequential interconnects, buried capacitors or resistors etc.**
c. **Specify a Coupon – The Test Vehicle**
    i. **PWB Interconnect has generic coupons that would work for most application. The generic coupons are the most flexible adapting to most material requirements.**
    ii. **Decide on an existing coupon design or create a new coupon that reflects the attributes of product and process.**

Specify a Coupon – The Test Vehicle Con't.

iii. **The coupon must have resistances on the power circuit of 300 – 1000 micro-ohm.**
iv. **A Typical coupon will measure .75" X 6" and will fix on the edge of the panel.**
v. **Coupon designs are available on the PWB website at http://www.pwbcorp.com**
vi. **Plot the artwork and incorporate is into the photo-tools.**

d. **Manufacture the product with coupons**
   i. **Incorporate the coupons into the production panel artwork for fabrication.**
   ii. **Fabricate, remove and label coupons for testing.**
e. **Testing the coupon**
   i. **Preliminary Inspection – Assure continuity, visual inspection for obvious defects.**
   ii. **Prescreening – Measure the resistance and registration of each coupon.**
      1. **The coupon must be within the prescribe resistance values to be tested (300-1500 micro-ohms).**
      2. **The registration of inner layer pads to drilled holes is recorded.**
   iii. **Preconditioning (if requested) – The coupon is subjected to 230^0 C or 260C for 3 or 6 cycles. This thermal excursion simulates the assembly and rework processes (Lead Free).**
   iv. **Testing – Test the board, cycling the temperature between ambient and 150^0 C. The resistance of the power and sense circuits are constantly monitored until there is a 10% increase in the power of sense circuits or 1000 cycles which ever comes first**
f. **Evaluation and processing of data**
   i. **Gather and quantify the raw data**
   ii. **Perform thermal imaging and cross section of the failure sites as required.**
      1. **Power is applied to the failing circuit to create a warm spot.**
      2. **Thermo-graphic imaging is used to find an exact location of the failure site.**
      3. **Microsections are prepared for the examination of the failure location.**

g. **Reporting**
    i. **Based on collected data, cross-section evaluation and thermal imaging, a report is generated.**
    ii. **A report can be generated that contains raw data, graphs, and photographs.**
    iii. **Conclusion may be made based on this objective data being compared to established criteria or historical data. Conclusion can be made that give an indication of product quality, integrity and longevity.**

7. How Does One Start Using IST Testing

a. **Visit the web site at http://www.pwbcorp.com**
b. **Determine your needs, concerns and consideration**
c. **Call PWB Interconnect Solutions 613-596-4244**