PCB Layer Calculation and Documentation Tool

User Guide

Speedstack

PCB Stackup Design and Documentation

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Speedstack User Guide

POLAR INSTRUMENTS LTD

Speedstack specifications

Maximum layer count	128+
Via rules	Conventional, blind and buried
Materials library	Foils, Cores, RCC foils, Non-copper cores, Prepregs, Solder masks, Flexible cores, Bondply, Adhesive, Coverlays, Ident inks, Peelable masks
Post press compensation	Yes (user defined)
Finished thickness compensation	Copper coverage/simple percentage
Stackup calculation	Copper thickness, stackup thickness, dielectric thickness, solder mask thickness
Drill types	Mechanical, Laser, Laser stacked, Through plated
Drill-via fill types	Copper, Resin, Solder Mask, Non-Conductive, Conductive, Sintering Paste, Copper Paste
Back drill types	Back Drill Must Cut Layer No, Back Drill Must Not Cut Layer No, Back Drill Minimum Distance From Cut Layer, Back Drill Maximum Distance From Cut Layer, Primary Drill Size
Design rules check	Design logic, symmetry, copper balance, board thickness, manufacturing tests, resin starvation
Si8000m/Si9000e integration	Bi-directional copy/paste structure parameters
Flex-rigid modelling	Mesh/crosshatch ground plane modelling in conjunction with Polar Si8000m/Si9000e
Controlled impedance structures	100+ structures supported with impedance goal seeking and structure validation
Symmetrical stacks	Structure mirroring for symmetrical stacks
Loss/Frequency dependent modelling/graphing	Differential, Odd mode, Even mode graphed over a user-specifiable frequency range
Frequency dependent calculations (causal interpolation of dielectric constant)	Single frequency Er causal modelling using interpolation of Er v frequency employing Svensson-Djordjevic method
Result presentation	Length of line, Inches, Metres
Display series	All Losses, Impedance Magnitude, Inductance, Resistance, Capacitance, Conductance, Alpha, Beta
Surface roughness compensation	Smooth, Hammerstad, Groisse, Huray, Cannonball-Huray
Material library	On-line and on-premises
File import	IPC-2581 Rev B, Ucamco Job file, Ucamco Integr8tor and Ucam (.ssx), XML, Zuken CR-8000
File export	CGen Coupon Generator, CITS File, DXF, Gerber, Stackup Image (JPEG, BMP, TIFF), Cadence Allegro (IPC-2581 Rev B), CSV, IPC-2581 Rev B, Mentor Graphics, XML file, Zuken CR-8000, Zuken DFM Center, Ucamco Integr8tor and Ucam (.ssx),

Personal computer requirements

Computer	IBM PC compatible
Processor	Pentium 1GHz or better
Operating system	Windows 10 or later
Environment	Requires .NET Framework v2.0 or above
System memory required	2GB recommended
Hard disk space required	200MB (min.)
Video standard	FHD (1920 x 1080*) 2 FHD (1920 x 1080*) monitors recommended * Note: refers to *effective resolution* (some systems automatically apply scaling to render text readable – i.e. *effective resolution* refers to the screen resolution after scaling.)
Licensing	Electronic: local FlexNet license Fixed: Parallel/USB key Floating FlexNet license (Windows servers only)

Guide to the manual

Introduction	Introduces Polar Instruments Speedstack.
Getting started with Speedstack	Steps through the process of creating a simple stack from a set of manufacturer's data.
Configuring Speedstack	Setting up the Speedstack environment including license options, crosshatch and structure defaults, goal seeking parameters and file locations.
Using Speedstack	Discussion of the Speedstack user interface; creating and editing stackups.
	Using Virtual Material mode; using Material Library mode
Design rule checking	Using the Speedstack Design Rule Checker to correct stackup design errors.
Adding controlled impedance structures	Working with the Si8000m/Si9000e field solvers to add controlled impedance structures to the stackup model. Using the goal seeking facilities of the field solver to obtain the correct impedance for a structure.
Frequency dependent calculations (Speedstack Si)	Working with frequency dependent calculations to produce graphs and tables of insertion loss v frequency for each stack substrate.
	Using causal modelling
	Using surface roughness compensation
Si Projects	Working with Si Projects in Speedstack with Si8000m and Si9000e
CITS test files	Creating CITS test files for controlled impedance structures in the stack
Speedstack Flex	Working with flex-rigid stackups – using the Speedstack Flex navigator
Speedstack HDI	Working with HDI builds – sequential lamination
The Speedstack materials libraries	Using the Speedstack materials libraries, creating new libraries, adding material to the library. Accessing the online libraries
Printing stackup reports	Printing Speedstack technical reports; using the stack data tables, drill data tables, controlled impedance data tables, bill of materials tables and frequency dependent tables and loss graphs

Contents

Introduction to Speedstack

Speedstack PCB Stackup Builder

Polar Instruments Speedstack PCB Stackup Builder is designed to accelerate the PCB stack design process and deliver significant reductions in the amount of time consumed in PCB stackup documentation and control. Given designer specifications the PCB fabricator can use the Speedstack Stackup Builder to create in just a few steps the most cost effective stack for the range of available materials. Speedstack offers interconnect designers (PCB layout engineers), PCB front-end engineers and fabricators a fast and professional solution to layer stackup creation and documentation. Speedstack provides formal documentation for everyone involved in ensuring the correct materials are used in the build process.

Speedstack PCB

Speedstack PCB is a versatile PCB layer stackup design tool featuring powerful and easy to use graphical stackup editing capabilities. For PCB fabricators Speedstack PCB interfaces with the industry standard Polar Si8000m PCB Multiple Dielectric Controlled Impedance Field Solver.

Lossless calculations

It includes a link and license for the Si8000m, using the proven Si8000m to provide the impedance data for the stack. In addition, Speedstack PCB licence holders have full access to the stand alone Si8000m Quick Solver.

Speedstack PCB is especially tailored for PCB fabricators and PCB brokers – anyone with a requirement to design or communicate controlled impedance PCB stackups.

Speedstack PCB customers are able to share stackups and read impedance requirements from designers who are using Speedstack Si PCB Insertion Loss Field Solver.

Speedstack Si

For electronic engineers involved in stackup design Speedstack Si interfaces with the Polar Si9000e PCB Insertion Loss Field Solver. Both Speedstack Si and Speedstack PCB are able to directly output controlled impedance test files associated with each stackup. For the fabricator this is an ideal way to link the impedance test requirements to a particular job. For the OEM this offers a

clear method of sending impedance test specifications out to suppliers or brokers. Designers and fabricators can work together and select the best material combinations for minimising build costs. Fabricators can share their in house material libraries with OEMs and ensure the most effective material choice is employed in the build.

Frequency dependent calculations
Speedstack Si caters for frequency dependent calculations and adds comprehensive insertion loss calculation capability into Speedstack; insertion loss can be graphed over a user-specifiable frequency range. Frequency dependent structure properties allow for insertion loss calculation: trace conductivity, frequency range and result presentation mode. Loss results can be shown in dB/m, dB/inch or dB/LL (length of line.)

Causal modelling
Frequency dependent parameters include length of line, trace conductivity, dielectric constant and loss tangent, frequencies of interest and causal extrapolation points for each substrate and also support amalgamated dielectric structures. Frequency dependent calculations employ causal interpolation of dielectric constant using Svensson-Djordjevic modelling. Library materials tables include dielectric constant and loss tangent fields and substrate causal extrapolation reference points values may be set either manually or automatically from the library (virtual material mode supports loss tangent in laminates and soldermask.)

Surface roughness modelling
Speedstack includes surface roughness compensation in frequency dependent calculations, supporting Hammerstad, Groisse and Cannonball-Huray surface roughness modeling methods.

Bidirectional copy and paste between Speedstack and the Si9000e transmission line field solver allows for quick transfer of structure parameters.

Technical reports optionally include insertion loss graphs for user-nominated structures.

Speedstack Flex

Speedstack Flex allows OEM designers to create accurate and efficient flex-rigid PCB stackups in just a few minutes, with error-free documentation for tighter control over the finished board. For PCB fabricators, Speedstack Flex provides the flexibility to quickly calculate the impact of substituting alternative materials to improve manufacturability and reduce cost while maintaining the specified parameters

and performance of the board. Speedstack Flex can be used in conjunction with the Si8000m and Si9000e field solvers when modelling and documenting mesh/crosshatch ground. Structure data and mesh geometry can be readily shared between Speedstack and the field solvers. The Navigator provides a clear contextual view of the rigid and flexible stacks within a flex-rigid build and allows easy alignment of displayed materials between stacks. The associated technical report also supports different materials on the same dielectric layer, improving the clarity of documentation between the stackup designer and fabricator.

Speedstack HDI

Speedstack's Navigator quickly guides you through the sequential sub-stack lamination sequence and presents the complete assembly in a parsed graphical display that shows each phase of the multi-step lamination sequence of an HDI PCB. There is no limit to the number of press cycles that can be documented.

Resin check / excess resin algorithms determine the order in which the materials are pressed together and return useful resin percentage information that can be used to determine potential de-lamination problems.

User-definable settings within the navigator allow engineers to display layers in transparent, invisible or 3D mode. Speedstack HDI makes re-ordering and renaming sub-stacks quick and easy with the Navigator. This is especially useful for HDI constructions.

Rapid stackup creation

Users may specify the stackup semi-automatically with the powerful Stackup Wizard or alternatively build the stack manually, layer by layer. Speedstack is flexible and allows full manual editing of stacks created by the Stackup Wizard.

Easy stackup editing

The Speedstack allows the user to view stackup in 2D or 3D format. Layer and material annotation is clear and easy to read and each layer may be selected and queried to display the associated material type and properties, including the associated data file. Visible drill information ensures that designers instantly know which layers support conventional, blind and buried vias.

Speedstack allows you rapidly to build and share stacks and verify via aspect ratios and track spacing rules. The stack file contains base material information combined with layer description and a complete listing of transmission line structures deployed in the stack. Keeping all stack

information in one file ensures that manufacturing data is accurately shared between original designer and fabricator.

Speedstack's Stack Editor provides efficient and time-saving features such as Copy/Paste Material properties so the stack designer can copy all properties from a selected material and then paste user-selectable property groups to other materials.

Speedstack allows the designer to retain and re-allocate structures when changes are made to the electrical layers of the stackup. This enables reallocation of structures after the following stackup changes:

Adding and deleting foils and/or cores – increasing or reducing the layer count

Moving foils and cores – maintaining the layer count

Exchanging two different thickness cores within the stack

Copying and pasting foils or cores – increasing the layer count

High quality documentation and file format

Speedstack saves the stack in efficient electronic format and outputs stack graphics in a variety of formats to suit your requirements. Stack data may be output in GERBER, DXF, BMP, JPEG, TIFF and XML. In addition, the stack data can be exported in comma-separated form for inclusion in other systems. Speedstack's high quality customisable printouts make it easy to discuss alternate builds and pricing impacts with fabricators.

Applications engineers, front end and production engineers benefit from receiving stack information in an intuitive, easy to understand format. The Speedstack .sci file contains full details of the layer stackup of a particular job. If changes are necessary or preferred stacks are to be shared with customers, Speedstack can cut the time for documentation and information sharing to a fraction of the time taken when employing traditional methods such as spreadsheet, word processor or presentation software.

Integration with the Si8000m/Si9000e

Speedstack is fully integrated with the Polar Si8000m Controlled Impedance and the Si9000e PCB Transmission Line Field Solvers so the user can quickly add controlled impedance structures to layers in the stackup. The designer or board fabricator can use the Goal Seek facility of the Si8000m/Si9000e field solvers to arrive rapidly at the controlled impedance structure parameters to produce the target impedance.

Materials library

The Speedstack supports a flexible materials library. This allows the designer to use standard materials data and also provides the facility to create new material libraries. PCB fabricators can also build libraries of commonly stocked materials to give interconnect designers visibility of the materials held in stock. Speedstack thus supports three types of library – custom user libraries of materials, generic designer libraries of materials of given dielectric characteristics (for example, thicknesses) along with a comprehensive set of materials libraries from PCB base material suppliers who are members of the Polar Speedstack Material Partner program.

Online / on-premise materials libraries

The Speedstack Material Library includes an online library to allow users to download material library MLBX files from the Polar website. The online material libraries feature provides the user with a list of available library files; on selection the file is downloaded and is either appended to the existing data or replaces the existing data.

Speedstack also includes an on-premise option to allow for users who cannot connect to the online library due to network security restrictions

Speedstack's Virtual Material mode

Speedstack provides *Virtual Material* mode allowing you to build and experiment with stackups (for example to examine the effects on impedance structures of different trace widths or dielectric heights) without requiring real materials to be entered into a materials library.

In Virtual Material mode you will use the Stackup Wizard to enter a few details about the stack, the number of layers, overall board thickness, plane and mixed layers, etc., along with solder mask and copper thickness and build type (foil, core or HDI.) and drills Speedstack will then build a stack to the specified board thickness by equally distributing the dielectric regions. If a preferred core thickness is specified the software will maintain the dielectric thickness for core regions but then equally distribute prepreg regions to reach the target board thickness.

Preferred builds

PCB fabricators are able to create and share preferred builds and exchange the associated information with designers. Build data also includes blind and buried via specification. This simplifies the task of sharing stackup and drilling information between board shops and the design community.

Dimensional information

Finished board thickness is a critical dimension in many applications; Speedstack keeps track of the finished PCB thickness and tolerance and allows fabricators the flexibility of adding in-house post-press thickness for prepreg layers. Additionally, Speedstack takes into account plating thickness where appropriate.

High layer count boards

On boards with high layer counts it can be very easy to make a change that would produce a non-symmetrical stack. The Speedstack Design Rules Check monitors symmetry across the stack, and ensures that material symmetry is maintained. Speedstack also makes it easy to set the symmetrical build mode to ensure that any changes you make are applied equally across the stack.

Supplier management

When multiple-sourcing PCBs or when moving from prototype to volume production, the stack and fabrication design rule checks ensure that the manufacturing capabilities of your chosen suppliers are not overlooked. In addition the professional documentation output ensures that layer stack information is accurately conveyed to PCB suppliers.

Graphical interface

Speedstack offers an easy to interpret graphical interface. Clearly showing the layers supporting blind and buried vias, Speedstack also records the data file for each layer (including ident and peelable mask layers). The graphical interface is especially designed to simplify the process of communication between interconnect designer and fabricator. OEMs who need to manage boards sourced from multiple suppliers will also find this facility invaluable. In addition to physical layers Speedstack adds mask and notation for electrical layers.

Interfacing with other systems

Speedstack is able to load an XML file on launch. If an XML file (.stkx) filename parameter is specified on the command line it will import this file into Speedstack.

Speedstack can call an external program / utility / script via the External Utilities menu options. The menu items are configured within the Configuration option.

Importing and exporting stackup information

IPC-2581 Rev B

Speedstack incorporates Import from and Export to IPC-2581 Rev B option with interactive interface, supporting stack up material and structure information

Ucamco

Speedstack incorporates the facility to read in files in XML format and Ucamco Job File format, providing comprehensive integration with Ucamco and will import files from and export to both Ucam and Integr8tor.

Zuken

Speedstack integrates directly with the Zuken CR-8000 Design Force and Zuken Design Force DFM Center PCB manufacturing pre-processing and CAM system, simplifying material communication in the supply chain. Designers can define layers in DFM Center then export to Speedstack to define materials and provide a fully documented stackup in a format widely recognised by both PCB supply chain managers and fabricators.

Stacks may be exported to the Polar CGen Coupon Generator for subsequent processing into test coupons.

The Export CITS File option will create test files for Polar CITS controlled impedance test systems.

Speedstack can generate printed output in DXF, Gerber, CSV and XML, as well as graphic image formats JPEG, BMP and TIFF.

Export options also include Cadence Allegro, CSV, IPC-2581 Rev B and Mentor Graphics.

Import / export XML file formats support frequency dependent structure properties.

Converting imported electrical layers to cores

When importing stackup data from some CAD / CAM systems only the electrical layers are defined, so copper layers may appear adjacent each other. Speedstack allows conversion of two adjacent electrical layers into core or flexible core materials using the Convert to Core function.

Structure net classes

Speedstack is able to import and store up to five net class names with each structure. These net class names provide a link to the matching impedance nets inside the ECAD PCB layout system.

Installing Speedstack

Installing and activating Speedstack

It will be necessary to install and activate the product license and set operating options prior to building stacks or performing calculations with Speedstack. See *Configuring Speedstack*|*Licensing* to select the associated field solver and purchased options.

Obtaining a Speedstack license

Speedstack is license using the FlexNet Publisher licensing service. Contact Polarcare@polarinstruments.com for installation/activation directions.

Download the software from the supplied link. Unpack and save the installation file to a suitable folder then run Setup.

Uninstalling the software

Caution: Prior to uninstalling, make a copy of the Speedstack folder structure and data files and store in a safe place.

To uninstall the Speedstack software:

Windows 7/8/10

Choose Settings|Control Panel; select Programs and Features and right click Speedstack and choose Uninstall.

Getting started with Speedstack

Online tutorial guides

Polar's web site provides online downloadable quick start and version specific user guides to familiarize users with the operation and features of the software.

From the Help menu choose Speedstack Help to download the Getting Started guide, along with tutorials for stack editing, managing materials libraries, manufacturing constraints and controlled impedance structures:

https://www.polarinstruments.com/help/speedstack/tutorials/

Download the user guide for your Speedstack version:

https://www.polarinstruments.com/help/speedstack/Nrmstart.htm

Stackup Templates

Polar's web site provides online downloadable prebuilt sample templates and associated technical reports (suitable for Speedstack 2019 or higher) to familiarize users with the operation and features of the software.

https://www.polarinstruments.com/support/stackup/templates.html

The stackup templates listed include materials and drills are typical of standard stacks used in PCB construction and can be used as a starting point when building your own stacks. Stackup samples include core and foil build models in both material library and virtual library modes (see *Creating and editing stackups*) for rigid stackups, flex-rigid stackups and multiple press cycle HDI stackups.

Click on the link to the stackup template page and download the Speedstack template project (.sci) file; save to a convenient location and the use the Open Project command in Speedstack to view and edit the stackup. Note that the sample stackups are shown with dimensions in microns.

Using Speedstack Stackup Builder

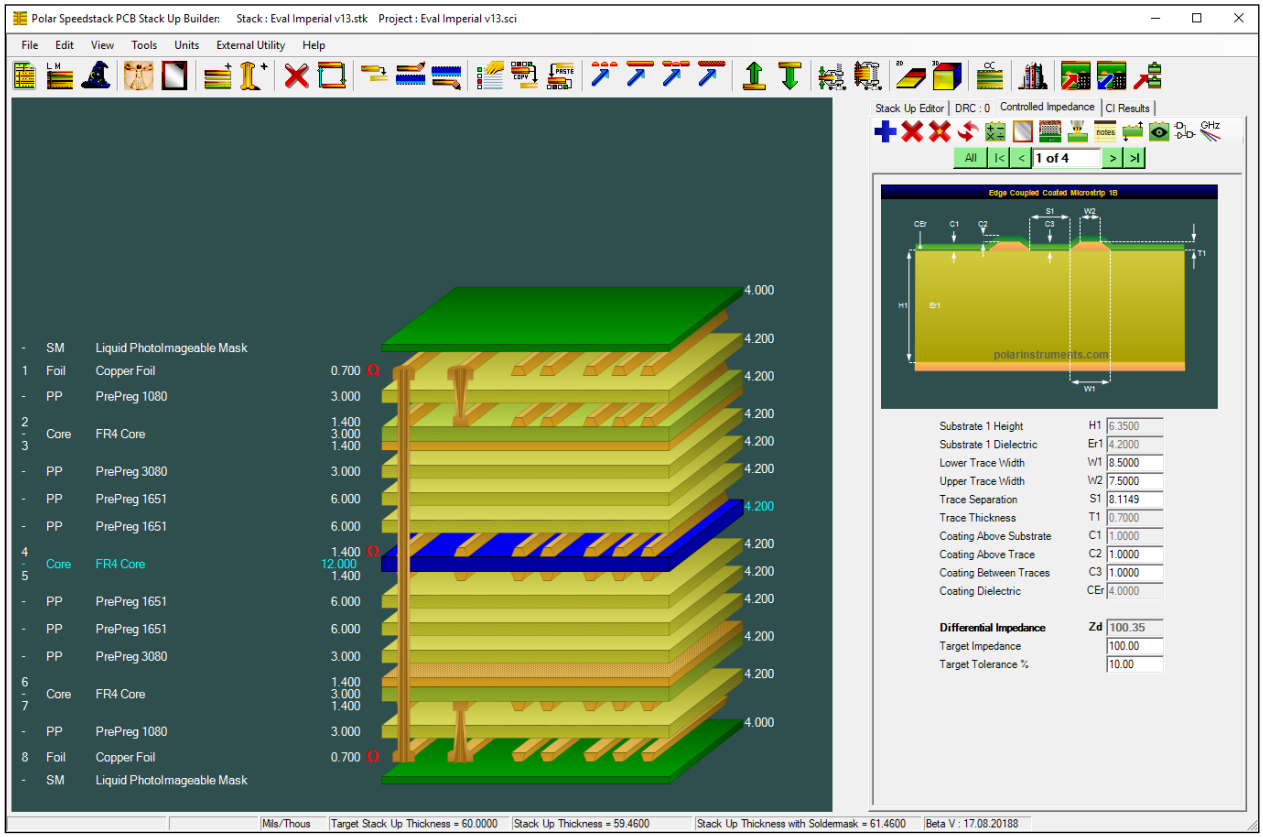
Speedstack Stackup Builder

Double-click the Speedstack icon to start the Speedstack program and display the Stack Editor.

The Stack Editor

The Stack Editor screen displays all details of the stack, including copper and prepreg materials, solder masks and ident layers, drilling information, controlled impedance structures and design rule check results.

Controlled impedance structure data may be transferred between Speedstack and the associated Polar Si8000m or Si9000e field solver to goal seek for the target structure dimensions.



The Stack Editor screen

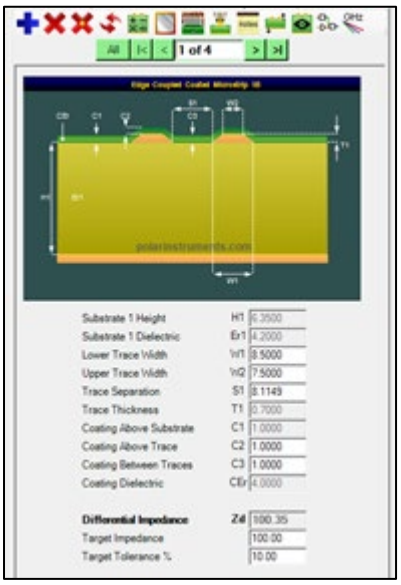
The Speedstack Stack Up Editor screen comprises:

- The Menu bar — drop-down context sensitive menus containing all the Speedstack Editor commands
- The Tool bar — incorporating short cut tool buttons to the most common menu commands

- The Stackup Build and Construction Window — where the board stackup is built and edited
- The Controlled Impedance window displaying the controlled impedance structures (if any) for the selected layer.
- Stack Up Editor/Notes tab— a free form text area for explanatory or commentary notes
- Design Rules Check (DRC) tab — allows design rules and manufacturing constraints to be specified and violations displayed
- Stack Up Information properties area — table containing information related to the whole stackup
- Selected Item Information area — properties table containing the attributes of the layer currently selected in the stackup
- The Controlled Impedance Results tab – summarizing the controlled impedance structures within the stack

Controlled Impedance window

The Controlled Impedance window displays all the controlled impedance structures and associated parameters for the selected layer.

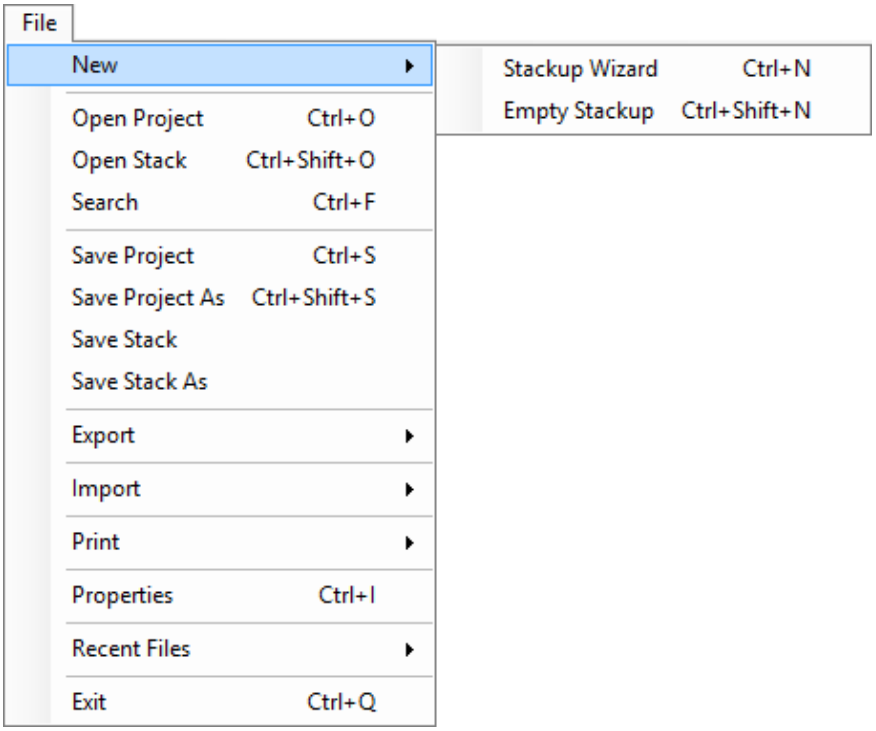


Step through the structures with the structure browse control – structures with the impedance within tolerance are shown in green, structures where the impedance is outside the specified tolerance range are shown in red.

The Speedstack menu system

The File menu

The File menu allows for creation of new stackups and projects and opening, saving, printing, importing and exporting existing stackups and projects and data files from companies providing data exchange with Speedstack.



Opening projects

Stackups that incorporate controlled impedance structures are saved as projects. Click Open Project and navigate to the project folder; projects are saved as .sci files. The stackup along with all its design rule checking settings and controlled impedance information is loaded.

Saving stackups

Click the Save button to save the stackup. Users are recommended to save the stackup frequently during the stackup creation process to avoid data loss; stackups are saved as .stk files.

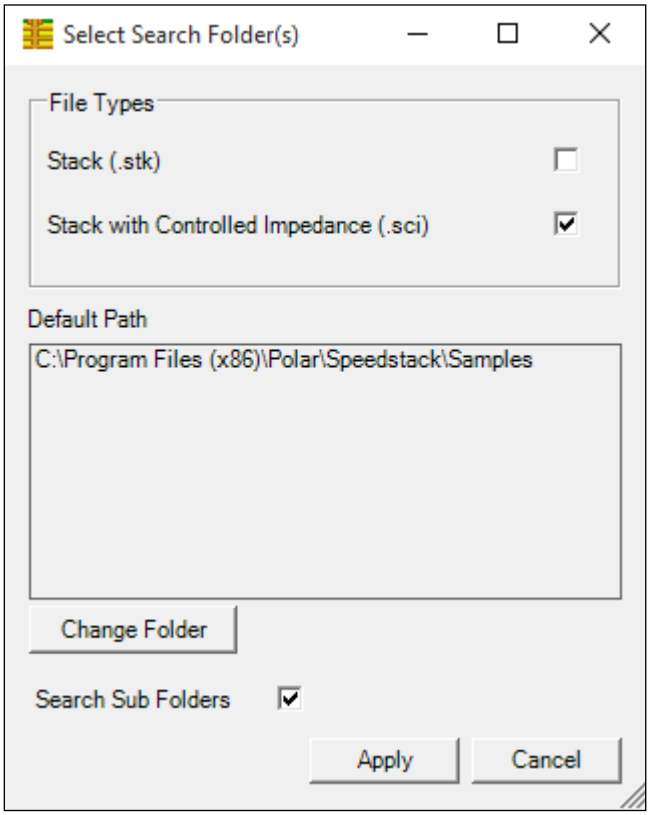
Saving projects

Use the Save Projects command to save a stackup and its controlled impedance structures.

Searching for stackups and project files

When creating new stackups and projects it will often be found convenient and timesaving to reuse an existing stack or project, modifying as required and the saving as a new

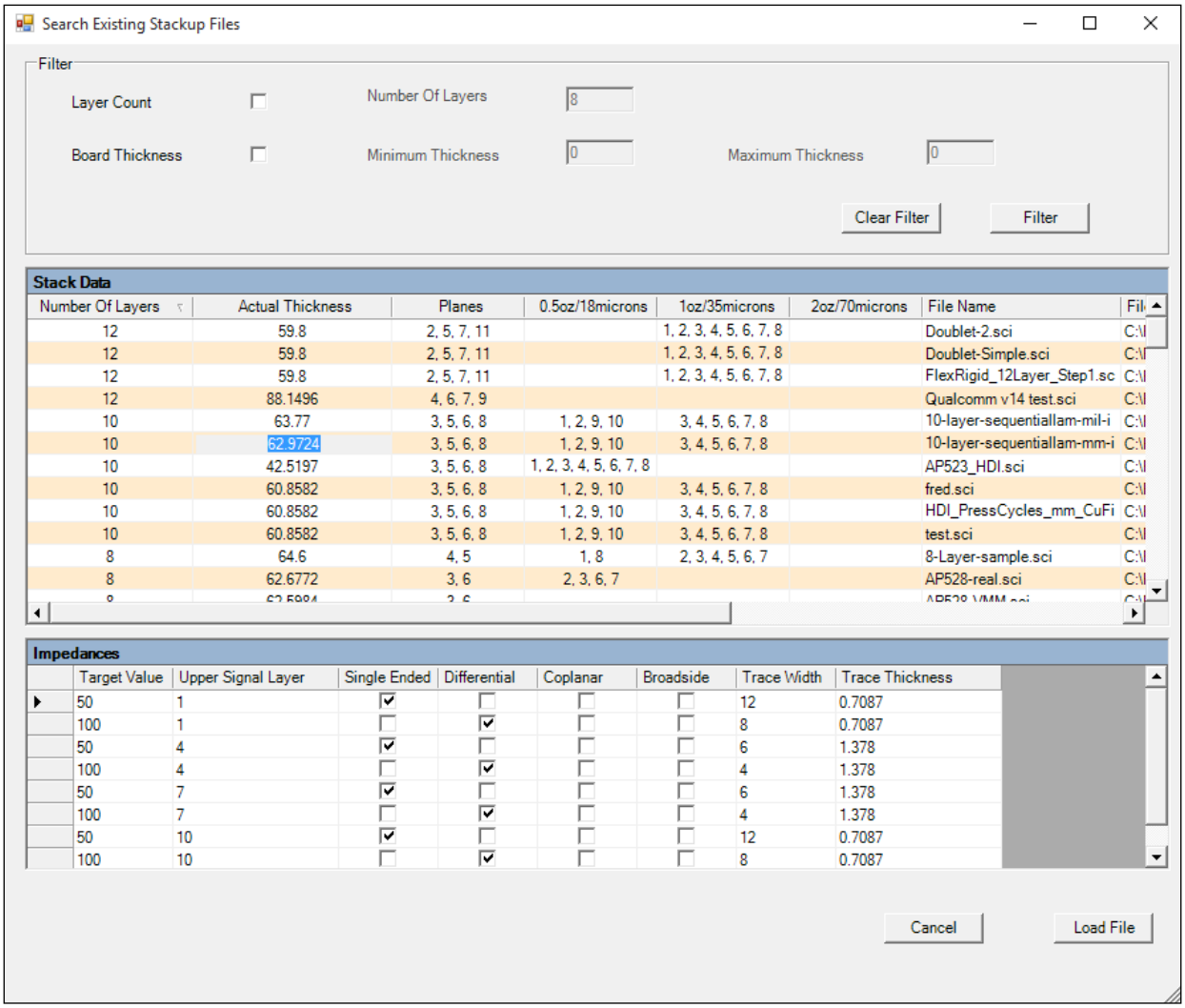
stack or project. From the File menu choose Search and click Change Folder to navigate to the collection of stacks.



Choose from stacks and/or projects (stacks with controlled impedance;) with the folder chosen, click Apply.

Supplying search criteria

The stackups and projects within the chosen folder structure are displayed. If appropriate supply criteria, layer count, board thickness, etc. and click Filter.



Step through the list, choose the matching stack or project and click Load File.

Importing Stackup information

Speedstack incorporates the facility to read in files in:

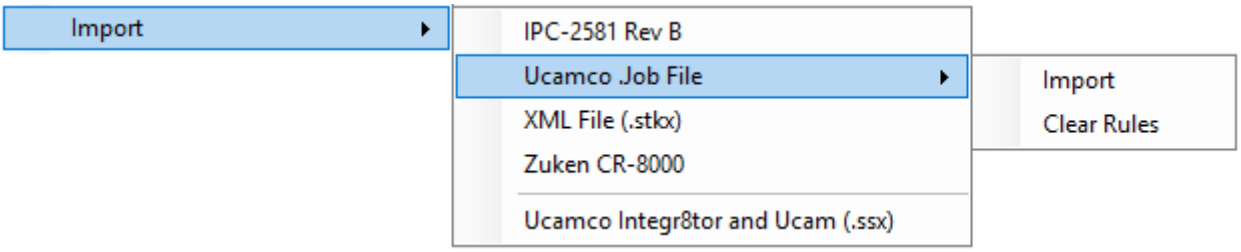
IPC-2581 Rev B format

Ucamco Job File format

XML format

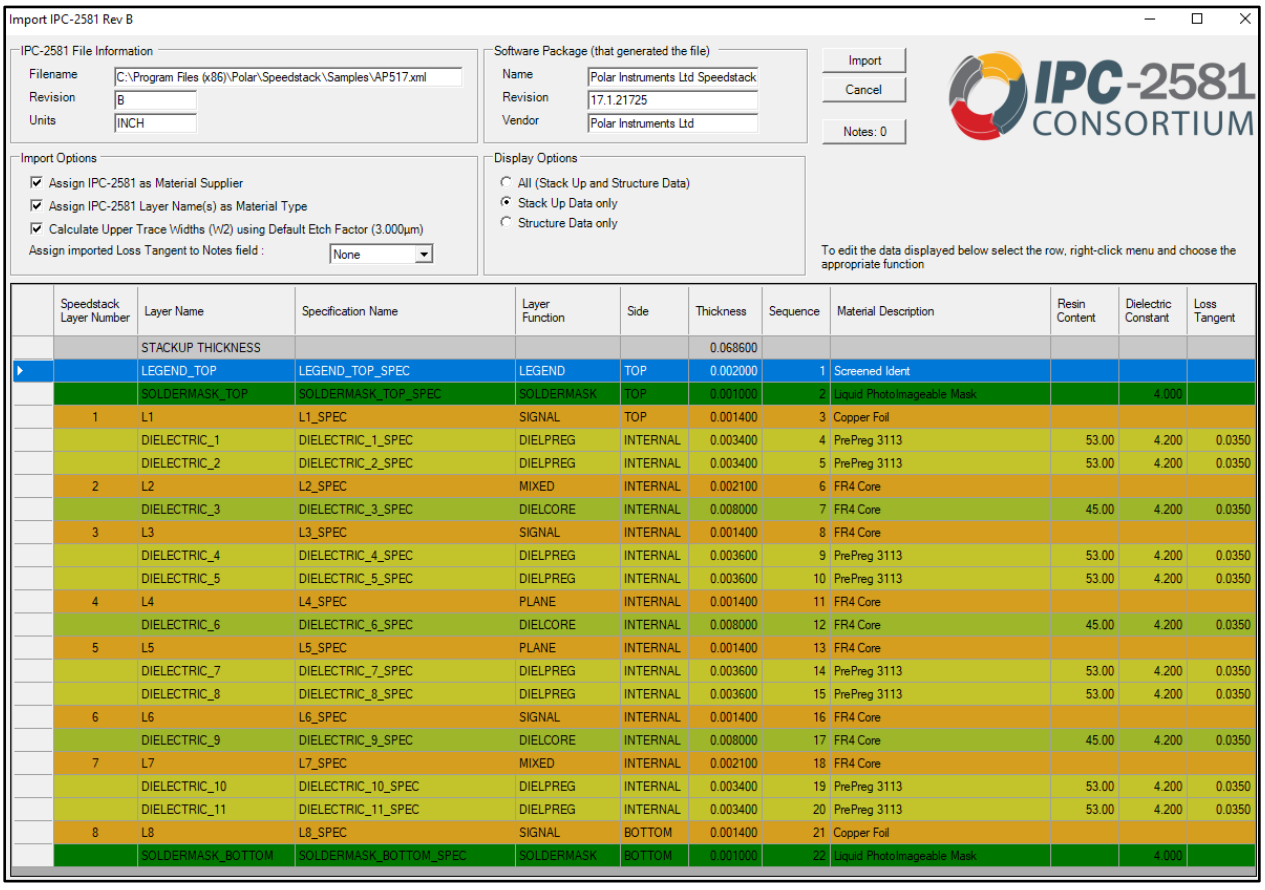
Zuken CR-8000 format

Ucamco Integr8tor and Ucam format



IPC-2581 Rev B

Speedstack can import stack up and impedance structure data using the IPC-2581 Rev B XML file format. Use the IPC-2581 Rev B command to import IPC-2581 Rev B (XML) files using the interactive interface. The stack shown below displays both stackup material and structure information. The foil, prepreg, core and solder mask material data grid colours are determined by the Speedstack Configuration,



Speedstack Layer Number	Layer Name	Specification Name	Layer Function	Side	Thickness	Sequence	Material Description	Resin Content	Dielectric Constant	Loss Tangent
	STACKUP THICKNESS				0.068600					
	LEGEND_TOP	LEGEND_TOP_SPEC	LEGEND	TOP	0.002000	1	Screened Ident			
	SOLDERMASK_TOP	SOLDERMASK_TOP_SPEC	SOLDERMASK	TOP	0.001000	2	Liquid PhotoImageable Mask		4.000	
1	L1	L1_SPEC	SIGNAL	TOP	0.001400	3	Copper Foil			
	DIELECTRIC_1	DIELECTRIC_1_SPEC	DIELPREG	INTERNAL	0.003400	4	PrePreg 3113	53.00	4.200	0.0350
	DIELECTRIC_2	DIELECTRIC_2_SPEC	DIELPREG	INTERNAL	0.003400	5	PrePreg 3113	53.00	4.200	0.0350
2	L2	L2_SPEC	MIXED	INTERNAL	0.002100	6	FR4 Core			
	DIELECTRIC_3	DIELECTRIC_3_SPEC	DIELCORE	INTERNAL	0.008000	7	FR4 Core	45.00	4.200	0.0350
3	L3	L3_SPEC	SIGNAL	INTERNAL	0.001400	8	FR4 Core			
	DIELECTRIC_4	DIELECTRIC_4_SPEC	DIELPREG	INTERNAL	0.003600	9	PrePreg 3113	53.00	4.200	0.0350
	DIELECTRIC_5	DIELECTRIC_5_SPEC	DIELPREG	INTERNAL	0.003600	10	PrePreg 3113	53.00	4.200	0.0350
4	L4	L4_SPEC	PLANE	INTERNAL	0.001400	11	FR4 Core			
	DIELECTRIC_6	DIELECTRIC_6_SPEC	DIELCORE	INTERNAL	0.008000	12	FR4 Core	45.00	4.200	0.0350
5	L5	L5_SPEC	PLANE	INTERNAL	0.001400	13	FR4 Core			
	DIELECTRIC_7	DIELECTRIC_7_SPEC	DIELPREG	INTERNAL	0.003600	14	PrePreg 3113	53.00	4.200	0.0350
	DIELECTRIC_8	DIELECTRIC_8_SPEC	DIELPREG	INTERNAL	0.003600	15	PrePreg 3113	53.00	4.200	0.0350
6	L6	L6_SPEC	SIGNAL	INTERNAL	0.001400	16	FR4 Core			
	DIELECTRIC_9	DIELECTRIC_9_SPEC	DIELCORE	INTERNAL	0.008000	17	FR4 Core	45.00	4.200	0.0350
7	L7	L7_SPEC	MIXED	INTERNAL	0.002100	18	FR4 Core			
	DIELECTRIC_10	DIELECTRIC_10_SPEC	DIELPREG	INTERNAL	0.003400	19	PrePreg 3113	53.00	4.200	0.0350
	DIELECTRIC_11	DIELECTRIC_11_SPEC	DIELPREG	INTERNAL	0.003400	20	PrePreg 3113	53.00	4.200	0.0350
8	L8	L8_SPEC	SIGNAL	BOTTOM	0.001400	21	Copper Foil			
	SOLDERMASK_BOTTOM	SOLDERMASK_BOTTOM_SPEC	SOLDERMASK	BOTTOM	0.001000	22	Liquid PhotoImageable Mask		4.000	

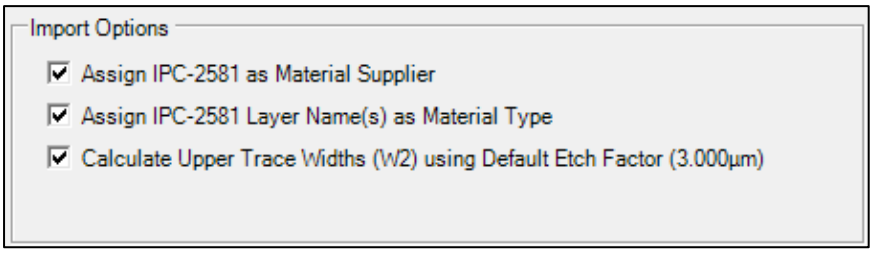
The dialog above provides user guidance through the import process.

The IPC-2581 File Information pane displays useful file data including the file name, revision and units. IPC-2581 supports inches, millimetres and microns.

The Software Package pane details the application (including the revision and vendor) that generated the IPC-2581 file.

Setting import options

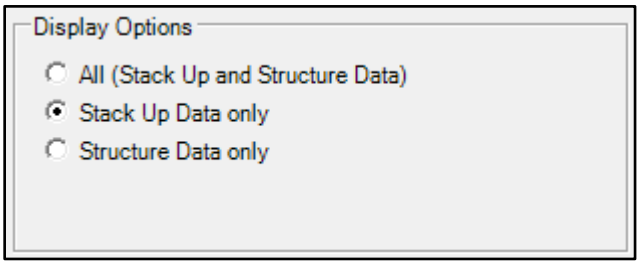
Set the import options to control how the IPC-2581 data is allocated in Speedstack:



The material type can optionally be derived from the layer name and the upper trace width can be derived from the given trace width and default etch factor.

Setting display options

From the Display Options dialog pane choose to display all data or stackup or structure data only



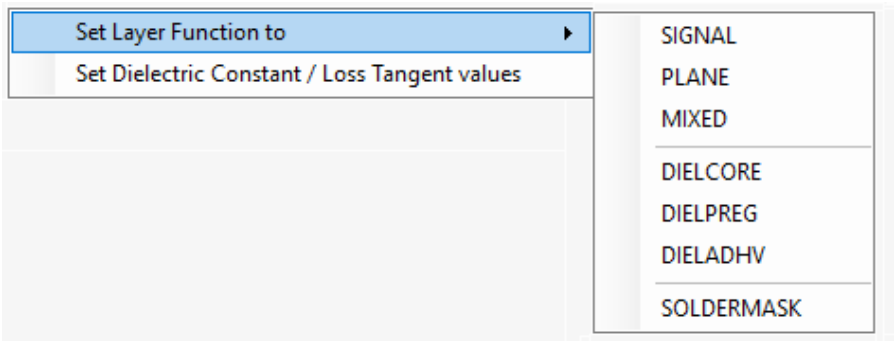
Sorting layer information

The stackup imported from the IPC-2581 file is shown in data grid form. Data can be sorted by column – click on each column header to sort in ascending or descending order by sequence, layer number, layer name, etc.

Assigning layer functions

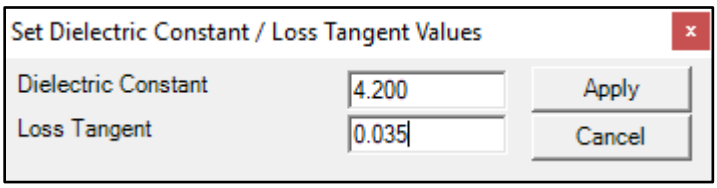
During the import process it may be necessary to consult the board authority or design documentation to ascertain the function of each layer, signal, plane, dielectric, core, etc.; the Layer Function determines the layer / material type.

Right click each layer and use the Set Layer Function to assign the layer its designated function.

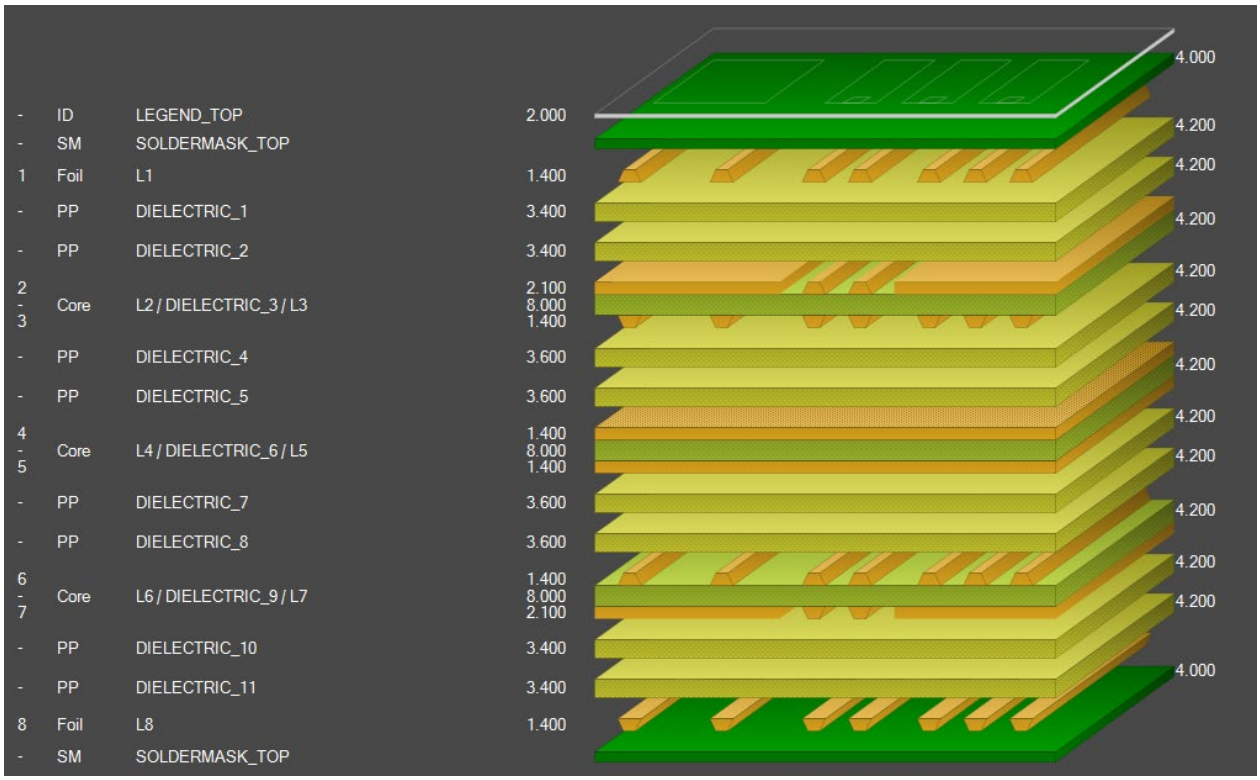


Setting loss values

Dielectric constant and loss tangent values can be set for each layer; select the layer (it will highlight in blue) and then right click the layer, the dialog should show the current values; enter each value and click Apply.



With all the editing completed, click Import to bring the file into the Speedstack Editor.



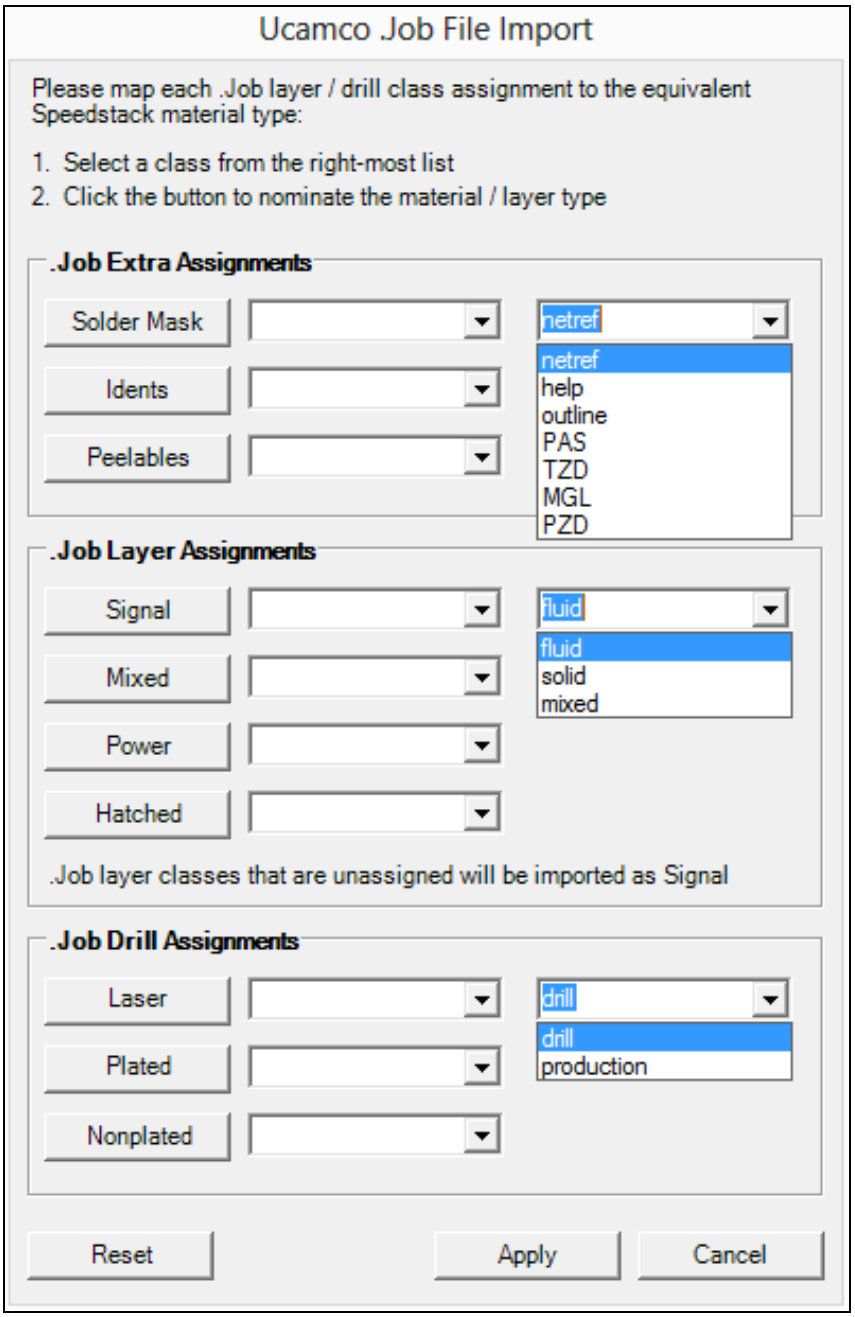
The imported stack can be processed using the Speedstack editing functions.

Ucamco Job Files

The .Job file format contains a varying amount of stackup information depending upon the how the system has been configured by the Ucam user.

Speedstack will import files from both Ucam and Integr8tor.

Choose File|Import|Ucamco Job File|Import and select the .job file and click Open. The Ucamco .Job File Import dialog is displayed:



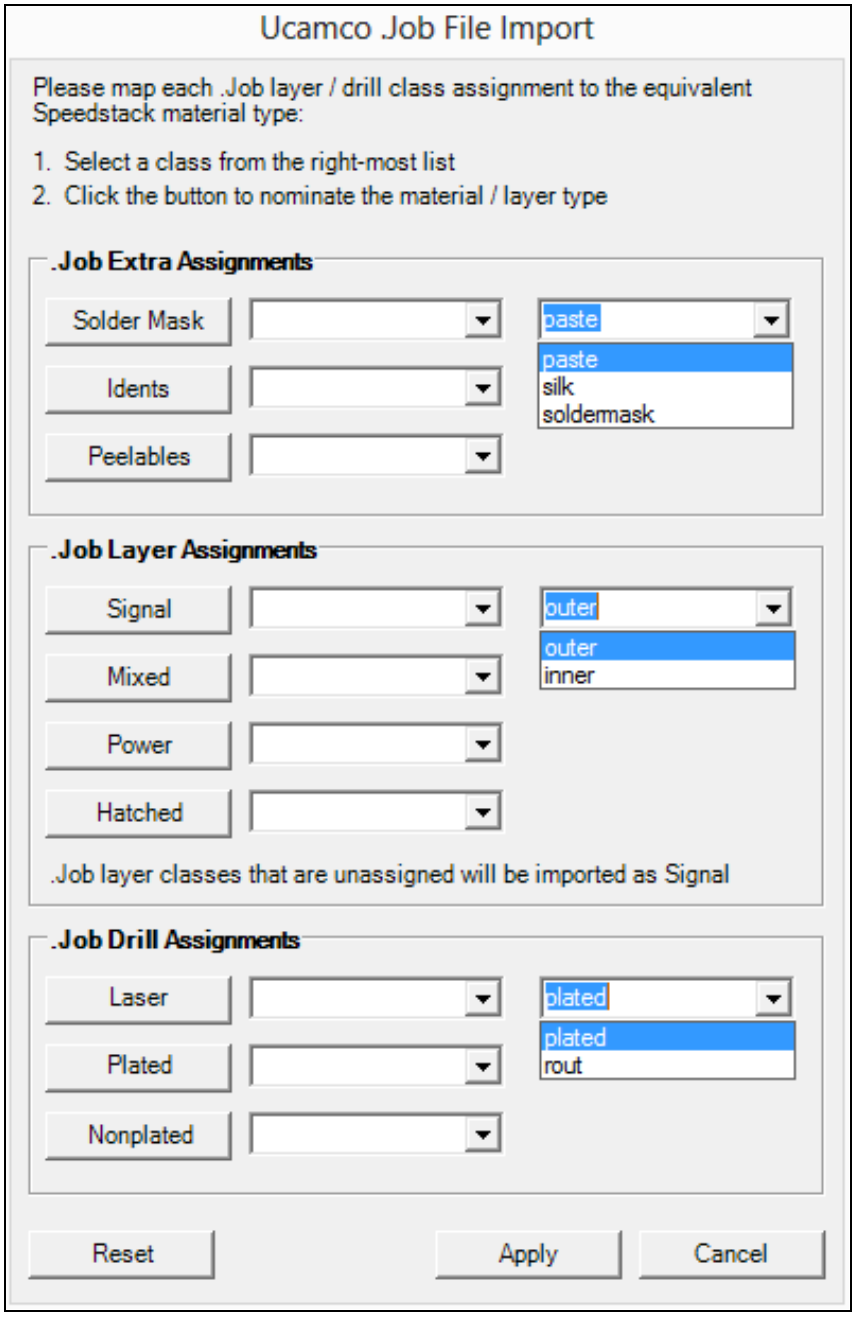
The .Job file contains user-definable material / drill class definitions so it will be necessary to map these definitions to the various Speedstack material and drill types.

To apply assignments select the class from the drop down list then click the associated button to nominate the material or layer type. Click Apply.

Note: Where stack data are not included in the .job file it will be necessary to include or update properties (for example, solder mask properties such as thickness and dielectric constant) before adding impedance structures.

Integr8torJob files

When Integr8tor files are imported the Ucamco .Job File Import dialog is displayed as shown below.



Select the assignment options as described above and click Apply. Click Reset to clear the assignments.

Clear Rules

The Clear Rules command will delete all previously learned rules.

XML files
Choose File|Import|XML File (.stkx), select the .stkx file for import and click Open.

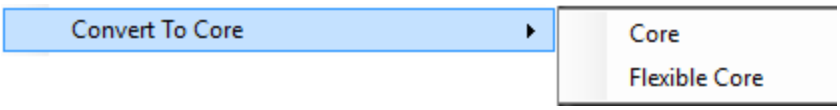
Zuken CR-8000
Choose File|Import|Zuken CR-8000 format, select the .stkx file for import and click Open.

Ucamco Integr8tor and Ucam format (.ssx)
Choose File|Import|Ucamco Integr8tor and Ucam format, select the .ssx file for import and click Open.

Converting imported electrical layers to cores

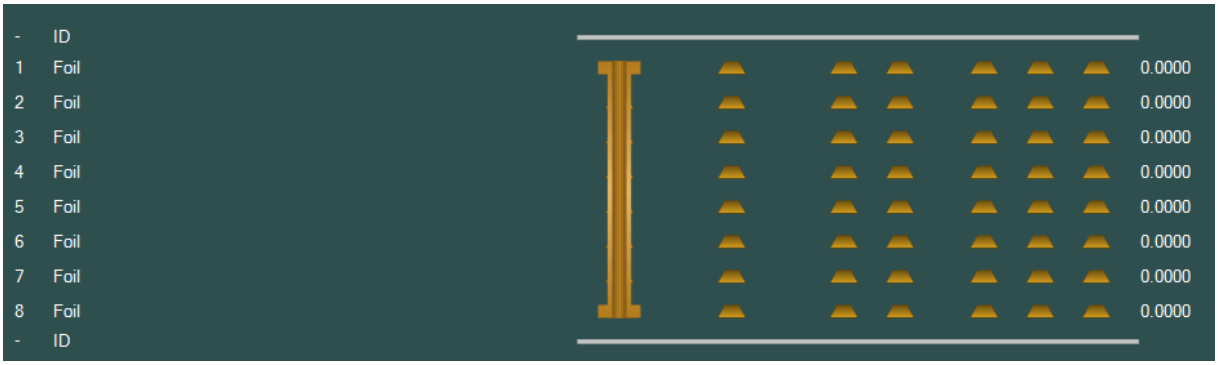
When importing stack up data from some CAD / CAM systems only the electrical layers are defined. In this case copper layers may appear adjacent each other in the Stackup Editor. Speedstack allows the user to quickly convert two adjacent electrical layers into Core or Flexible Core materials using the Convert to Core function.

Select the adjacent layers within the stack – Speedstack adds the Convert to Core command to the Edit menu.



Select the Core type – Speedstack displays the core library; select the core – the layers are converted into the selected core; note that when converting two foils to a single core material the lower copper trace will be shown inverted.

Consider the stack below. Using ‘Convert to Core’ alongside other Speedstack editing functions, an electrical layer only stackup can be converted into a useful fully defined stackup containing full definitions of foils, prepreg and core materials.



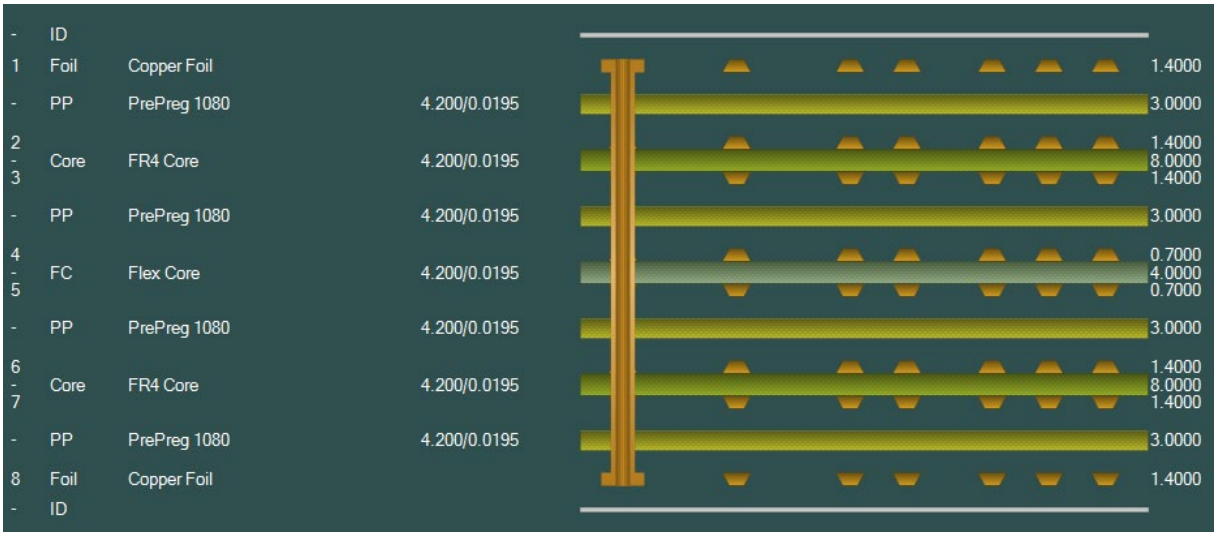
Add a prepreg layer between layers 1 and 2.

Repeat for layers 3 and 4, 5 and 6 and 7 and 8.

Select layers 2 and 3 and convert to a core.

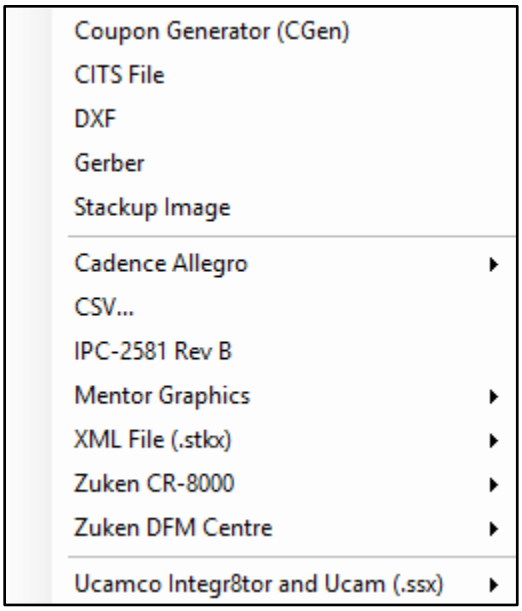
Repeat for layers 4 and 5, 6and 7.

The resulting stack should appear similar to the stack below.



Exporting stackup information

Speedstack incorporates the facility to export stack data to external programs. From the File menu choose Export and choose the format from the Export sub-menu.

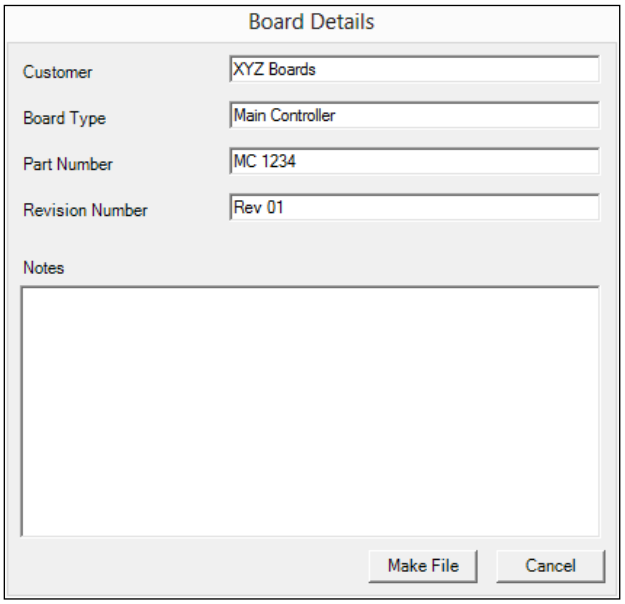


Exporting to Coupon Generator (CGen)

Stacks may be exported to the Polar CGen Coupon Generator for subsequent processing into test coupons. Click Export To | Coupon Generator – open the file in CGen.

Export CITS File

Use the Export CITS File to create test files for Polar CITS controlled impedance test systems. Supply board details via the Board Details dialog.



Click Make File to generate .cif files (CITS test files).

Generating printed output

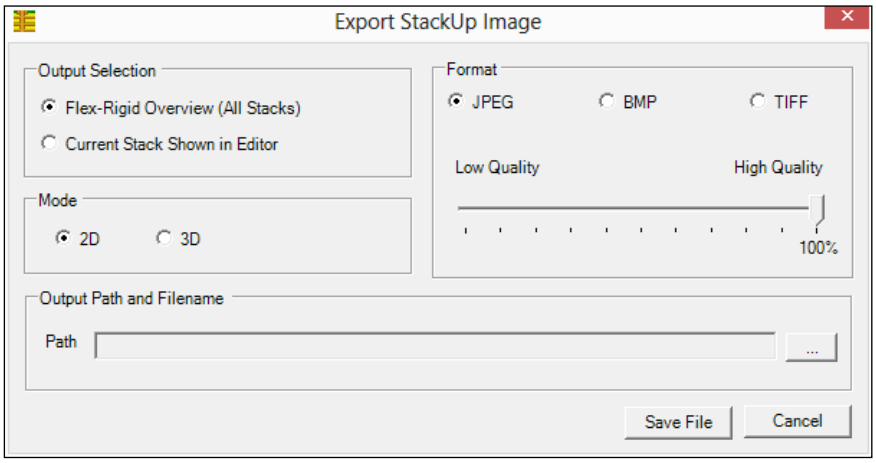
Speedstack can generate printed output in DXF, Gerber, CSV and XML, as well as graphic image formats.

DXF, Gerber, CSV and XML files

Choose DXF…, Gerber…, CSV… or XML File and navigate to a suitable folder, name the file as appropriate and save.

Stackup images

Speedstack can export stackup images in JPEG, BMP and TIFF file formats. Select from 2D or 3D displays.

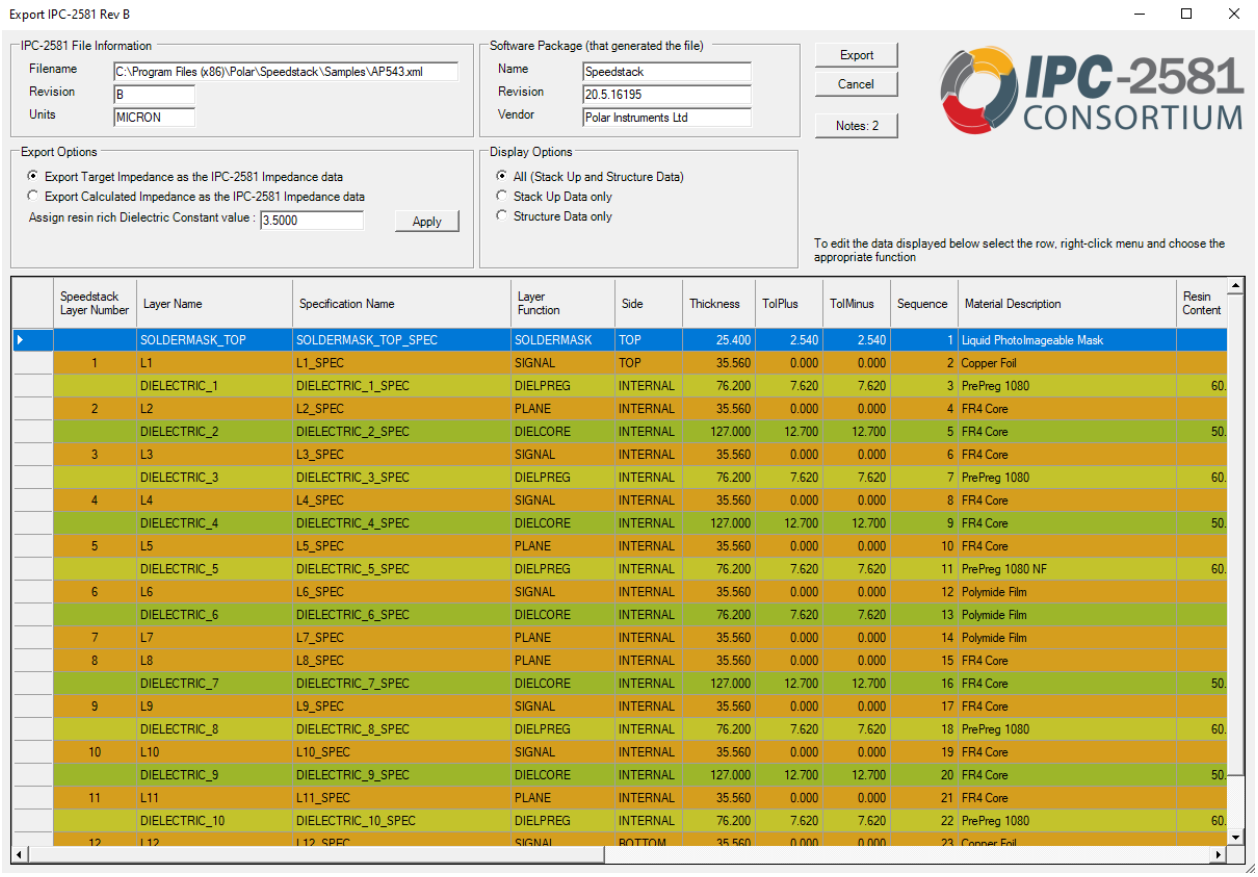


The Low Quality – High Quality slider specifies JPG quality.

Choose the Flex-Rigid Overview (if appropriate) to display the master stack and associated sub-stacks or Current Stack Shown in Editor. Specify the destination folder and file name and save.

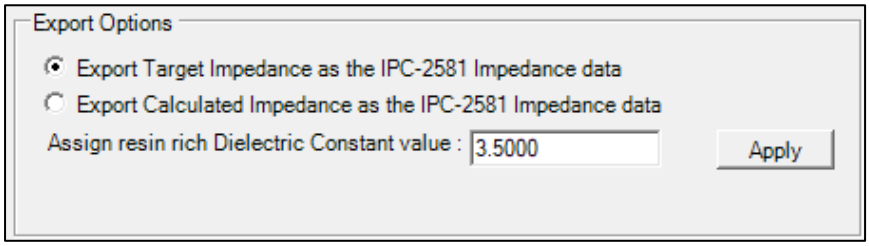
Cadence Allegro (IPC-2581 Rev B)

Speedstack supports reading/writing in IPC-2581 Rev B formatted data. Choose the Cadence Allegro/IPC-2581 Rev B option and supply the file name and destination folder: the Export IPC-2581 Rev B dialog is displayed.



Choosing export options

Use the dialog to modify, if necessary, the file information details and choose the export options.



Specify whether Speedstack's target or calculated impedance is to be used to populate the IPC-2581 file.

Supply a value for dielectric constant and click Apply.

Click Export.

Mentor Graphics
Choose the Mentor Graphics option, choose the file version and supply the file name and destination folder. (Note the .ssx file extension.)

Zuken CR-8000/DFM Centre
The Zuken CR-8000 and DFM Center PCB manufacturing pre-processing and CAM systems integrate directly with Polar Instruments' Speedstack PCB system. Choose the file version, navigate to a suitable folder and save the file (XML format).

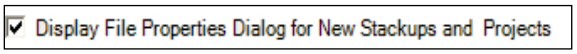
Ucamco Integr8tor and Ucam
Choose the Ucamco Integr8tor and Ucam option and file version and supply the file name and destination folder. (Note the .ssx file extension.)

Assigning properties to projects and stackups

The stack file Properties dialog may be displayed automatically each time a new stackup is created (see Tools|Options|General) and provides a range of text fields for descriptive information, e.g. stackup author, company name, file create date, stackup name, version, etc.

From the File menu choose the Properties command to add descriptive text fields — information contained in the Properties dialog will be displayed on stackup printouts.

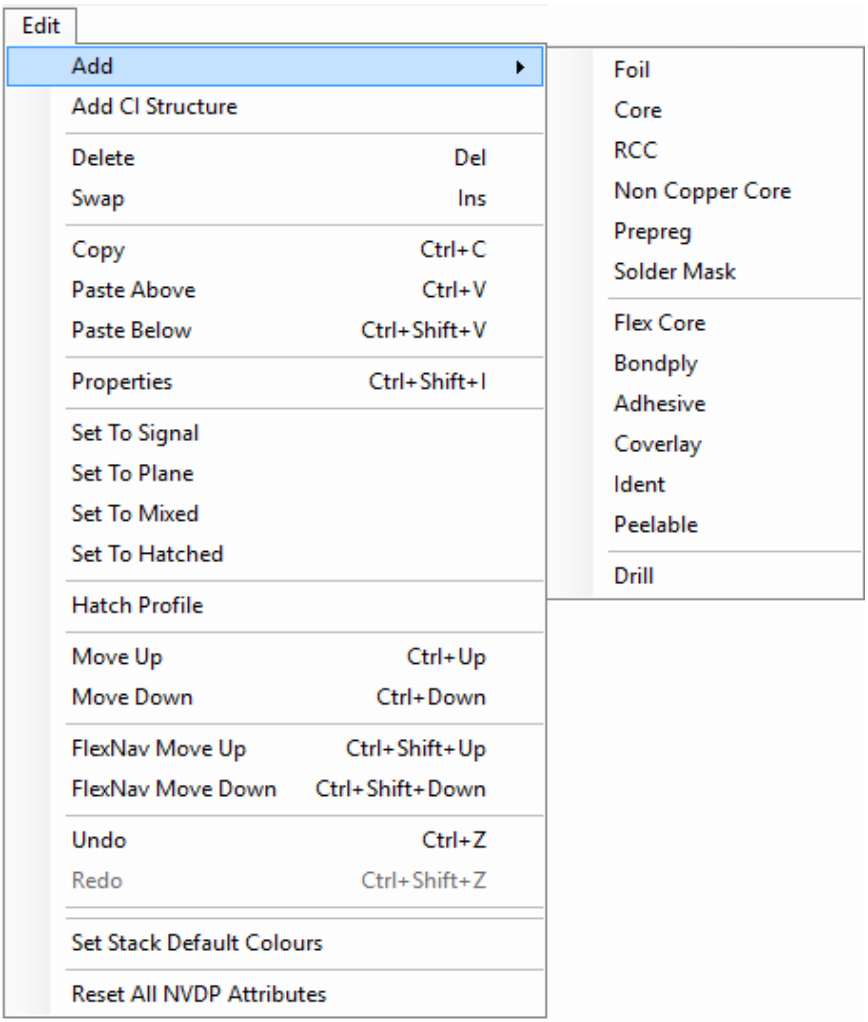
To display the Properties dialog each time a new stackup or project is created, from the Tools menu choose Options and click the check box below on the General tab



Backing up stackups and libraries
It is strongly recommended that stackup files (assigned the .stk extension), project files (assigned the .sci extension) and library files (assigned the .mlbx extension) be backed up to a secure location.

Opening recent files
Click Recent Files to select and open a file from the most recently used file list.

The Edit menu



The Edit menu contains the commands necessary to create and modify board stackups. The designer or fabricator works within the free-form stackup build and construction window and in Materials Library mode adds layers of foil, core, prepreg, etc., from the materials library.

Material Library and Virtual Material modes

Speedstack provides the option to switch easily between Material Library and Virtual Material modes allowing the stack designer to build and experiment with stackups (for example, to examine the effects on impedance structures of different trace widths or dielectric heights) without requiring real materials to be entered into a materials library.

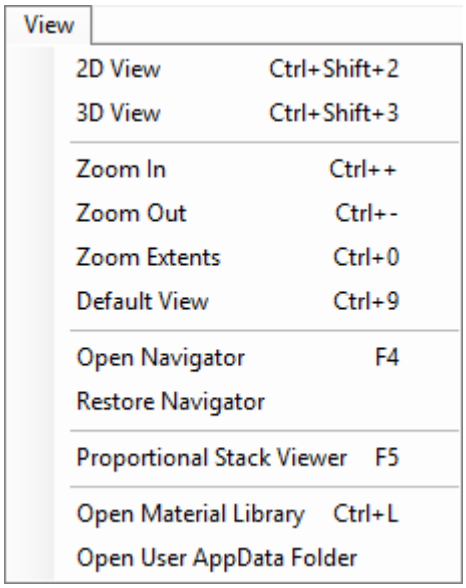
Controlled impedance structures can be added to the stack. When Add CI Structure is selected Speedstack switches to the Controlled Impedance pane and allows the designer to add structures appropriate for the selected layer. The items that can be edited depend upon whether the Stack Up Editor or Controlled Impedance tab is selected.

Layers can be changed to signal, plane, mixed or hatched, moved up or down or copied and pasted, or assigned properties as required.

Use the Delete and Swap commands to delete materials or swap materials from the Materials Library.

The View menu

Use the View menu to change the Stack Editor display whilst adding or removing materials or modifying or refining the stack.



The View menu allows Speedstack to display the stackup in a 2-dimensional or 3-dimensional aspect.

Zoom In to get a close-up view of the stack or Zoom Out to see more of the stack at a reduced size. Zoom Extents will adjust the zoom level to display the whole stack.

Hint: Click the mouse centre button/wheel to Zoom Extents.

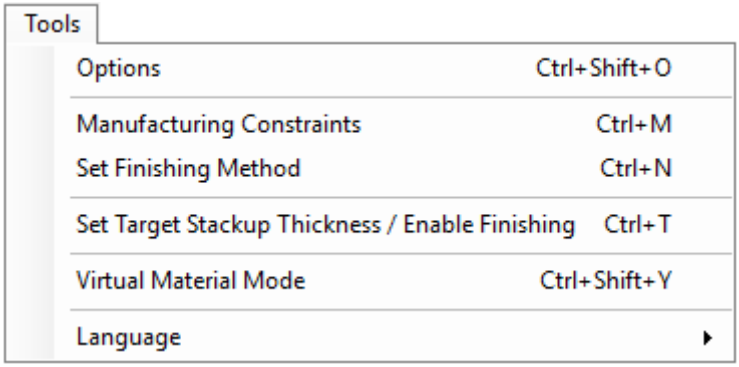
With the Flex / HDI option installed choose the Open Navigator command to view the master and associated sub-stacks. The floating Navigator window may get covered by other application windows when switching between programs; – use the Find Navigator to display a reduced Navigator window at the top left screen corner.

Proportional Stack Viewer

Use the Proportional Stack Viewer to display the stack currently selected in the Stack Editor so the material thicknesses are shown proportional to each other. This can be informative as a visual aid, especially when considering the dielectric thicknesses between electrical layers.

The Tools menu

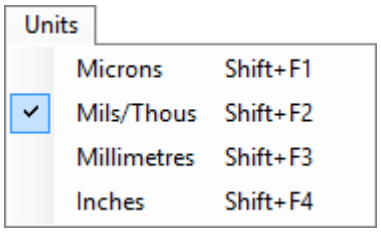
Use the Tools menu to configure Speedstack.



The Options command displays the configuration options, manufacturing constraints, target stack thickness and finishing options. See *Configuring Speedstack* for details.

The Units menu

Use the Units menu to select the stackup units, Microns, Mils/Thous, Millimetres or Inches



External Utility

Use the External Utility commands to start a program external to Speedstack. The programs are defined in the Configuration Options|External Ulilities dialog.

The Help menu

Use the Help menu commands to access the User Guide for the current Speedstack version or tutorials relating to common Speedstack operations.

Review the licensing terms with the License and About Speedstack commands.

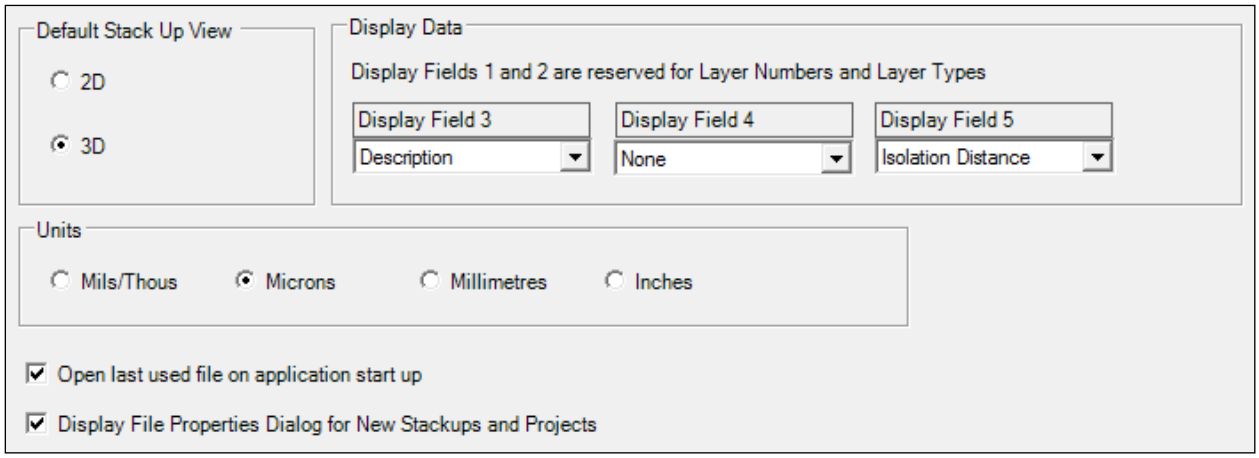
Configuring Speedstack

When first run, the Speedstack environment is initialised to its factory settings. These may require adjustment before outputting a finished stackup and/or project. Default settings are changed using Tools|Options, Tools|Manufacturing Constraints and Tool|Set Finishing Options.

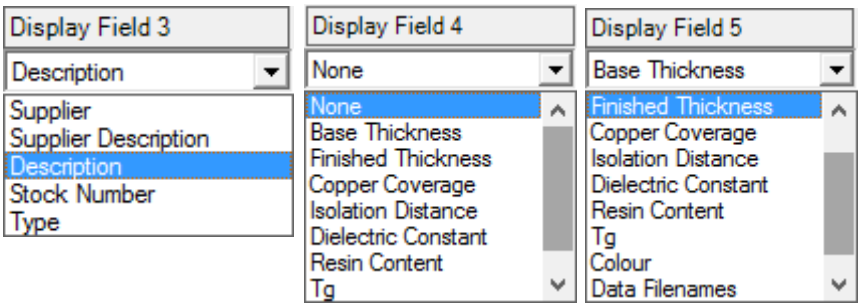
Environment and default settings

From the Tools menu choose the Options command to display the Configurations Options dialog.

General Options



Choose the Default Stackup View – 2D or 3D; select the data fields that will appear alongside the stack in the Stack Editor

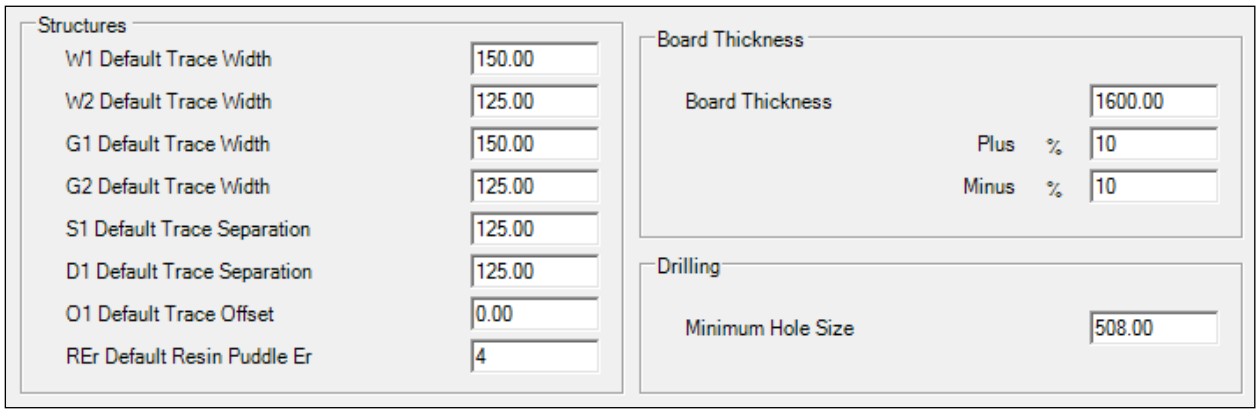


Choose the stackup units; Speedstack supports Mils/Thou, Microns, Millimetres and Inches. Click the Open last used… check box to specify that Speedstack should open the last used file on start-up.

Note: Processed Thickness is the Finished Thickness for copper layers and Isolation Distance for dielectric layers.

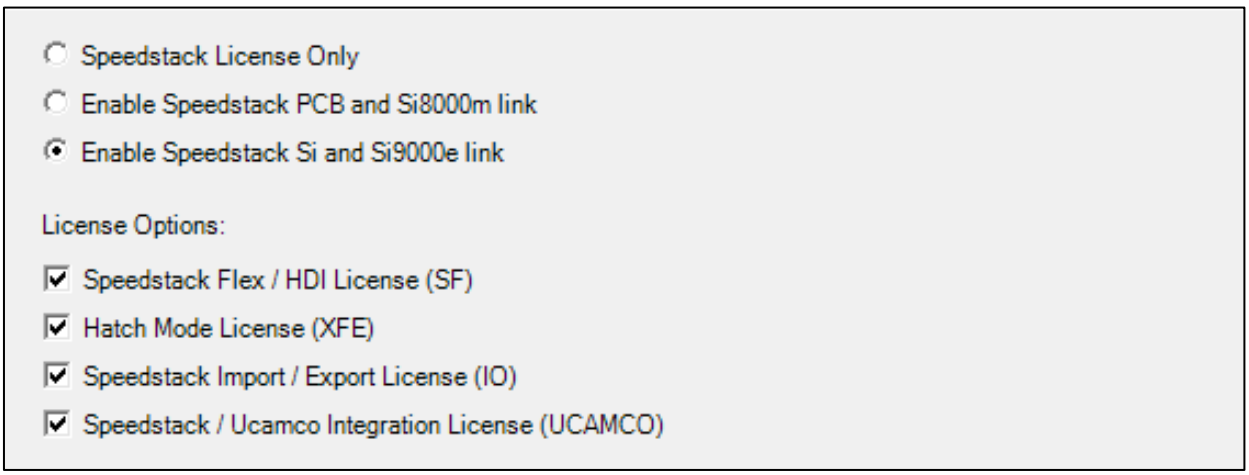
Clicking the Display File Properties Dialog… will display the File Properties Dialog each time a new stackup or project is initiated.

Structure Defaults



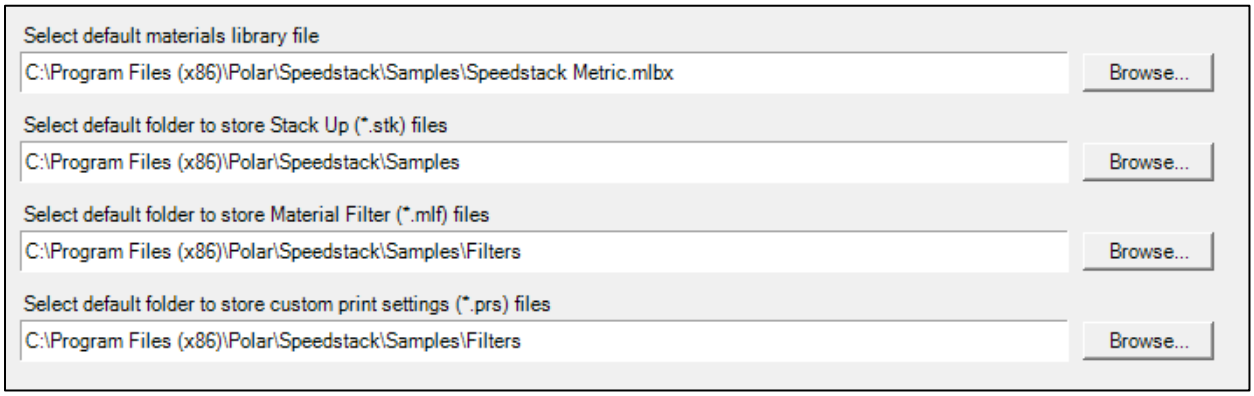
When adding new controlled impedance structures default values are entered for the trace widths and separations. Use the Structure Defaults tab to specify the default structure parameters, board thickness and minimum drill hole size.

Licensing
Use the Licensing tab to tick the purchased licensing options.



To activate the Speedstack controlled impedance function, ensure that the Si8000 or Si9000 is installed; from the Licensing tab choose either Use Polar Si8000m License or Use Polar Si9000e License option as appropriate.

Choosing default file locations

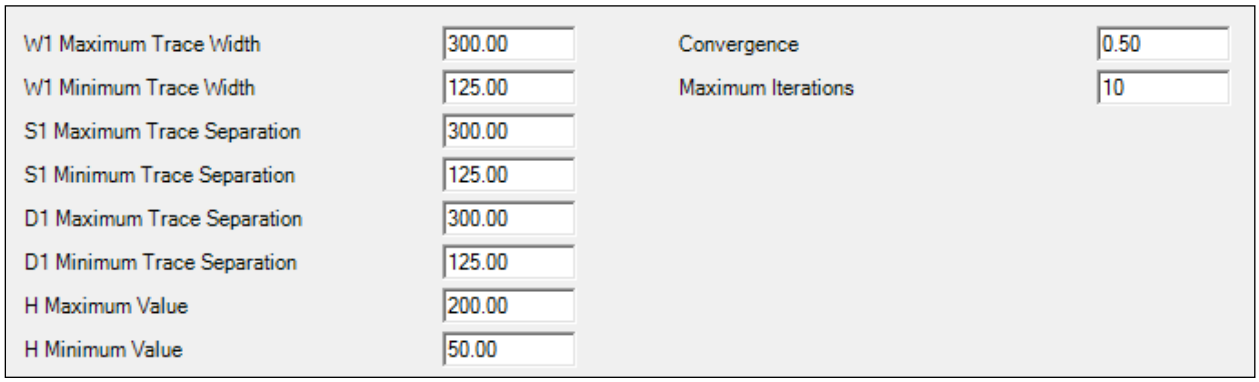


Use this dialog to choose which materials library the Speedstack uses at start-up. Click the File Locations tab and use the Browse button to navigate to the library (.mlbx) file.

The File Locations tab provides for default locations for stackup or project files, Material Filter (.mlf) files and custom print settings (.prs) files. Browse to the target folders and click OK to confirm (create new folders if necessary).

Specifying goal seeking parameters

Click the Goal Seeking tab to specify the default values for trace widths and separations used during goal seeking.



During goal seeking the calculated value for impedance will progressively converge upon the target value.

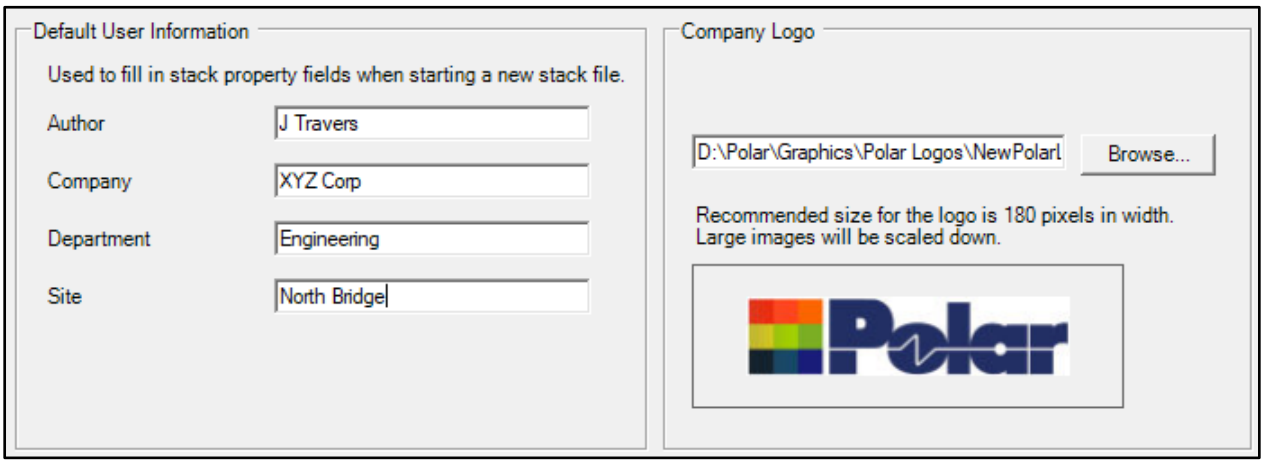
In the Convergence text box specify the difference between the target impedance and the actual impedance at which goal seeking will terminate.

Use the Maximum Iterations text box to limit the number of iterations used during goal seeking.

Setting user defaults

Information added to the User tab will be transferred to the File Properties dialog and used on printouts

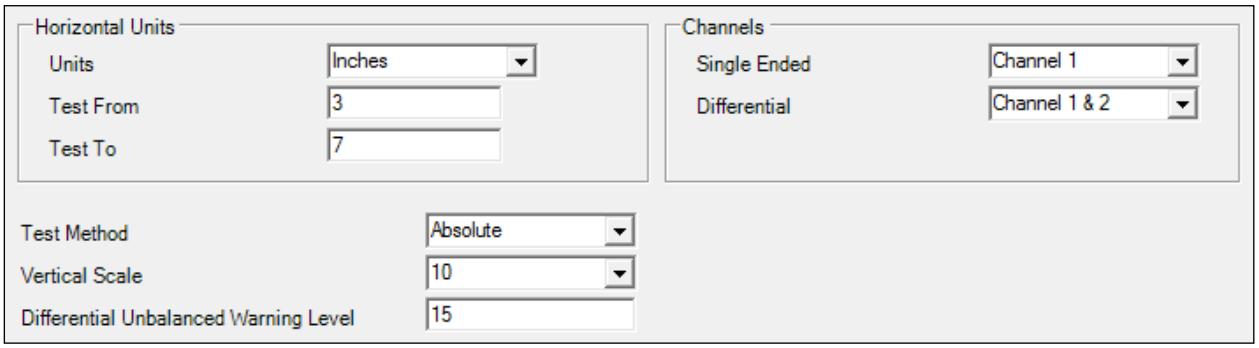
Enter information as appropriate into the associated text fields; optionally, select a graphic for use as the company logo — optimum graphic size is 180 x 32 pixels — the graphic is printed in the preview box.



Specifying default CITS test file parameters

Speedstack allows the user to generate a CITS test file for each controlled impedance structure within the stack.

Select the CITS Test tab to specify the default test parameters to be used when initiating a CITS test file.



Each test file contains the test parameters (test units, distance, number of channels, etc.) to be used when testing the stack's controlled impedance structures using a Polar CITS (Controlled Impedance Test System). The test file may be edited via the Edit Test Data dialog.

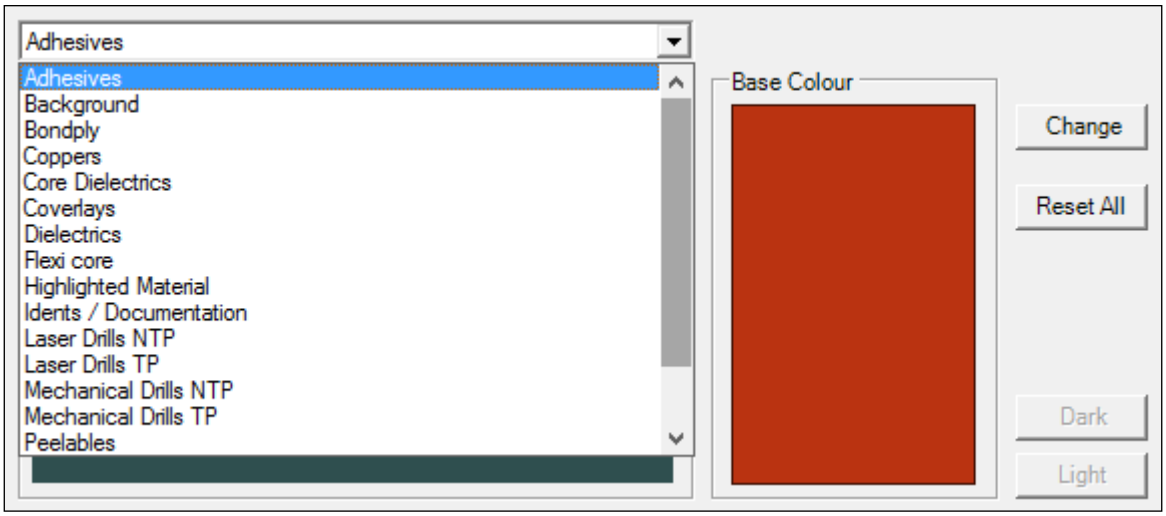
CITS test methods

Note that the preferred test method is **Absolute**

*The **Average** method should only be used with the express approval of the specifying authority.*

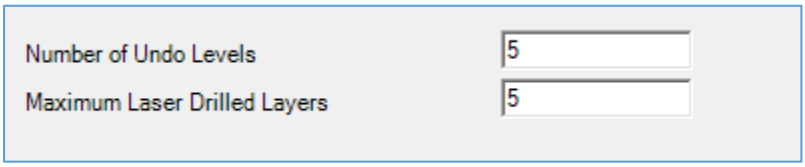
See Polar Application Note AP8515 – *CITS Test Methods*

Choosing background and stackup layer colours
Choose the Colours tab to change stackup component colours from their factory defaults.



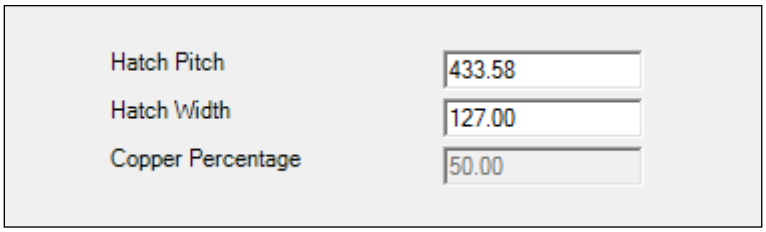
Click Reset All to return to cancel changes.

Miscellaneous Options



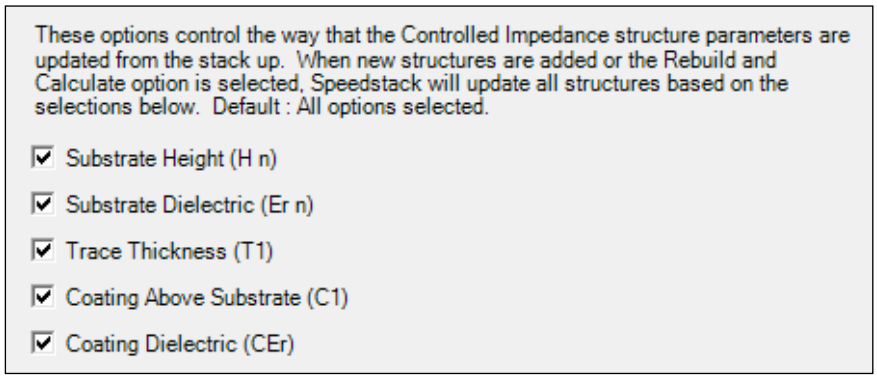
Use the Miscellaneous tab to specify the maximum Number of Undo for editing actions; choose the number of levels of editing Undo and the maximum number of layers a laser drill can span. (Exceeding this number will produce a Drill not Valid error message.)

Hatch Defaults



Use the Hatch Defaults tab to specify the default values for Hatch Pitch and Width and Copper Percentage when setting a plane to hatched (see Hatch Configuration.)

Rebuild and Calculate Structures

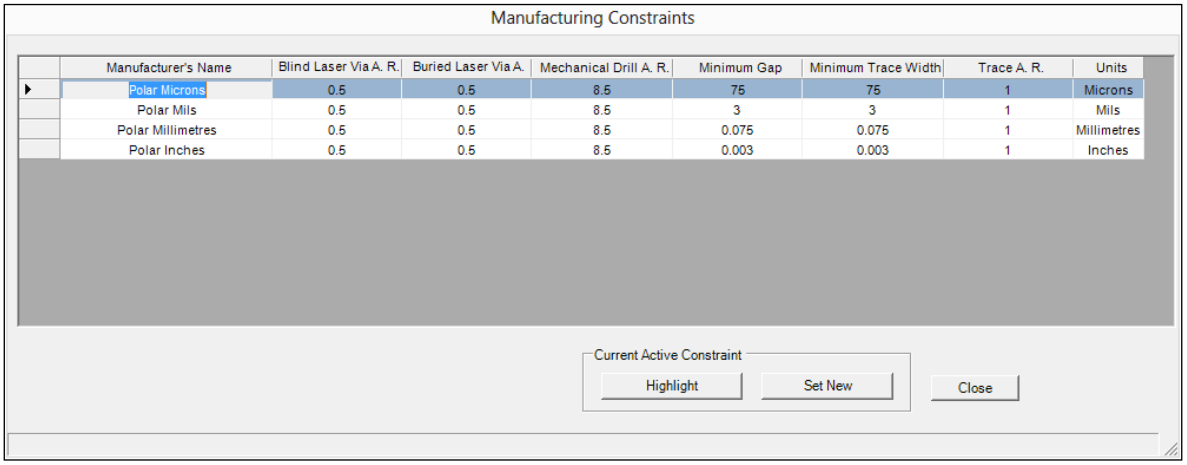


The Rebuild and Calculate Structures tab allows the designer to specify which parameters are included when controlled impedance structures are recalculated after modifying the stack.

Manufacturing Constraints

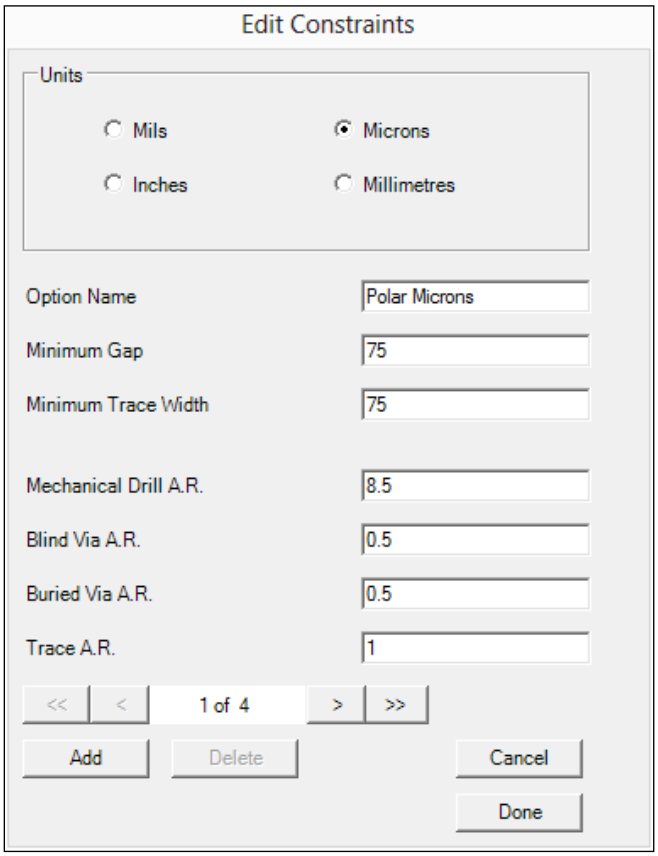
The Manufacturing Constraints options consist of a collection of manufacturing capabilities, minimum gaps and trace widths, buried and blind via and trace aspect ratios, drill aspect ratios, etc. that can be applied during design rule checking (see the DRC tab detail below.)

They will normally refer to differing levels of technology offered by one or more PCB manufacturers for a range of prices. The required information (shown in the example below) can normally be obtained from the manufacturer.



Click the Highlight button to highlight the current active constraint; to apply a new constraint select the constraint row and click Set New.

Editing and adding constraints
To modify a constraint or add a new constraint, double click within the constraint row to be edited.

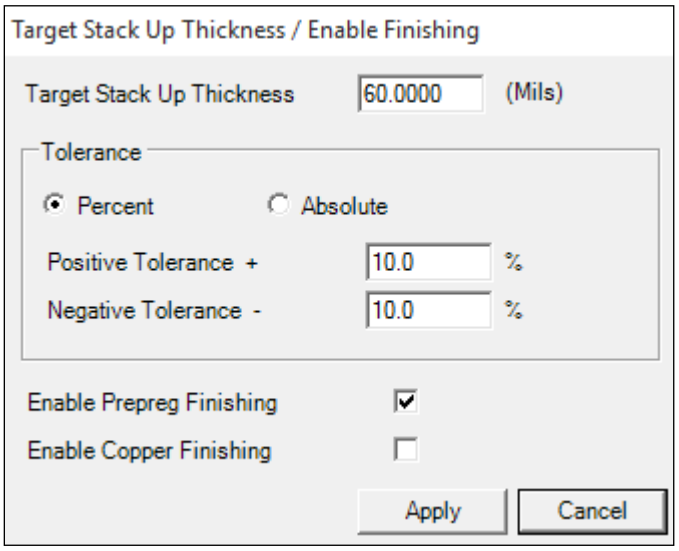


Modify each setting as required; click Done to confirm the settings and close the dialog.

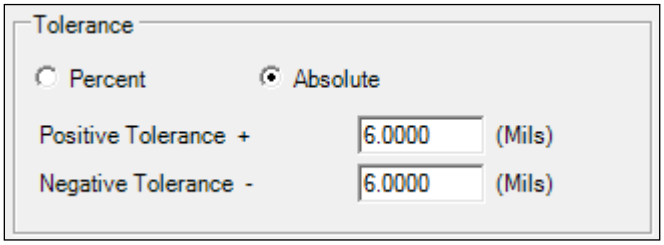
To add a new constraint click the Add button, fill in the settings fields and click Done to finish. The new constraint will be added to the table of current constraints. Click the Delete button to remove the constraint from the list.

Set Target Stackup Thickness/Enable Finishing

Set the Target Stackup Thickness and tolerances via the dialog below.



Tolerance may be set in terms of percentage or absolute values:



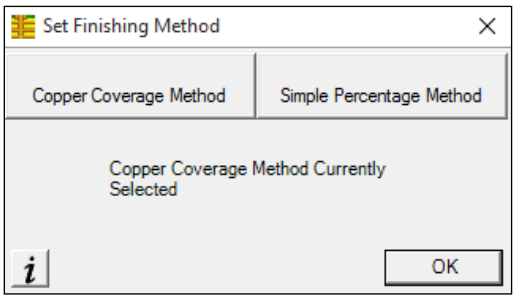
Note that positive and negative tolerance values can be set independently. The values should reflect the currently selected units.

To enable prepreg and/or copper finishing tick the associated check boxes. Click Apply.

Note: Unchecking the Enable Finishing options disables the Apply and Reset Finishing buttons. Note that these buttons are only available in Materials Library Mode – they are disabled in Virtual Material Mode.

Finishing Options

From the Tools menu choose the Set Finishing Method command to display the set finishing corrections dialog. Speedstack offers two methods: Copper Coverage Method and Simple Percentage Method.

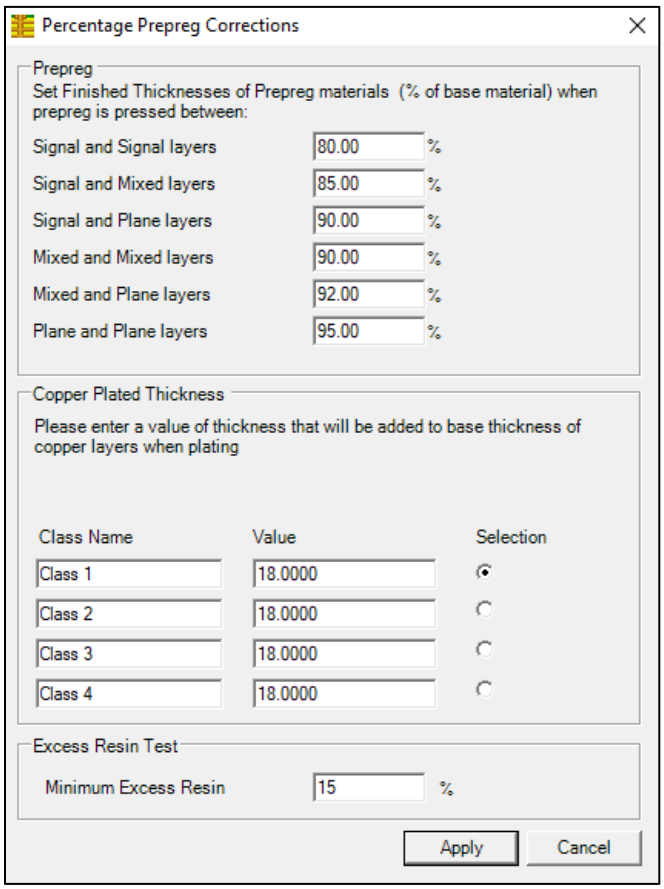


Each method requires that the amount of copper to be added where plating is required be set. In addition, where the Excess Resin design rule check is used the minimum acceptable value must be set.

Simple Percentage Method

Use the Simple Percentage Method to set the percentage of prepreg base height, which will be used to determine the isolation distance. The percentage is set for each electrical layer type pair.

Specify the IPC-6011 Class and plating thickness.

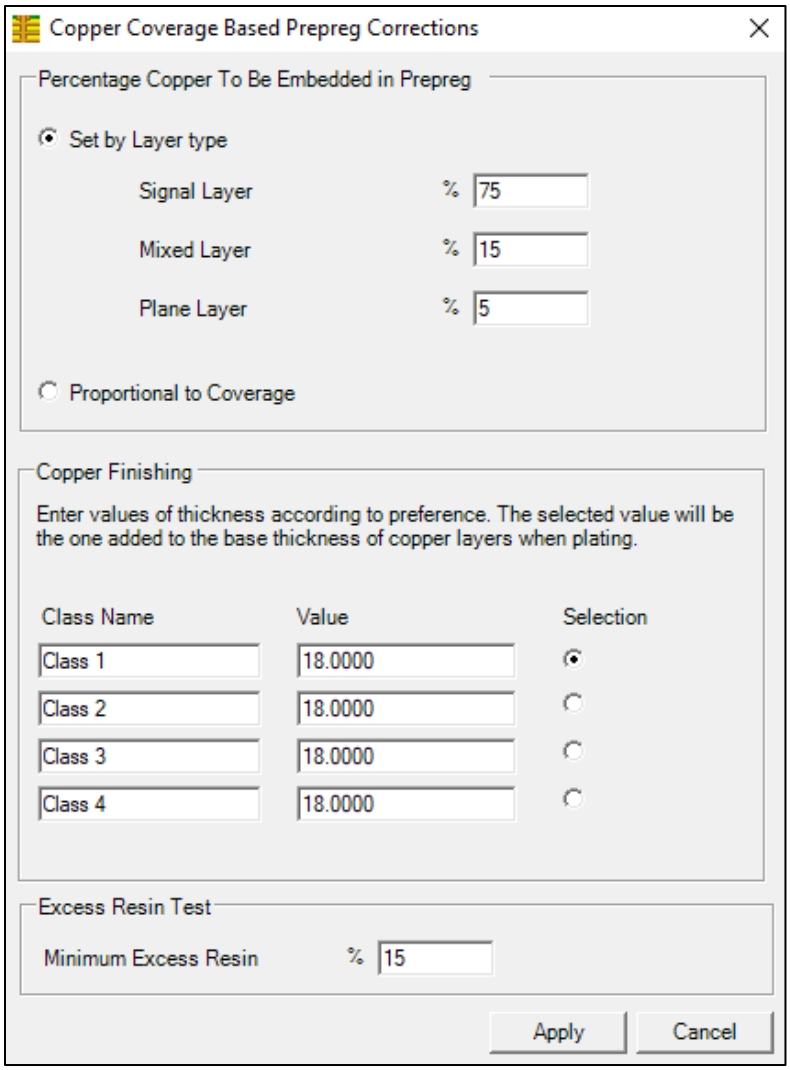


Copper Coverage method

The Copper Coverage method allows the user to specify the amount of copper that will be embedded into the prepreg.

This can be set as a single value for each electrical layer type. Alternatively the amount of copper embedded will be calculated on an electrical layer by layer basis dependent upon the copper coverage for the layer set in the properties window. The greater the copper coverage the smaller the amount of copper that is embedded.

Specify the IPC-6011 Class and plating thickness.

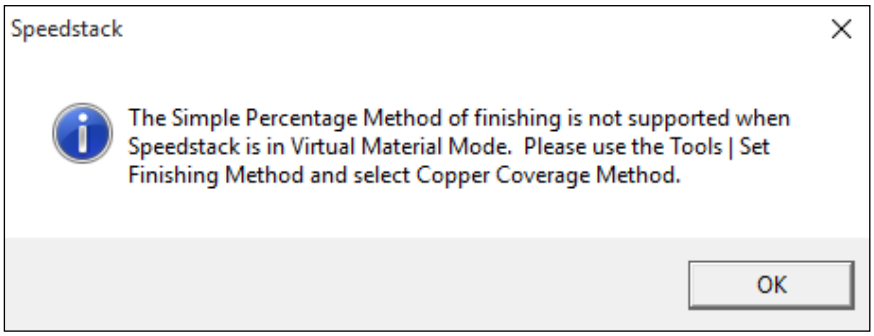


Note: The two methods of finishing are not compatible with each other. The Copper Coverage method requires that the finished thickness of prepregs be entered in the library; that value stays locked in the stack unless the Simple Percentage method is set up; if Reset Finishing is then clicked the finished thickness reverts to the base thickness.

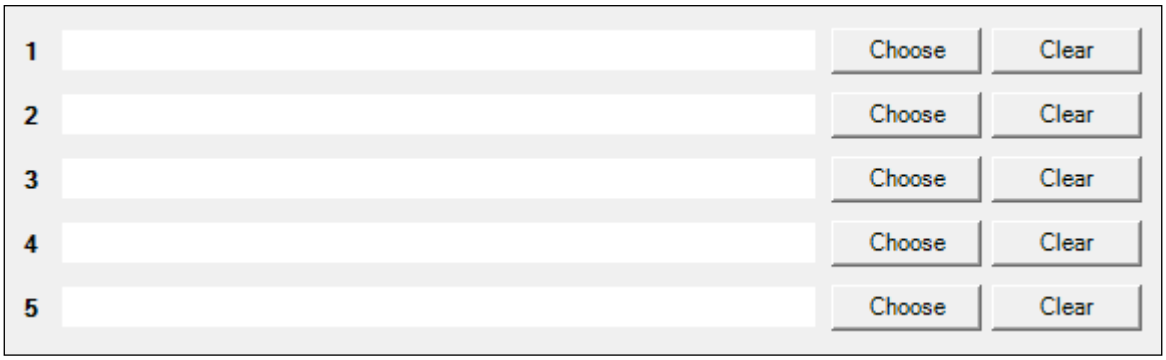
Virtual Material mode
The Virtual Material Mode command toggles between Virtual Material and Material Library modes.

Note: Switching to Virtual Material Mode disables the Apply and Reset Finishing buttons.

Note: Virtual Material mode and the Simple Percentage method of finishing are not compatible. Speedstack displays the message below if the two are selected simultaneously.



Working with external utilities
Speedstack can call an external program / utility / script via the External Utilities menu options. The menu items are configured via Configuration Options|External Utilities.



To specify a program click Choose and navigate to the program and click Open. The program will be added to the External Utility menu.

The Speedstack toolbar

The Speedstack toolbar comprises shortcut links to the most popular commands.

Note: toolbar buttons will be enabled/disabled depending on whether Speedstack is performing stack editing or controlled impedance calculations. Pause the mouse over each tool button to display the tool's screen tip

File operations

Create new stackup

Library mode

Virtual Material mode

Stackup Wizard

Stack building operations

Symmetrical Mode off

Symmetrical Mode on

Mirroring Mode

Add layer to the stackup

Click to select the layer type. The list of layer types is displayed in the associated sub-menu.

Layers available include:

Foil	Add foil layer to the stackup
Core	Add core layer
RCC	Add resin coated copper layer
Non-Copper Core	Add non-copper core

Prepreg	Add prepreg layer
Soldermask	Add solder mask
Flexible core	Add flexible core layer
Bondply	Add bond ply adhesive
Adhesive	Add Adhesive
Coverlay	Add coverlay layer
Ident	Add screened ident layer
Peelable	Add peelable mask

 Add mechanical/laser drill between layers

Editing the stackup

 Delete selected stackup material or drill

 Swap selected material

Note: the Copy and Paste buttons below are only enabled for the Stack Editor and DRC tabs – they are disabled for the Controlled Impedance and CI Results tabs.

Copying and pasting materials

 Copy material of the selected layer

 Paste material above selected layer

 Paste material below selected layer

Copy material properties

Paste material properties

Changing plane types

 Set the selected electrical layer as a signal layer

 Set the selected electrical layer as a plane

Set the selected electrical layer as a mixed signal/plane layer

Set the selected electrical layer as a hatched plane

Note: the Move Selected Layer buttons below are only enabled for the Stack Editor and DRC tabs – they are disabled for the Controlled Impedance and CI Results tabs

Move selected layer up one layer

Move selected layer down one layer

Display properties dialog for the selected layer or drill

Note: the Apply and Reset Finishing buttons below are only enabled for the Materials Library Mode with the Prepreg and Copper Finishing Options checked (see Set Target Stack UpThickness/Finishing Options) – they are disabled for the Virtual Materials Mode.

Applying finishing

Apply finished thickness

Reset finished thickness

Changing the stackup view

Display 2-dimensional view

Display 3-dimensional view

Proportional Graphics View

Managing the materials library

Go To/Display materials library

Exchanging data with the Si8000m or Si9000e Field solver

Copy controlled impedance data to field solver

Paste controlled impedance data from field solver

Copy to Si8000m or Si9000e Project

Creating and editing stackups (Virtual Material mode)

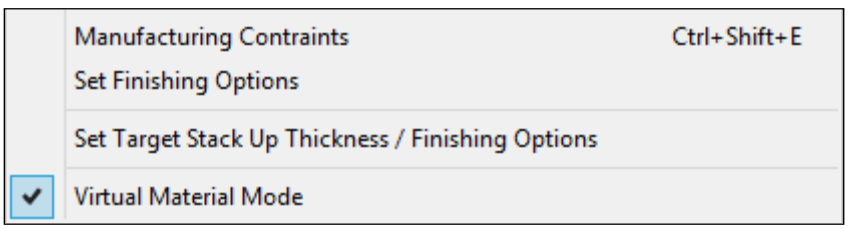
Material Library and Virtual Material modes
Speedstack provides the option of switching easily between Material Library and Virtual Material modes, allowing the stack designer to build and experiment with stackups without requiring real materials to be entered into a materials library.

In Virtual Material mode the Stackup Wizard allows rapid entry of stack details, the number of layers, overall board thickness, plane layers, solder mask and copper thickness. Speedstack will then build a stack to the specified board thickness by distributing the dielectric regions equally. If a preferred core thickness is specified Speedstack will maintain the dielectric thickness for core regions but equally distribute prepregs to reach the target board thickness.

This section will describe the steps to construct an 8-layer, symmetrical FR-4 stack to the specification below using Speedstack's Virtual material Mode.

Thickness:	60 mil
Signal layers:	1, 3, 6, 8
Plane layers:	2, 4, 5, 7
Er:	4.2
Preferred core thickness:	8 mil
Copper (all layers):	1 oz. / 1.4 mil
LPI Mask:	1 mil
PTH drill passes:	Layers 1 – 8
Laser microvia passes:	Layers 1 – 2, 8 – 7
Impedance structures:	SE 50 Ohm Layer 1, Diff 100 Ohm Layer 1

From the Units menu choose Mils/Thou, from the Tools menu toggle Virtual Material Mode On.

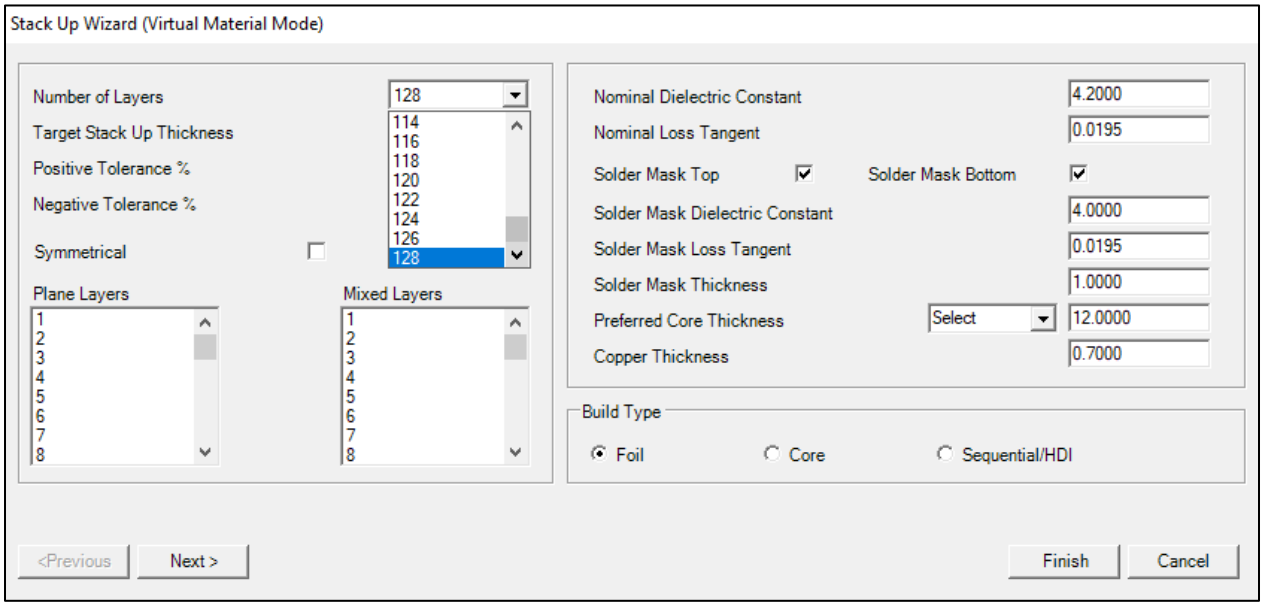


Library/Virtual Material mode indicates Virtual Material mode.

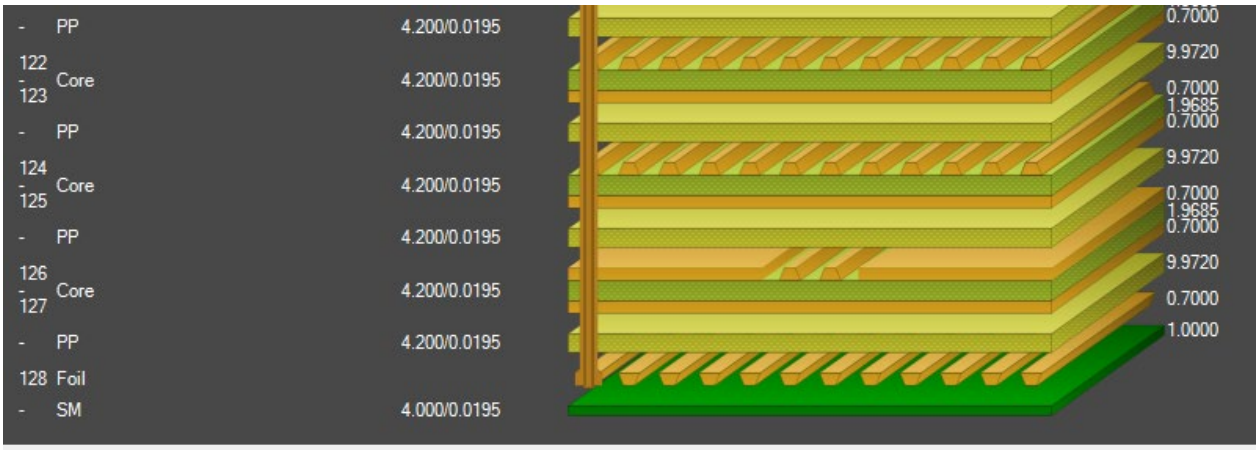
Using the Stackup Wizard

From the File menu chose New|Stackup Wizard.

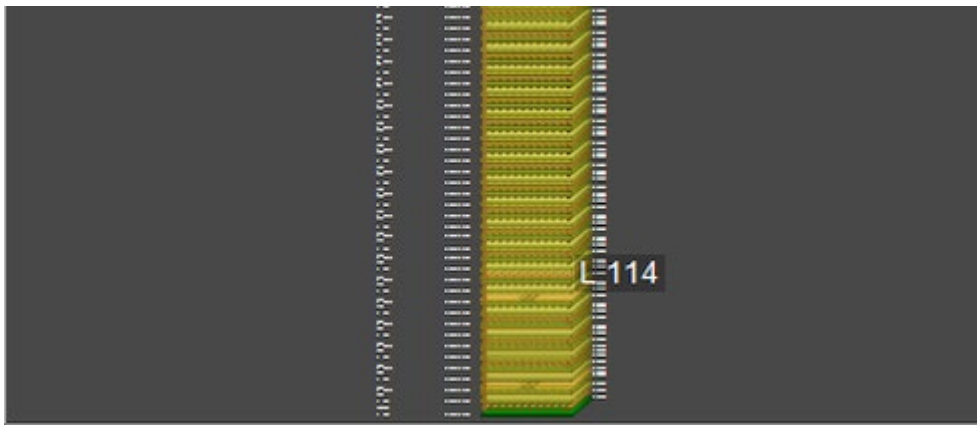
The Stackup Wizard supports up to 128 layers



In the example below the Stack Editor displays the last few layers of a 128 layer stack

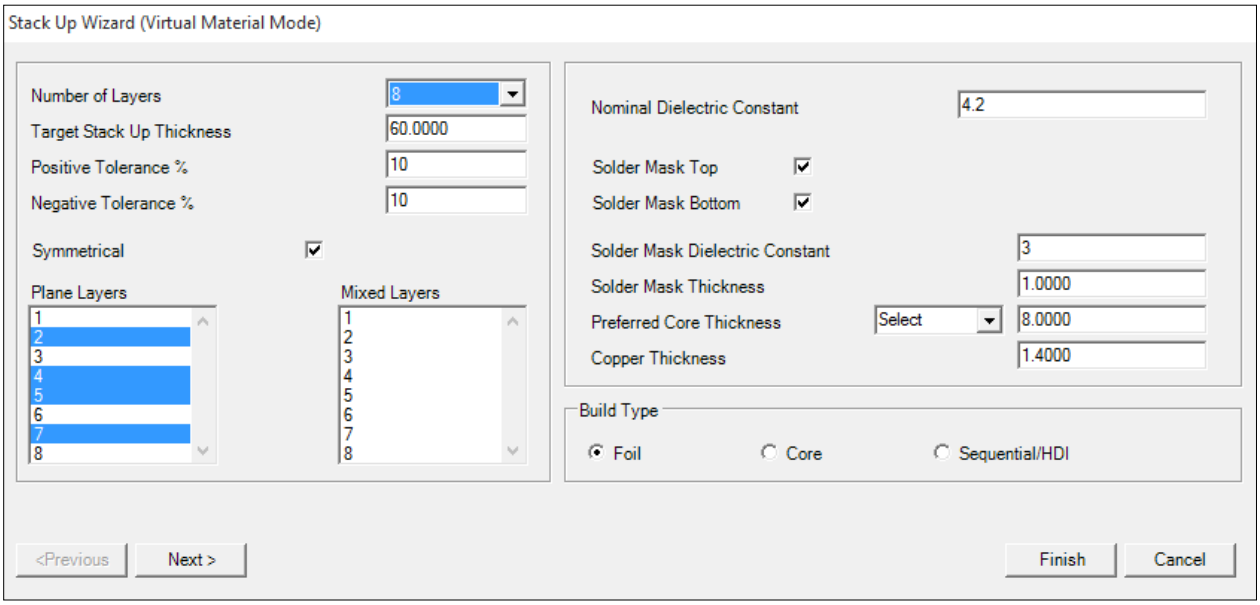


Use the Zoom Extents command to view the entire stack; navigate quickly to the layer to be edited with the mouse wheel zoom.



Setting basic stack data

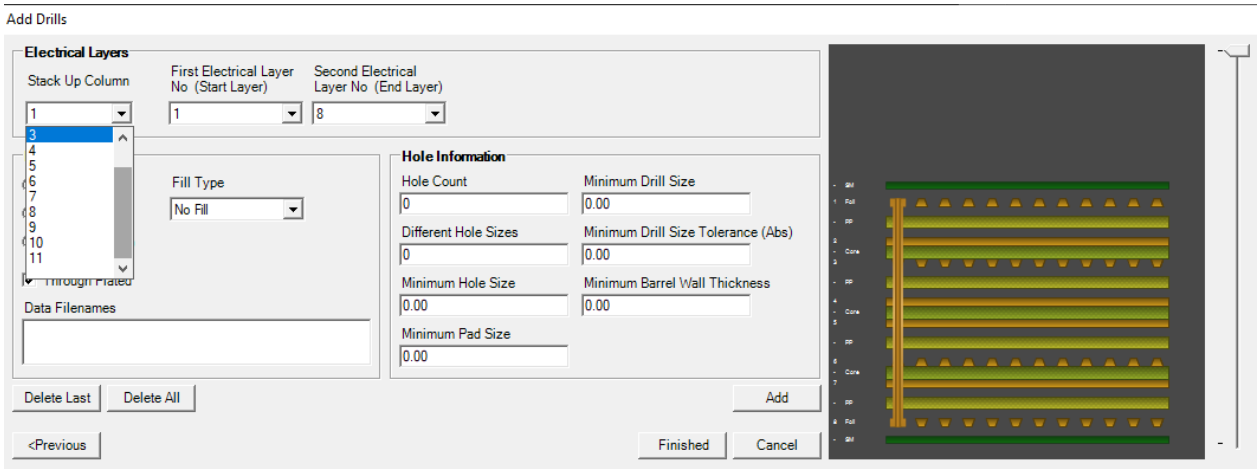
Fill in the dialog as shown below.



Click Next to add drills.

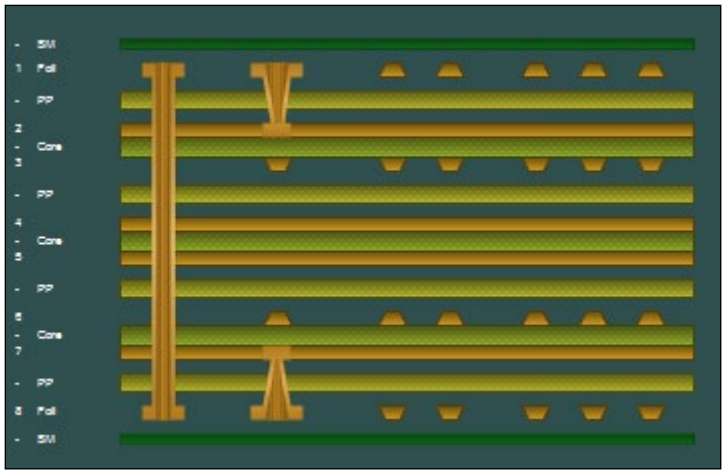
Adding drills

Drill information is assigned to drill columns (up to 11 columns are available) Select Column 1 and specify the First Electrical Layer as Layer 1 and the Second Electrical Layer as Layer 8; choose Mechanical, Through Plated with No Fill and click Add to add the first drill to the stack.



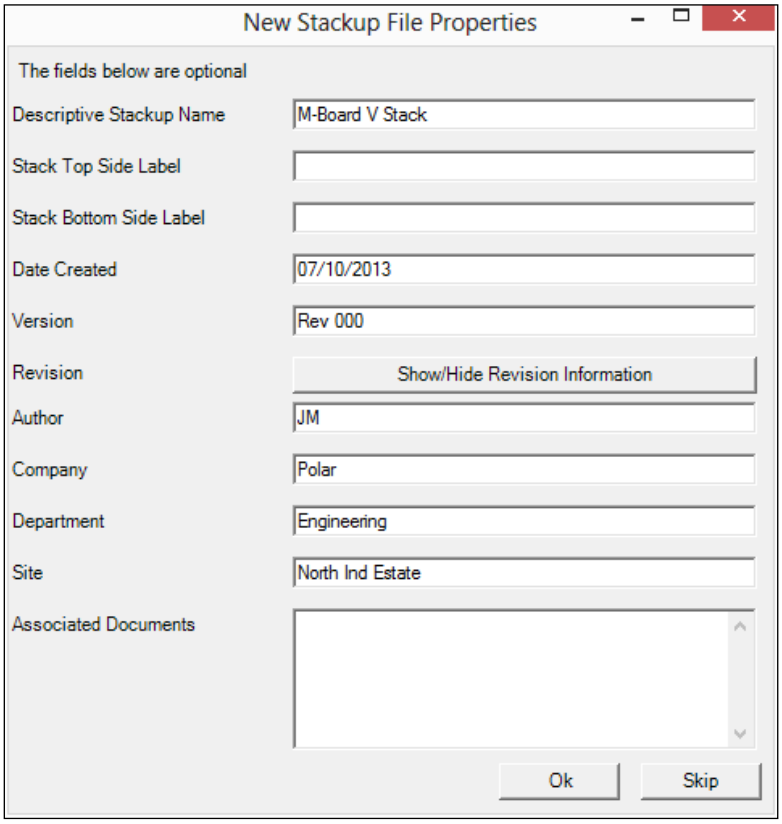
Adding microvias

Choose Column 2, specify the First Electrical Layer as 1 and the Second Electrical layer as 2; choose Laser with No Fill and click Add. Repeat the process to add another microvia to Column 2 between electrical layers 8 and 7 (shown below.)



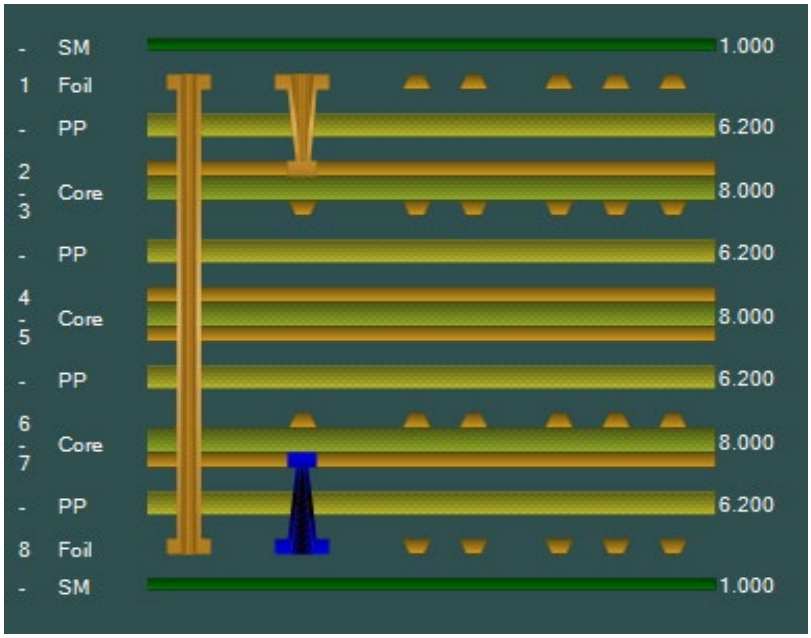
Click Finished.

The Stackup Wizard displays the New Stackup File Properties dialog; enter the (optional) stackup properties.

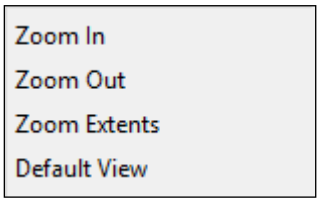


Click OK to close the dialog and edit the stack. Speedstack builds the stack to achieve the specified board thickness.

Click the 2D button to assist in visualisation while editing the stack.

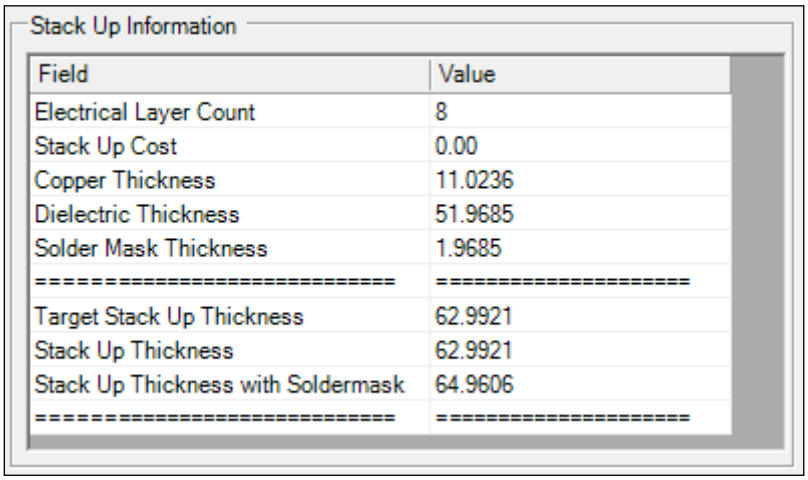


Use the View menu to zoom in and out of the stack.



Hint: Click the mouse wheel in the Stack Editor (Zoom Extents) to view the entire stack.

The Stackup Editor displays summary information for the whole stack and for items within the stack as they are selected.



Selected Item Information : Drill

Field	Value
First Electrical Layer No	8
Second Electrical Layer No	7
Mechanical Drill	False
Laser Drill	True
Fill Type	No Fill
Data Filenames	
Hole Count	0
Different Hole Sizes	0
Minimum Hole Size	0.001
Minimum Allowable Hole Size	15.2000

Editing the stack

With the “virtual” stack in the Stack Editor the stack can be changed as required.

Changing material properties

To change the properties of a material, right click the material in the stack and choose Properties; fill in the text fields with the associated information and click Apply. Most material properties can be changed, including the material descriptions, base and finished thickness, dielectric constants, drill parameters along with the graphical colours.

Choosing Symmetrical mode

Stackups are often designed symmetrically to prevent warping and twisting – using similar materials in the top and bottom halves of the stack.

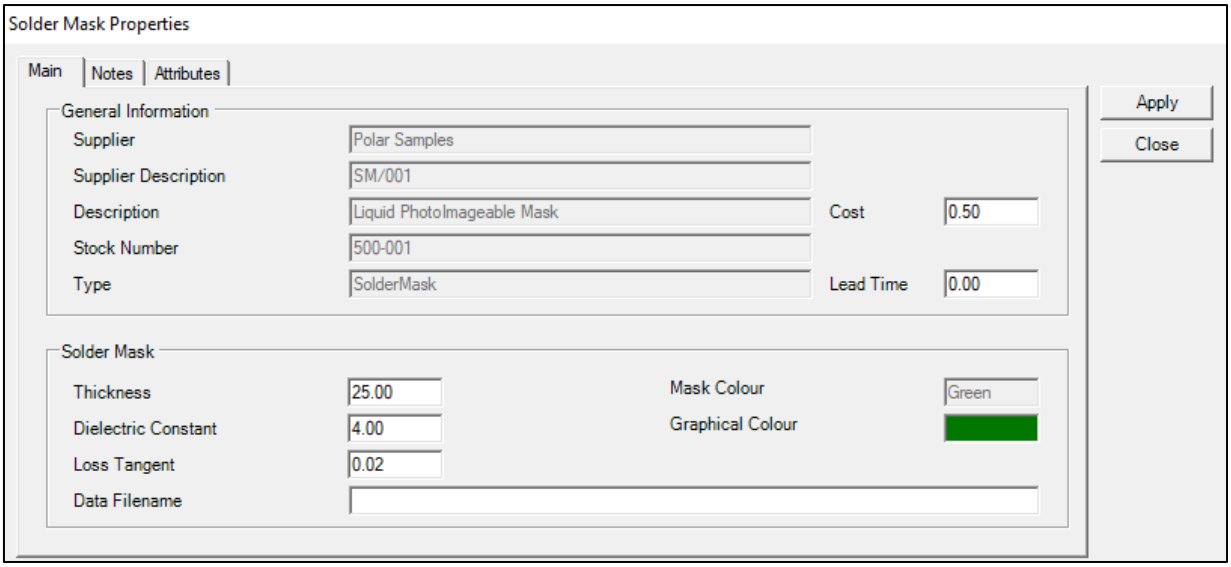
Symmetrical OFF

Symmetrical ON

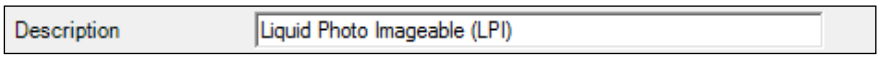
Clicking the Symmetrical button will toggle the Symmetrical mode on or off. In Symmetrical mode the stack editing functions will process materials in the upper and lower halves of the stack simultaneously.

Changing the material description

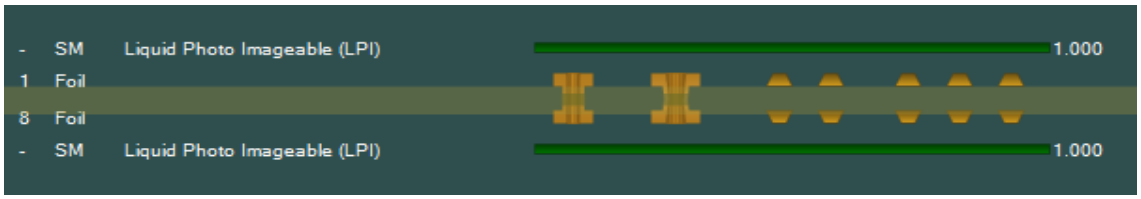
In this example stack, ensure symmetrical mode is selected then right click the solder mask material in the stack to display the Solder Mask Properties dialog.



Change the Solder Mask Description to Liquid Photo Imageable (LPI).



The change on the Description in both solder masks is reflected in the Editor window.



Changing electrical layers

Electrical layer types may be changed from plane to signal, mixed and hatched. Right click the layer to be changed and choose from Signal, Plane, Mixed or Hatched.

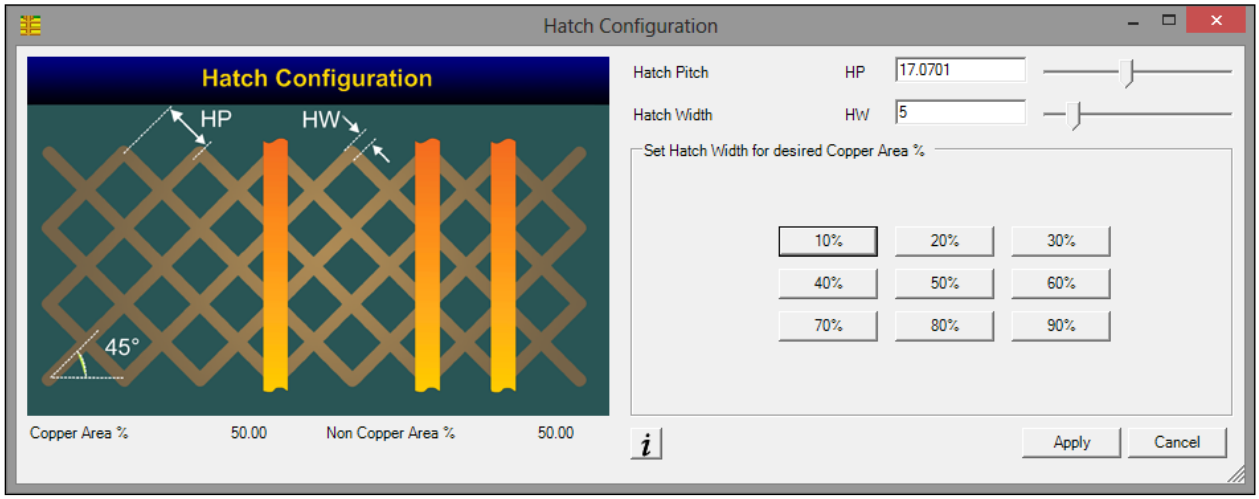
Speedstack will take the designated layer type into consideration when adding controlled impedance structures.

Setting hatched planes

Set Layer to Hatched Plane

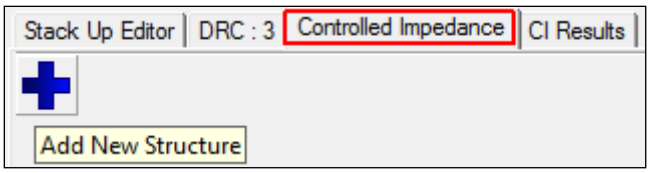
With the XFE option Speedstack supports hatched planes, implementing the same crosshatch calculation technique used in the Si8000m / Si9000e. If a crosshatch plane is required click Set Layer to Hatched Plane –use the Hatch

Configuration dialog to set hatch pitch and width or set the hatch width by percentage copper area. Click Apply.

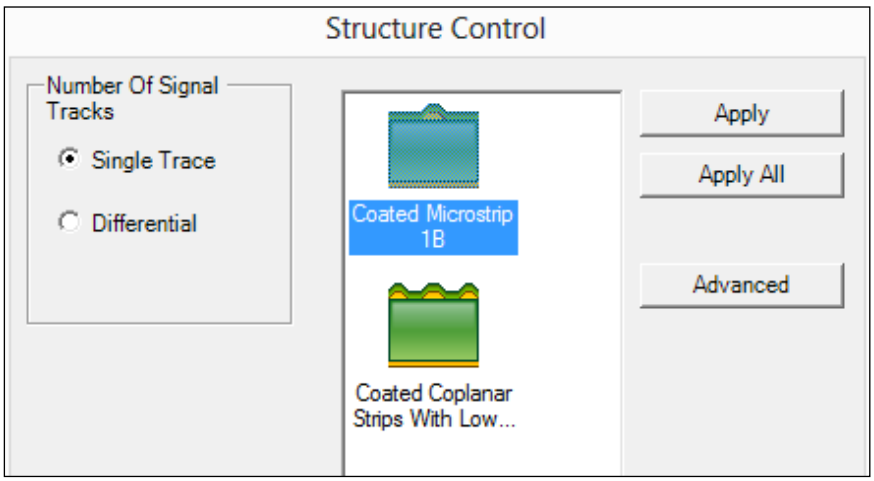


Adding controlled impedance structures

To add controlled impedance structures, click the Controlled Impedance tab, select the copper layer (in this example, Layer 1) and click the Add New Structure button.



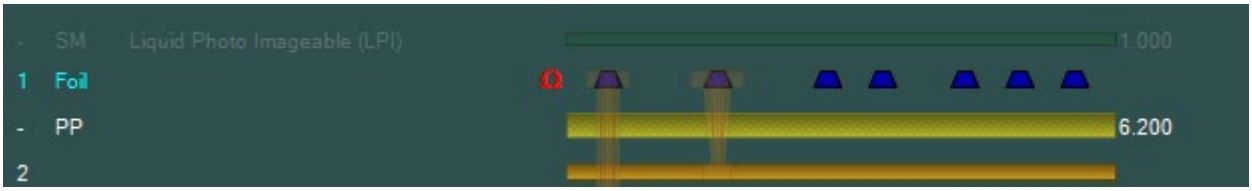
Speedstack suggests structures valid for the layer based on the plane layer types.



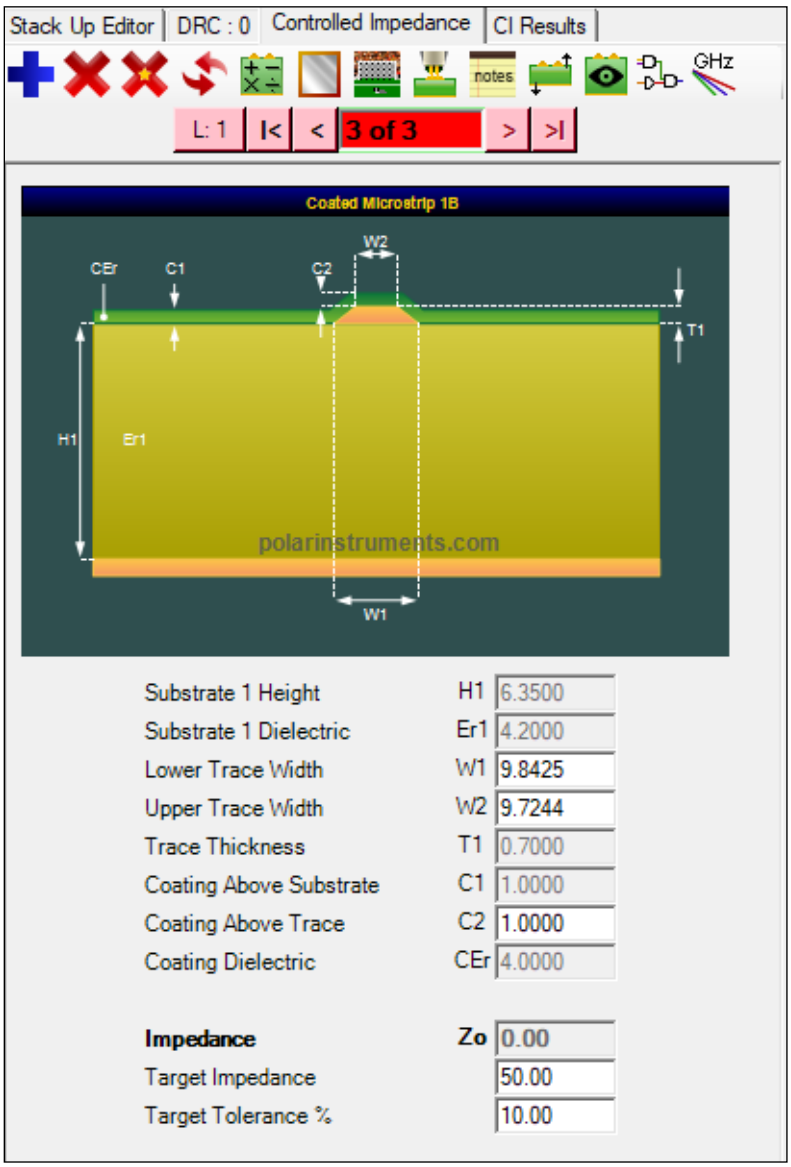
For this example, choose a 50 Ohm single ended coated microstrip; leave the tolerance at 10%; click Apply then Done.

Structure on Layer

The new structure is shown in the stack, highlighting the materials employed by the structure.



The structure also appears in the Controlled Impedance panel, along with its parameters.



Calculating the structure impedance

Parameters calculated from the stack materials, such as the substrate height and dielectric are read only and shown greyed out; other parameters may be edited. If the editable parameters are known they may be entered directly.

For example, modify W1 to read 10.5 and W2 to read 9.5 and click the Rebuild and Calculate All Structures.

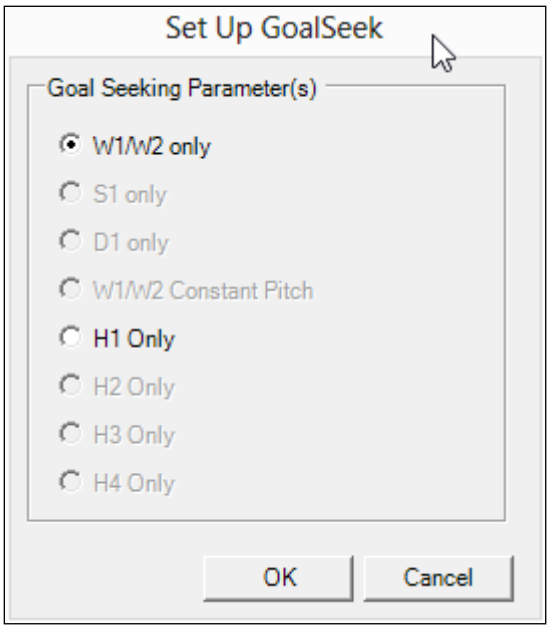
The impedance is calculated as 51.94 Ohms


Goal Seek button

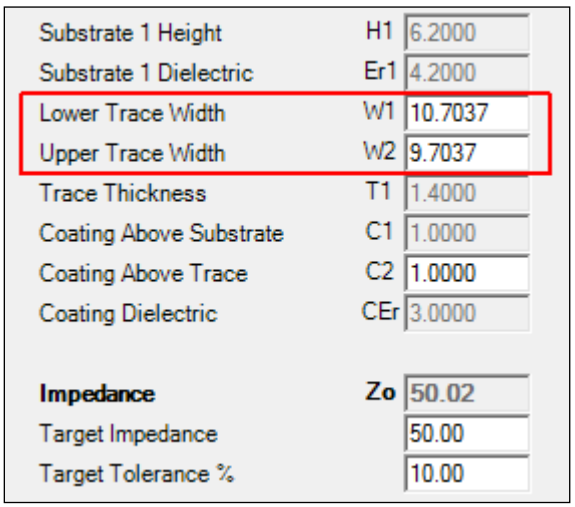
Goal Seeking the target impedance

Speedstack can adjust one or more structure parameters to achieve a specified target impedance. Leave the Target Impedance at 50 Ohms and click the Goal Seek button

From the Set Up Goal Seek dialog choose W1/W2 only



Click OK – Speedstack adjusts trace width (below) to achieve the target 50 Ohm impedance.



With the impedance in tolerance the navigation buttons display green.

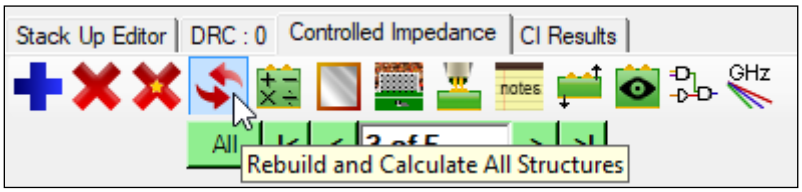
Mirroring structures

This example stack is symmetrical so structures may be copied to the lower half of the stack (i.e. on the lower outer layer.) Click Mirror Structures if Stack Symmetrical.

The impedance structure on Layer 1 is copied to Layer 8.

Rebuilding the stack

During stack editing changes to the stack (for example, inserting prepreg materials into a layer or altering the existing material thickness) will affect the impedance value of one or more structures. If Speedstack senses that an impedance structure has changed it issues a Rebuild alert.



Click Rebuild and Calculate All Structures – Speedstack recalculates the impedance for the new parameters. If the impedance value is out of tolerance the structure browse control changes colour to red.

Virtual Material mode allows the designer to experiment with material properties to examine the effects on impedance structures of different trace widths or dielectric heights, etc. Materials may be added, moved, copied, pasted or removed and the properties of materials changed – Speedstack will sense the changes and allow the “generic” stack to be rebuilt and recalculated.

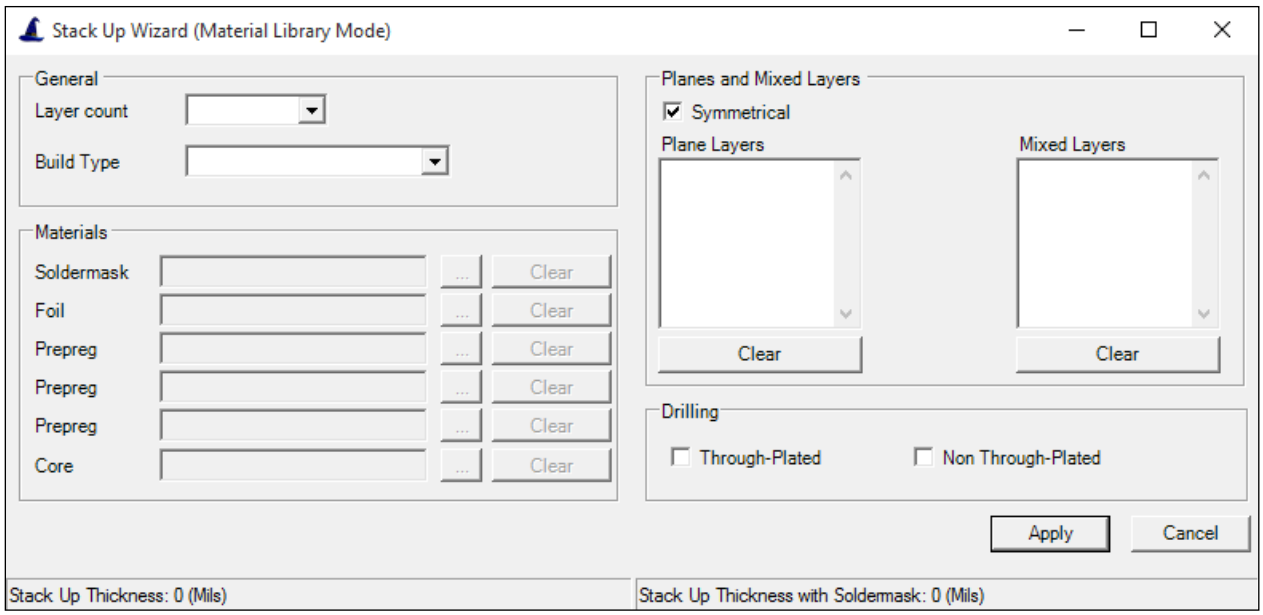
Creating and editing stackups (Material Library mode)

This section describes creating stackups using the Material Library mode. Stackups may be created manually using the Stackup Wizard or using the editing window. Ensure Tools|Virtual Material Mode is toggled Off.

Using the Stackup Wizard

Stackup Wizard button

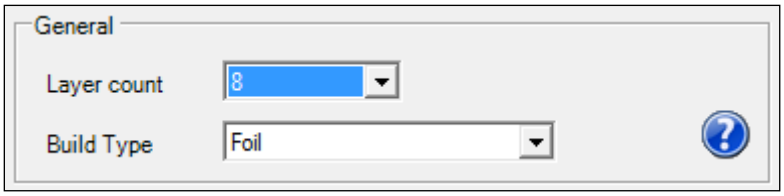
The Stackup Wizard guides the user through the process of creating complex stackups in only a few steps. Click the Stackup Wizard button or choose Stackup Wizard from the File|New sub menu. The stackup editing window is cleared and the Stackup Wizard displayed.



Using the Wizard the user can specify the layer count and build type, stackup materials, planes and drill types in a single operation.

Electrical layer count
Begin by specifying the electrical layer count — up to 64 electrical layers may be specified. Choose the number of layers from the drop down list box.

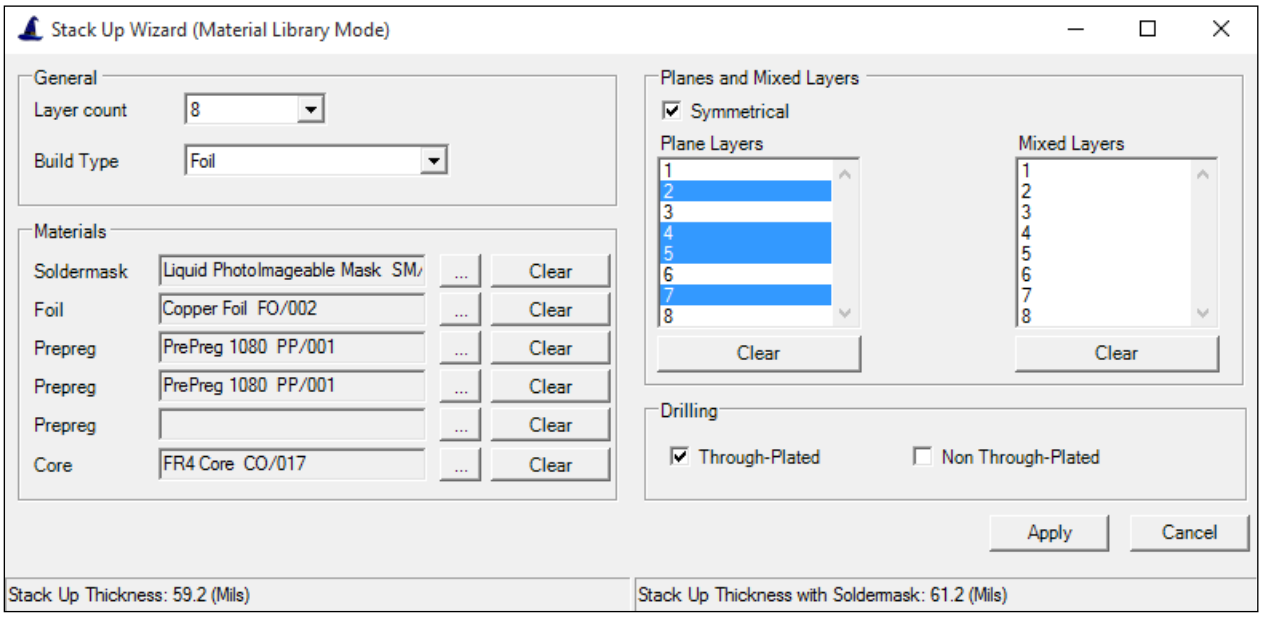
Build type
Choose the build type (Foil or Core) from the drop down list box. Core builds contain only core materials; most builds will be foil builds — containing internal layers of cores with two outer foils.



Choosing stackup materials

Note; if Core build type has been specified the Foil material control will be disabled.

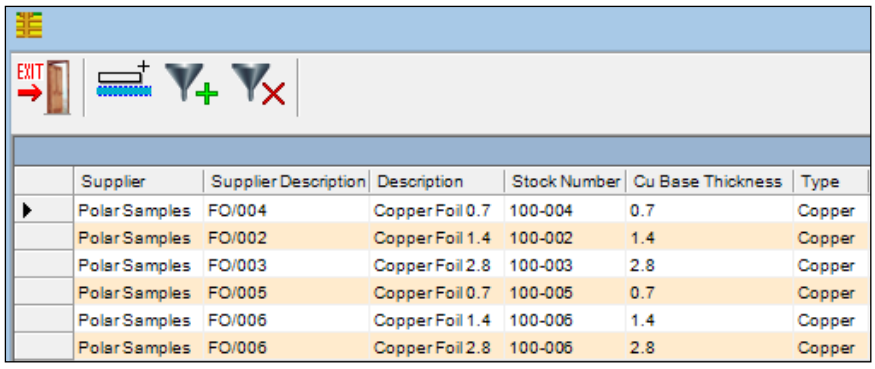
The Wizard allows for a stack comprising solder mask, foil, and cores with up to three prepreg materials between.



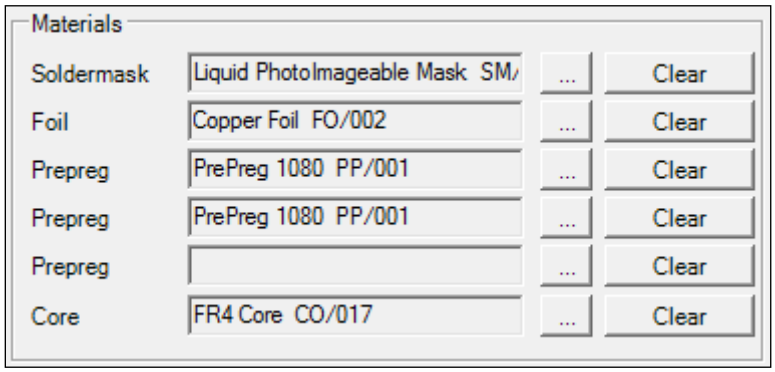
The Wizard displays a running total of the stackup thickness in the Wizard's status bar.

Adding layers

To include a layer (in this example a foil layer) click the Foil Add Material button; the library of foil materials is displayed. Choose the foil material from the list and click the Add Material Above button; the material is added as a foil layer to the stackup.

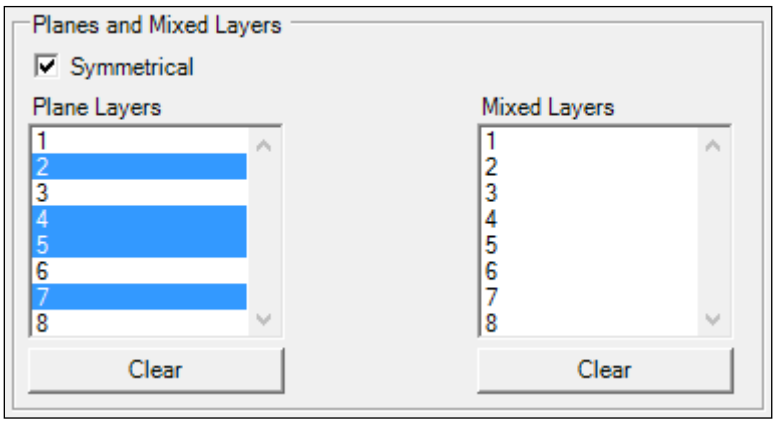


Repeat the procedure for prepreg and core materials and the (optional) solder mask layers. Use the Clear button to remove a layer from the stackup.



Nominating power planes and mixed layers

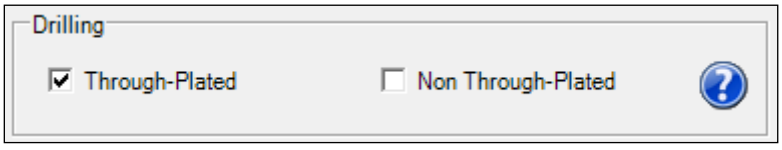
Use the list boxes to specify planes as power planes or layers as mixed layers. Select all planes as required. To remove a plane from the list select the plane number from the list and click Clear.



The dialog above shows Layers 2, 4, 5 and 7 specified as power planes

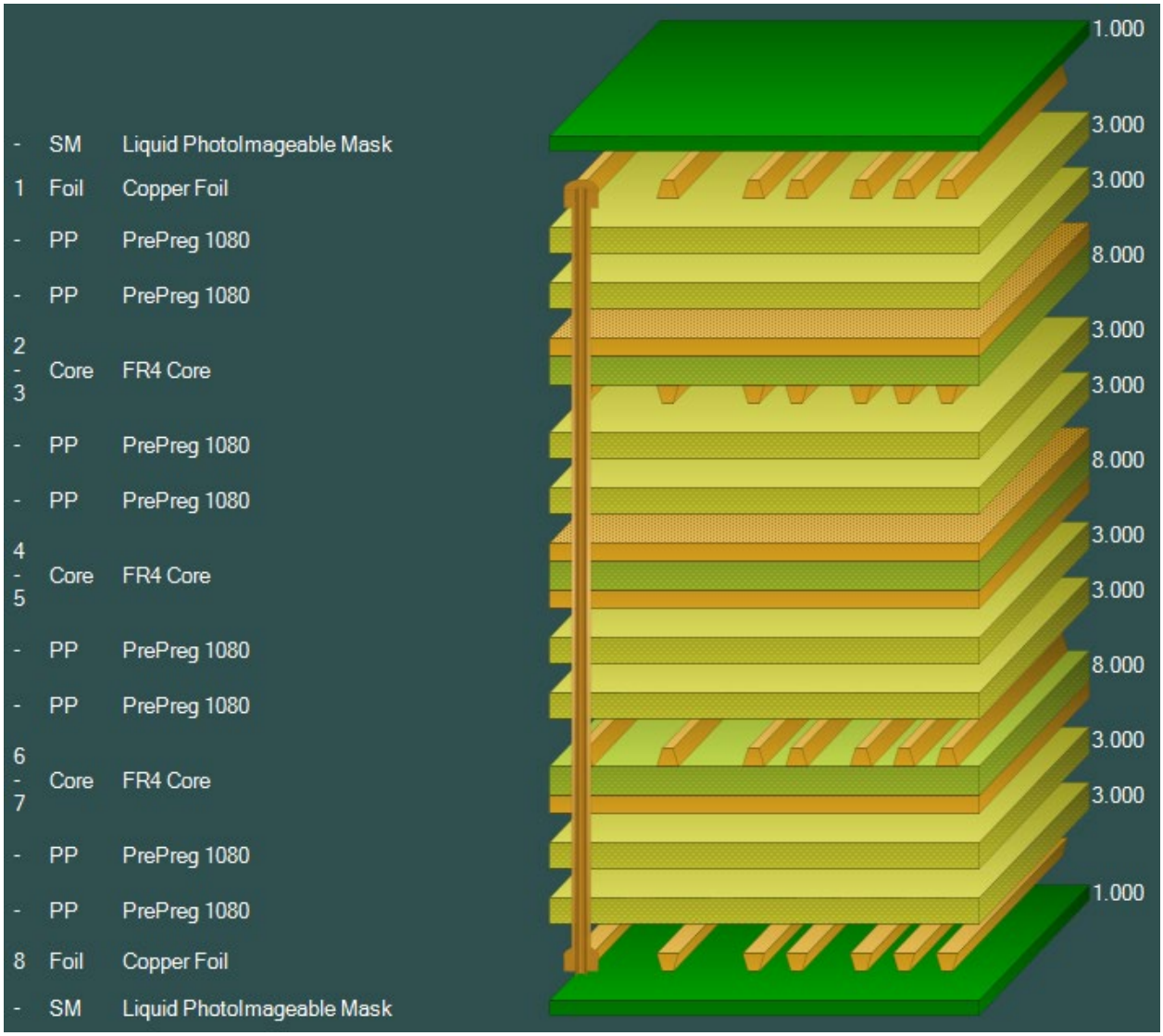
Adding drill information

To add a drill between electrical layer 1 and the last layer click the Through-Plated and Non-Through-Plated check boxes as required.

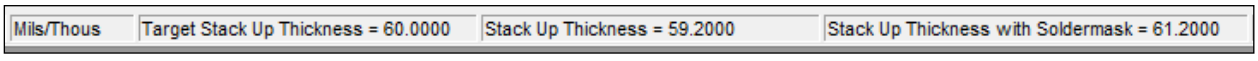


With all build options specified click Apply to complete the stackup. The finished stackup appears in the Editor window.

The example stack below includes two prepreg materials between layers.



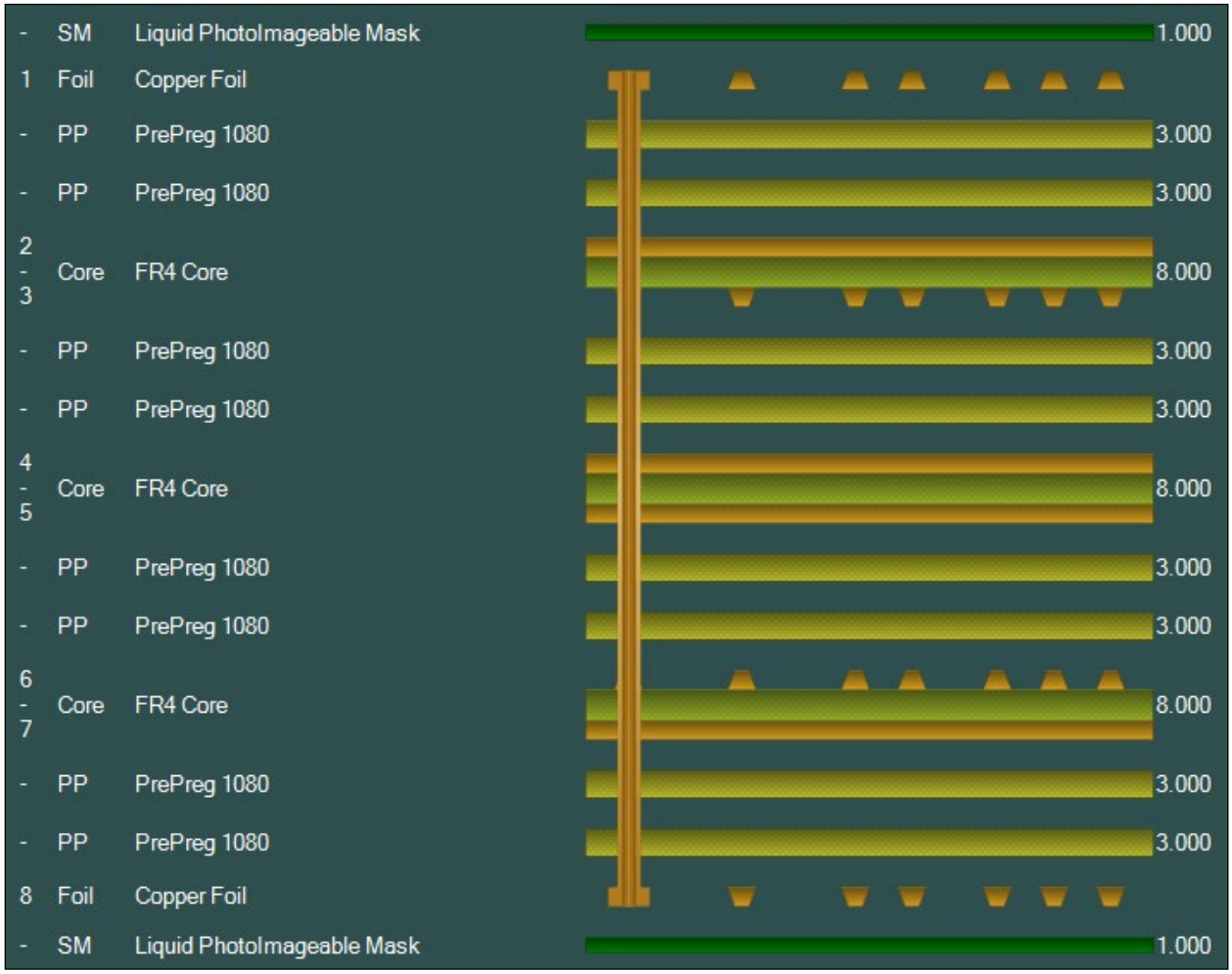
Summary information is shown in the Status Bar and includes the units in use, the target stackup thickness and the stackup thickness without and with soldermask.



See 2D View

Changing the stackup view

For many editing operations changes to the stack may be easier to visualize when shown two-dimensionally. Click the See 2D View button



Filtering Materials

When adding or swapping materials, available materials (foils, prepregs, etc.) are listed in the associated material library dialog.

Lists can be filtered for materials matching desired parameters (dielectric thickness, Er, etc.) See *Using Speedstack Materials Libraries*.

Saving stackups

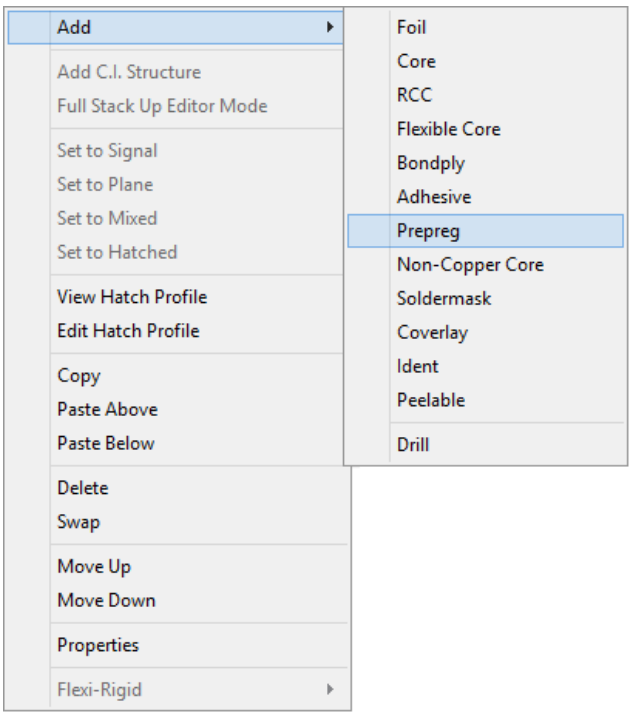
It is strongly recommended that users save work frequently and maintain safe backups of stackups and projects.

Creating stackups manually

Speedstack allows the designer to add or edit stackup layers in any order, from top to bottom, bottom to top or from the centre layer outwards. This example will create a four-layer stackup, starting at the centre core layer and adding layers above and below.

Editing the stack

When editing the stack it will probably be most convenient to right click an object in the stack and select the associated command from the context menu. The menu will reflect the commands available for the selected object — commands that are not appropriate for the object are greyed out.



Alternatively, select the object (copper, prepreg, core, etc.) with the left mouse button and choose the command from the Speedstack toolbar.

Adding layers to the stackup

Go To Materials Library

Items added to the stackup are added from the currently open materials library. Speedstack opens Program Files\Polar\Speedstack\default.mlbx if it exists; if a different library is required, open it via Go To Materials Library.

Note: Speedstack does not ship with the default.mlbx library.

For this discussion open one of the two sample library files, Speedstack Imperial.mlbx or Speedstack Metric.mlbx (stored in the Program Files\Polar\Speedstack\Samples folder at installation time for a default installation.)

Consistency of units

When defining dimensions for a stackup (for example, layer thicknesses) ensure that all measurements are defined using the same units (mils, mm, etc.) throughout the structure and its libraries.

Note: the libraries supplied for these examples are preloaded with sample data only.

Click the File|New command to clear the stackup screen and notes and information text areas.

Click the File|Save Stackup or Save Project command to save the stackup or project. Users are recommended to save stackups or projects frequently during the stackup creation process to avoid data loss. Stackup files, project files and library files should be backed up to a secure location.

Adding a core layer

Add Layer Material

Click the Add Layer Material button and choose Core…the Core library is displayed

The Core library contains full details of the core material, including base and finished thicknesses, dielectric constant, and upper and lower copper thicknesses.

Supplier Description	Description	Stock Number	Dielectric Base Thickness	Dielectric Finished Thickness	Dielectric Constant	Upper Cu Base Thickness	Lower Cu Base Thickne
CO/001	FR4 Core 2	400-001	2	2	4.2	0.7	0.7
CO/002	FR4 Core 2	400-002	2	2	4.2	1.4	1.4
CO/003	FR4 Core 2	400-003	2	2	4.2	2.8	2.8
CO/004	FR4 Core 3	400-004	3	3	4.2	0.7	0.7
CO/005	FR4 Core 3	400-005	3	3	4.2	1.4	1.4

Click on any of the column buttons to sort the library list by the selected column.

Add Material above

Choose a core type from the list of cores and click the Add Material Above button. The core is added to the stackup screen. When editing a stack this button adds a core above the selected layer.

Stackup core layer

Add Material below

Layers may also be added below the selected layer. The Add Material below button adds a core below the selected layer.

As each layer is added the stackup information table is updated to reflect the current status of the stackup.

Stack Up Information

Field	Value
Electrical Layer Count	8
Stack Up Cost	0.00
Copper Thickness	11.0236
Dielectric Thickness	51.9685
Solder Mask Thickness	1.9685
==========	==========
Target Stack Up Thickness	62.9921
Stack Up Thickness	62.9921
Stack Up Thickness with Soldermask	64.9606
==========	==========

Stackup information table

Note: The Stackup Information is printed in red when the stack thickness is outside its tolerance.

With the core selected, the Selected Item table displays the properties of the core.

Selected Item Information : Core

Field	Value
Upper Cu Base Thickness	35.00
Upper Cu Finished Thickness	35.00
Upper Copper Coverage	0
Minimum Trace Width	75.00
Data Filenames	
Dielectric Base Thickness	100.00
Dielectric Finished Thickness	100.00
Dielectric Constant	4.2
Loss Tangent	0.0195
Resin Content	53
Tg	180
Td	0
CAF Resistance	0
Z Axis Expansion	0
Excess Resin	0.00
Isolation Distance	100.00
Lower Cu Base Thickness	35.00
Lower Cu Finished Thickness	35.00
Lower Copper Coverage	0
Minimum Trace Width	75.00

Core layer information

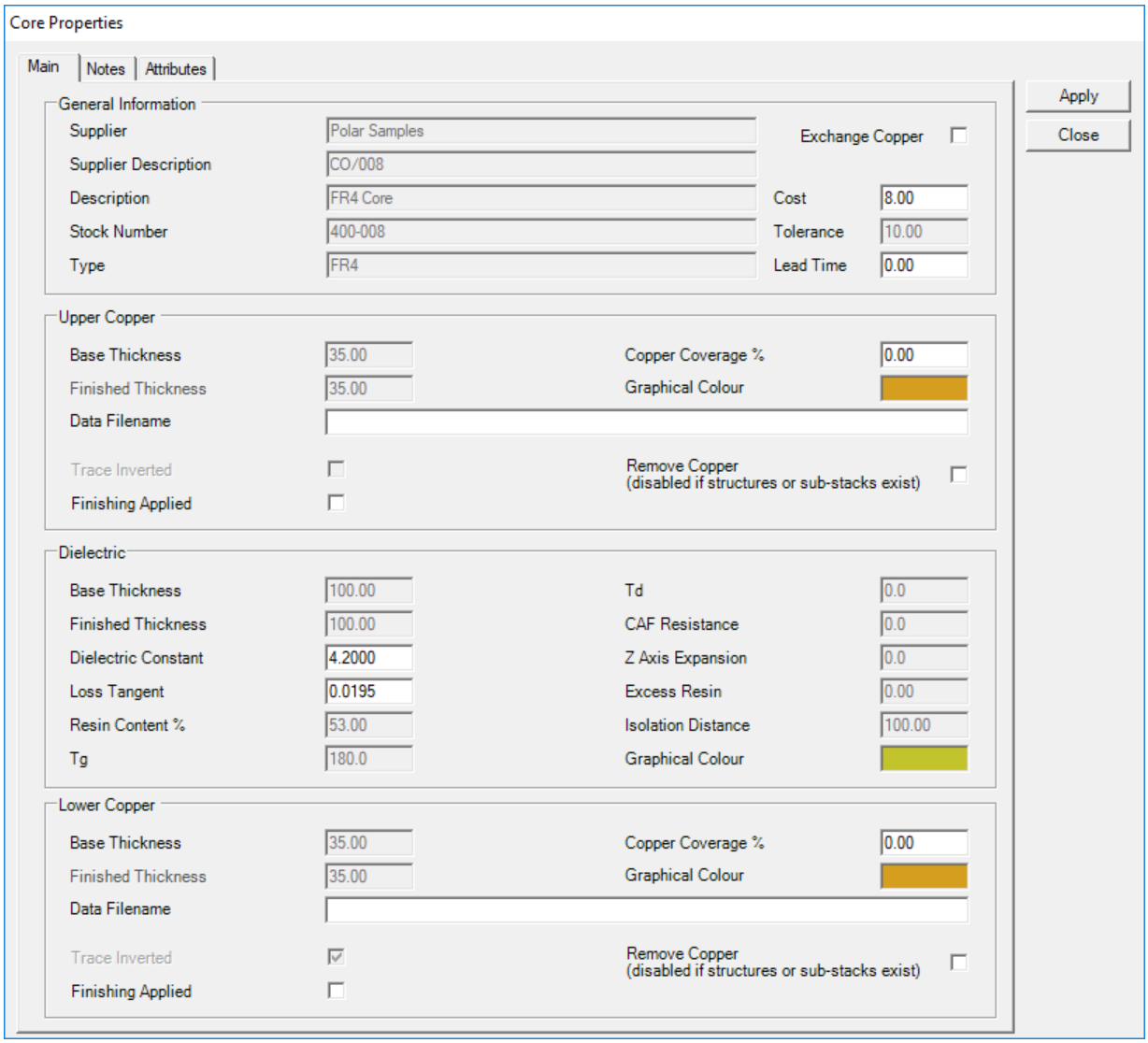
To observe the properties of any material, click the material in the stack and read off the properties in the Selected Item Information panel.

Editing the selected layer properties

To change the properties of the selected object (for example, to modify the dielectric constant or the value for the finished thickness of the dielectric), right click the object in the stackup and choose Properties from the shortcut menu; in this example the Core Properties dialog is displayed.

Note that the Enable Finishing setting in the Tools|Set Stackup Thickness/Finishing Options dialog must be unchecked to enable the Finishing Thickness to be specified manually.

Change the value to the corrected value and click Apply.



Adding data file names

If available, add the data file name(s) to the upper and lower copper layers and click Apply.

Close the dialog when all changes are completed.

Changes will be reflected in the Stackup Information table.

Changing a layer function

In this example both the signal layers above and below the core dielectric are changed to planes.

Set Layer to Plane

Click the lower signal layer and click the Set Layer Plane button. Repeat for the upper signal layer.

The changes are reflected in the stackup window

Exchanging layers

Swap Selected Material

To change just the core dielectric (leaving the copper layers unaffected), right click the core material (for example the FR4 in the graphic above) and choose Swap from the context menu or left click the core material and click the Swap Selected Material button. Choose the new core type from the library and click the Swap button. The layer properties will change to reflect the new material and changes appear in the Stackup Information table.

Adding prepreg layers

Add Material

With the core selected, click the Add Material button and choose Prepreg…; the Add Prepreg library is displayed.

Supplier	Supplier Description	Description	Stock Number	Dielectric Base Thickness	Dielectric Finished Thickne	Dielectric Constant	Loss Tangent	Resin Content
Polar Samples	PP/006	PrePreg 106	300-006	50	50	4.2	0.0195	60
Polar Samples	PP/001	PrePreg 1080	300-001	75	75	4.2	0.0195	60
Polar Samples	PP/004	PrePreg 1651	300-004	150	150	4.2	0.0195	47
Polar Samples	PP/002	PrePreg 3080	300-002	75	75	4.2	0.0195	60
Polar Samples	PP/003	PrePreg 3113	300-003	100	100	4.2	0.0195	53
Polar Samples	PP/005	PrePreg 7628	300-005	200	200	4.2	0.0195	45

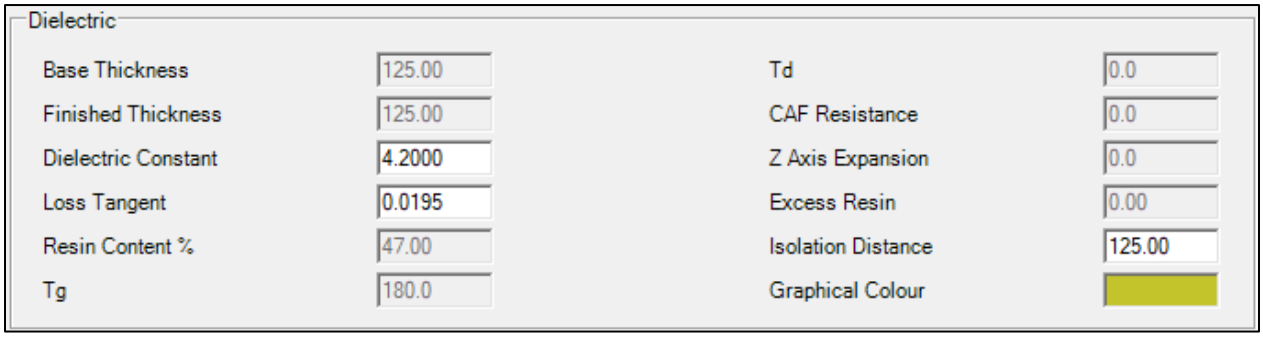
The Prepreg library contains details of the prepreg material, including base and finished thickness, dielectric constant and loss tangent, resin content and excess resin.

Add Material Above

Choose the Prepreg material from the database and click the Add Material Above button.

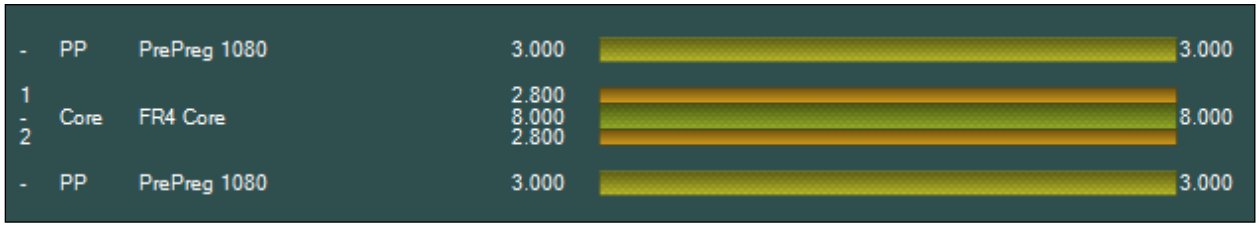
The prepreg layer is added above the core.

To change the properties of the prepreg material right-click the layer and choose Properties from the short cut menu. Items with a white background can be modified.



Add Prepreg Below

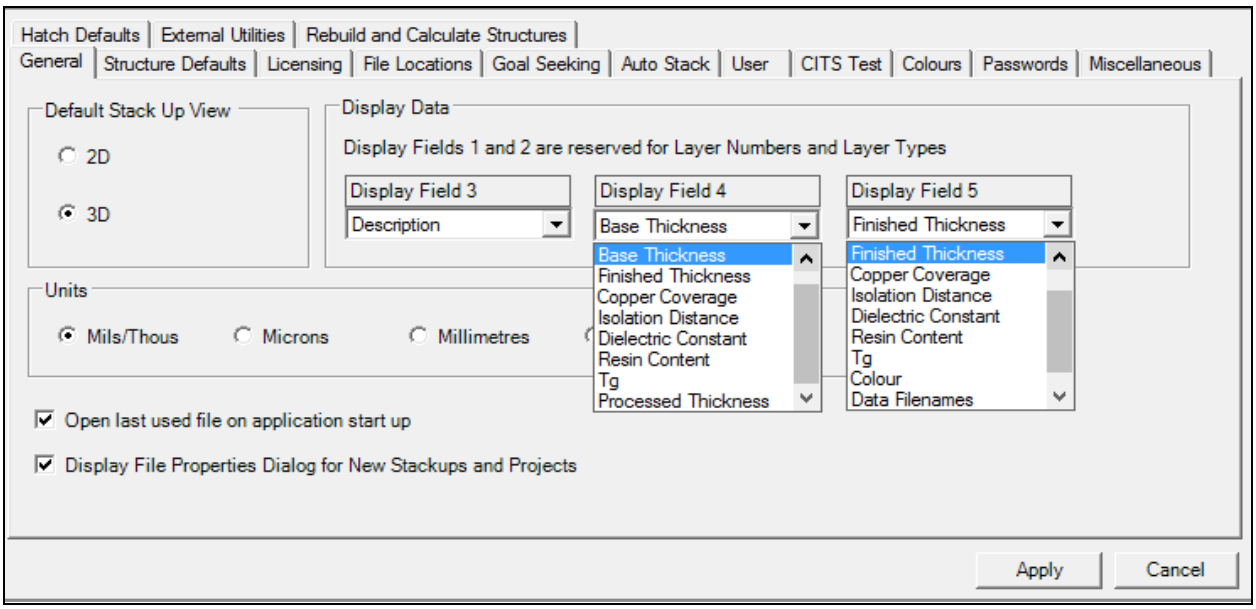
Select the Core material and click Add Material|Prepreg to display the prepreg library and click the Add Below button. The layer of prepreg is added below the core.



Modify the properties as necessary.

Choosing the Display Data fields

The Speedstack Stack Editor provides a range of useful data fields for optional display alongside each material. Base and Finish (Display Field 4) refer to thicknesses and weights and appear to the left of the stackup graphic.



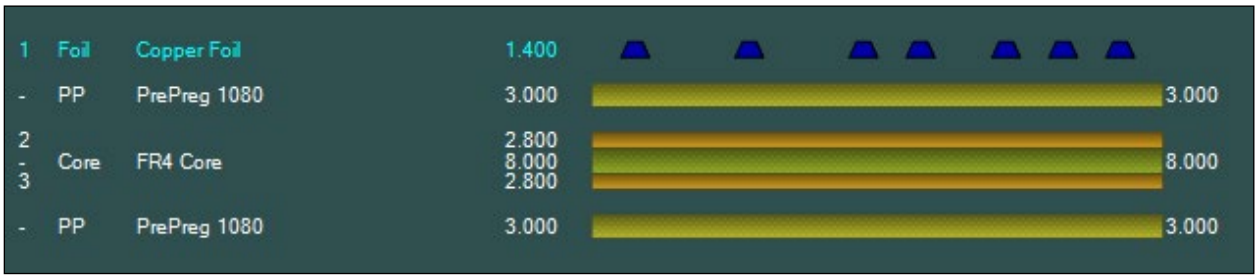
Display Field 5 appears to the right of the stackup graphic. Choose the data of interest from the drop down lists.
Note: Processed Thickness is the Finished Thickness for copper layers and Isolation Thickness for dielectric layers.

Adding a foil layer

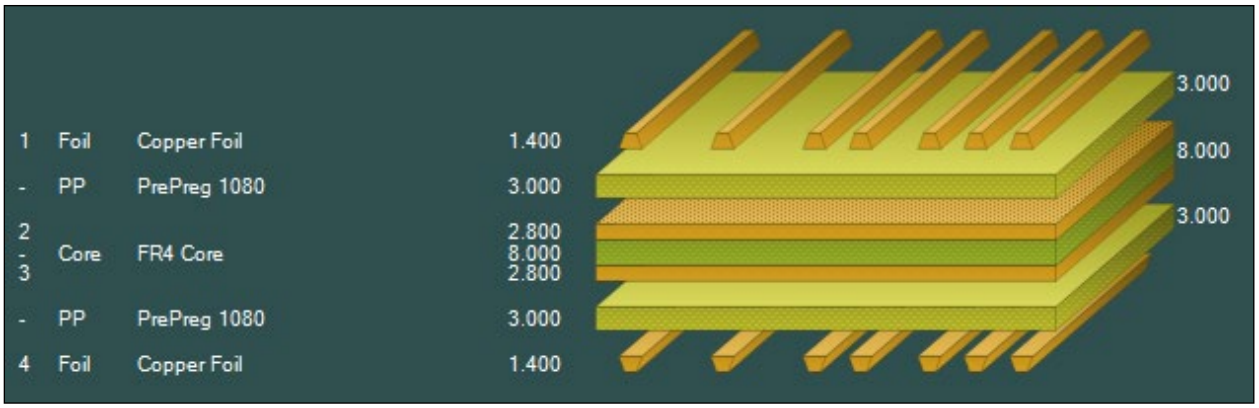
Select the upper layer of prepreg and click the Add Layer Material button and choose Foil to display the copper foil library.

Supplier Description	Description	Stock Number	Cu Base Thickness	Type	Cost	Lead Time
FO/001	Copper Foil	100-001	0.7	Copper	1	0
FO/002	Copper Foil	100-002	1.4	Copper	2	0
FO/003	Copper Foil	100-003	2.8	Copper	3	0

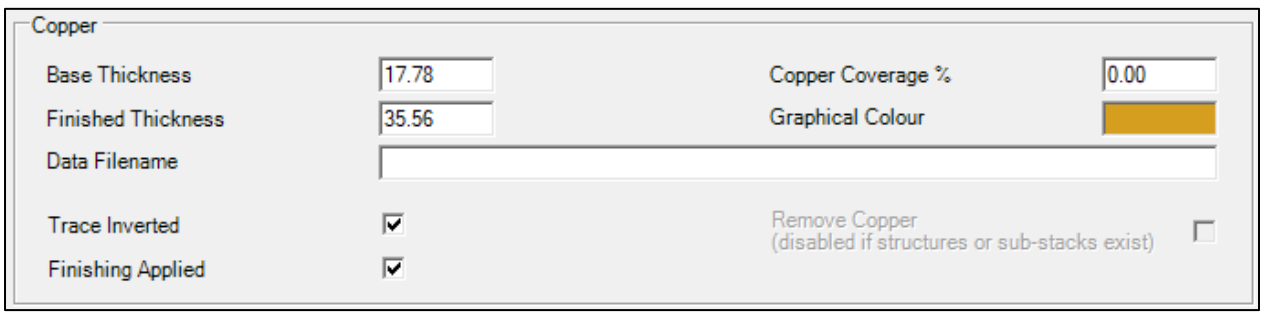
Choose the foil type and click Add Above, the copper foil layer is added above the selected prepreg layer.



Repeat the procedure for the lower prepreg layer: select the lower prepreg layer and add a layer of copper foil below the layer (shown below as layer 4 in the 3D view).



To alter the foil properties, right-click the foil layer and choose Properties. Using the Properties dialog the user can, for example, specify that the trace is shown inverted.

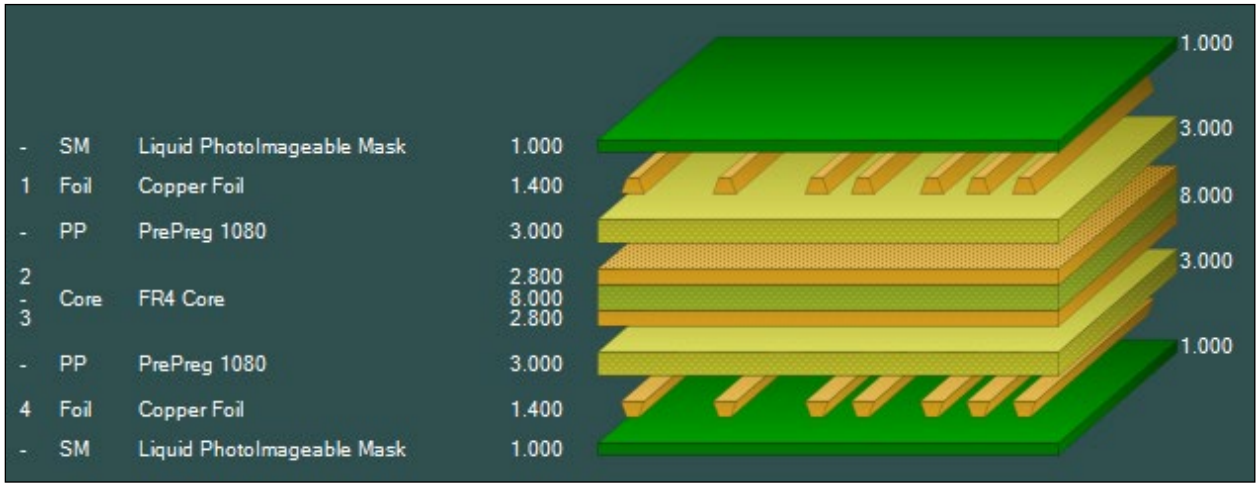


Note that the stackup is being built symmetrically about the centre layer.

Adding solder mask layers
With the upper layer of foil selected, click the Add Layer Material button and choose Soldermask to add a layer of LPI solder mask above the foil.

Supplier Description	Description	Stock Number	Mask Thickness	Dielectric Constant	Colour	Type	Cost
SM/001	Liquid Photolmageable Mask	500-001	1	4	Green	SolderMask	0.5
SM/002	Liquid Photolmageable Mask	500-002	1	4	Green	SolderMask	0.6
SM/003	Liquid Photolmageable Mask	500-003	1	4	Blue	SolderMask	0.6
SM/004	Liquid Photolmageable Mask	500-004	1	4	Red	SolderMask	1

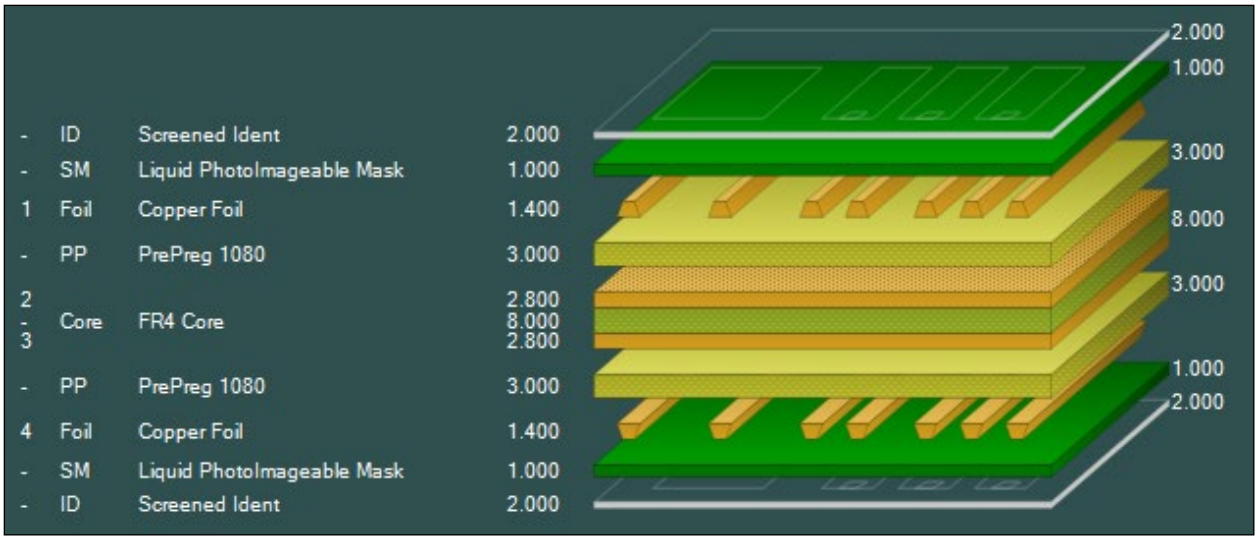
Repeat the process for the solder mask material below the lower foil layer.



Adding the Ident layers
Select the lower LPI Soldermask layer and click the Add Layer Material button and choose Ident to add a layer of Screened Ident below the layer. The sample Ident library includes ink thickness and colour

Supplier Description	Description	Stock Number	Ink Thickness	Colour	Type	Cost
ID/001	Screened Ident	600-001	2	White	Ident	0.1
ID/002	Screened Ident	600-002	2	Yellow	Ident	0.1
ID/003	Screened Ident	600-003	2	Black	Ident	0.1

Repeat for the upper layer.



AddDrill

Adding a drill

To add a drill between layers click the Add Drill button; the Add Drill dialog is displayed.

Drill information is stored in columns. Select the column in which to place the drill. Choose the first and second electrical layer numbers (layers 1 and 4 in the example).

Specify the drill type, mechanical or laser and whether through plated.

Note that with laser drills the order of drill layers is important, e.g. layer 1 and 4 is different from layer 4 and 1.

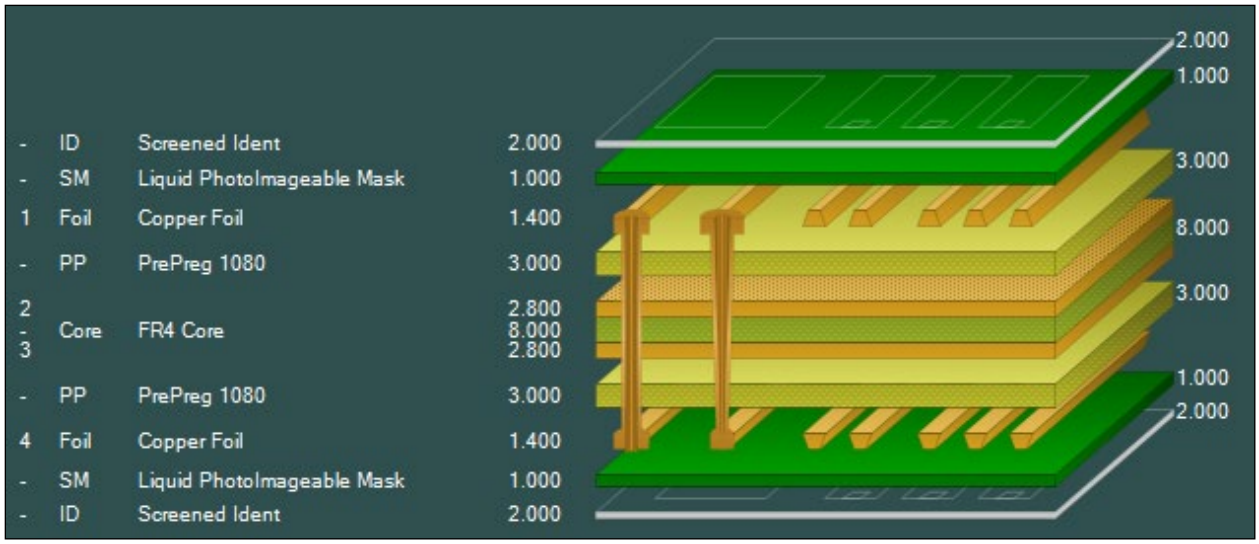
Choose the Fill Type from the dropdown list of fills.

Optionally, add the NC drill data filenames.

Optionally, add the hole count, number of different hole sizes and the minimum hole size. Click Add and close the dialog. The drill information is added to the stackup. The example below contains through plated and laser drill information.

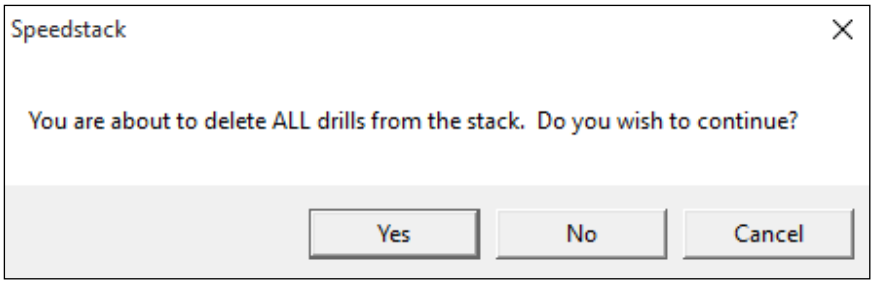
Note: The drill properties (i.e. Drill Information and Hole Information) are retained between each Add Drill operation. This can speed up the process of adding drills, especially when multiple drills of the same type are being added to the stackup.

The finished stackup is shown below



Deleting drills

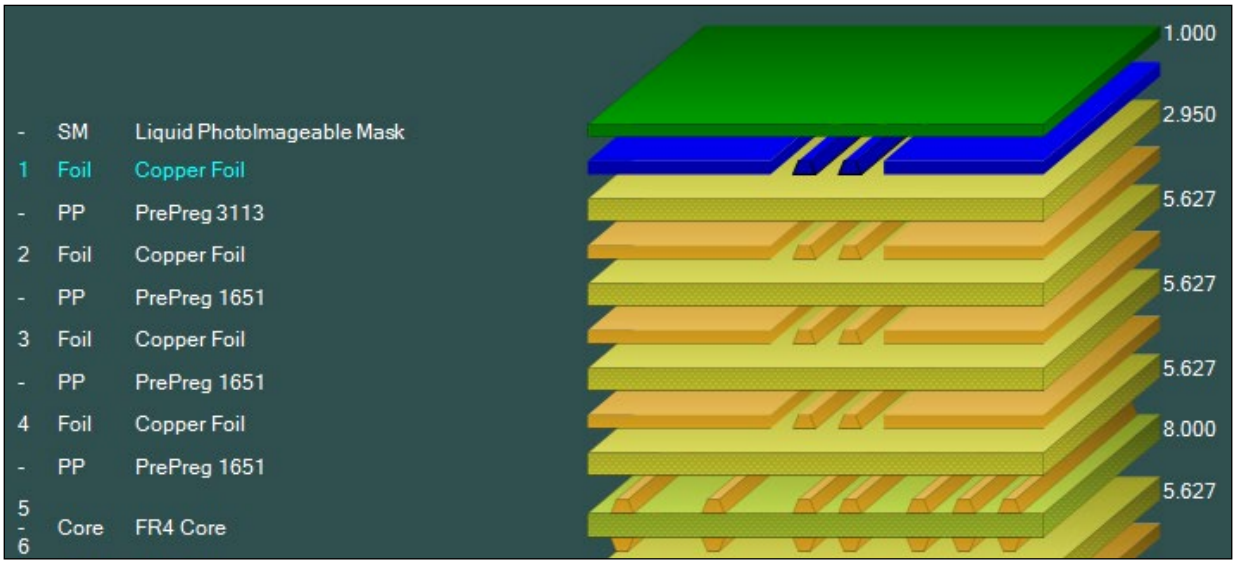
To delete a drill right click the drill and from the context menu choose Delete. To delete all drills choose Delete all Drills – confirm via the dialog below.



All drills will be cleared from the stack.

Adding stack vias

Speedstack can add stack vias to the stackup in a single operation. To add stack vias between layers 1 and 5 in the stackup below, select layer 1 and click Add Drill.



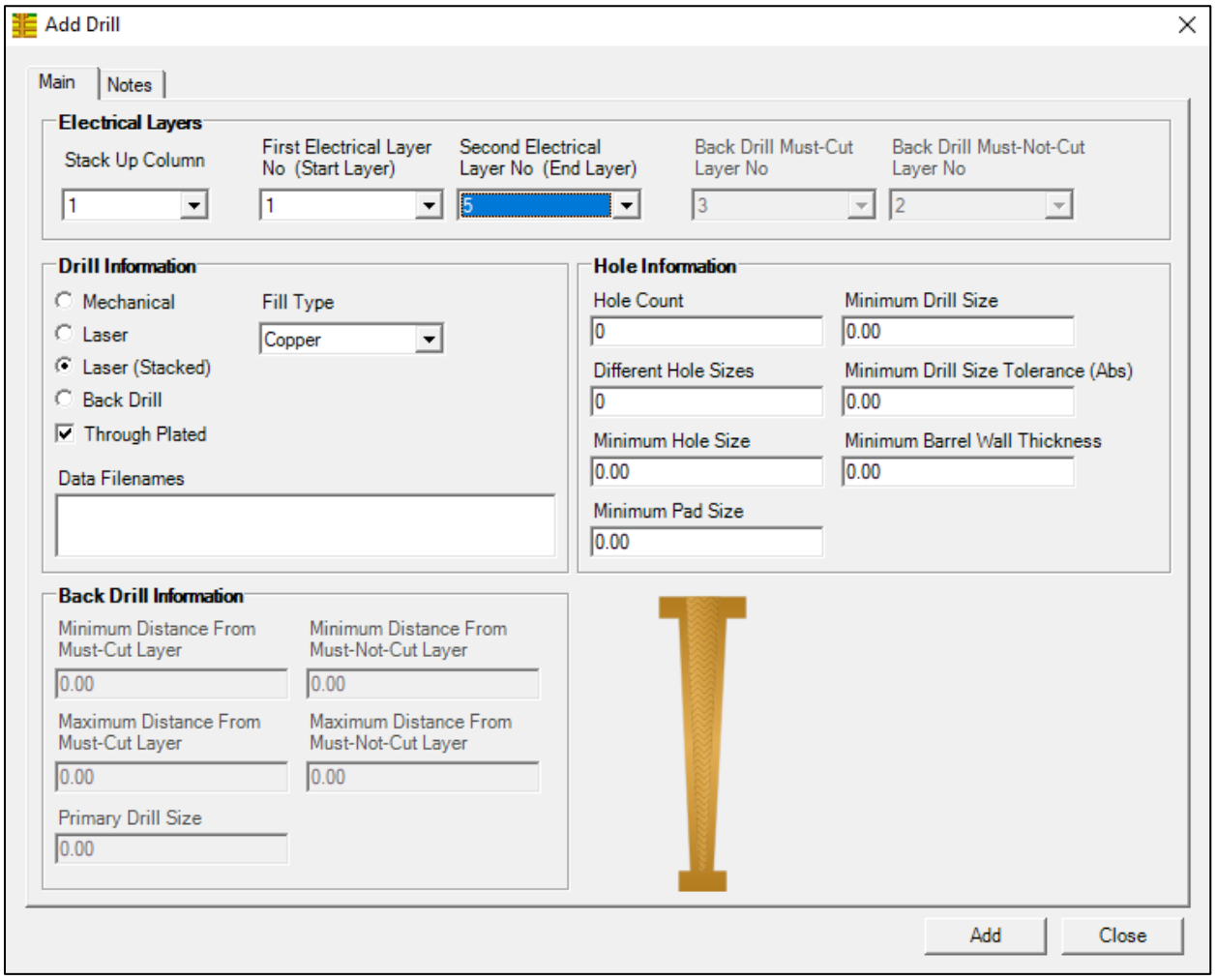
Specify the column number – (Column 1)

Specify the electrical layers (Layers 1 and 5)

Choose Laser (Stacked)

From the Fill Type drop down list choose Copper.

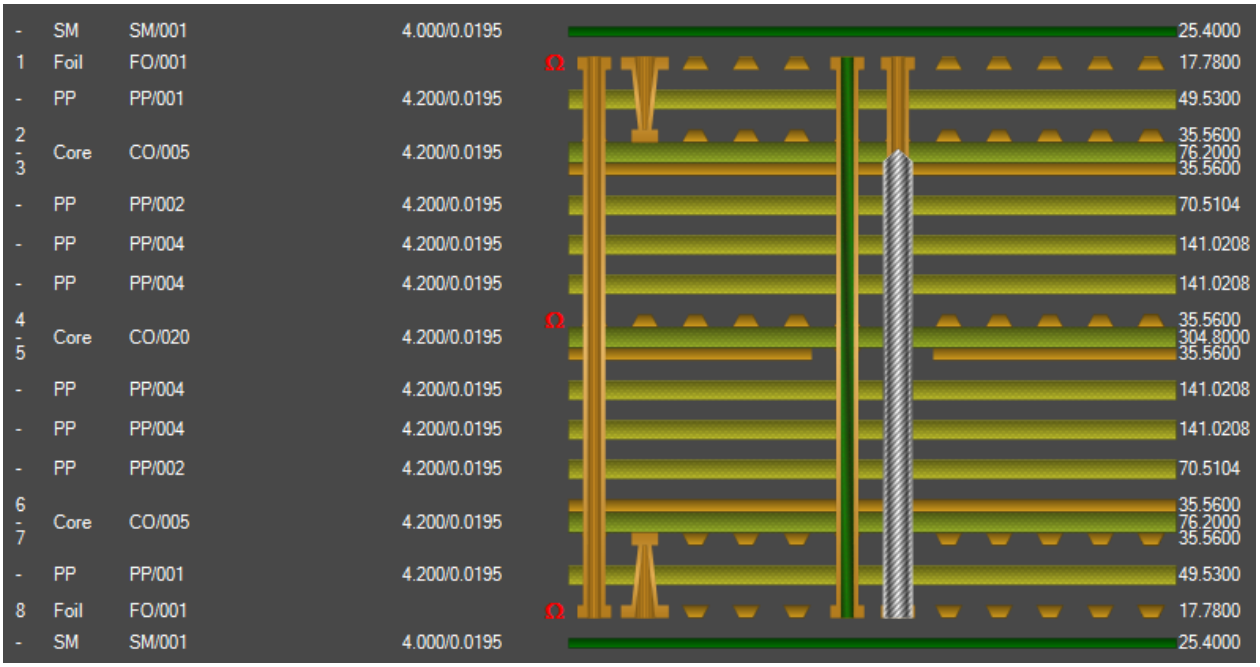
Click Add.



The stack vias are added to the stack (below.)

Via stub removal (controlled depth drilling / back drilling)

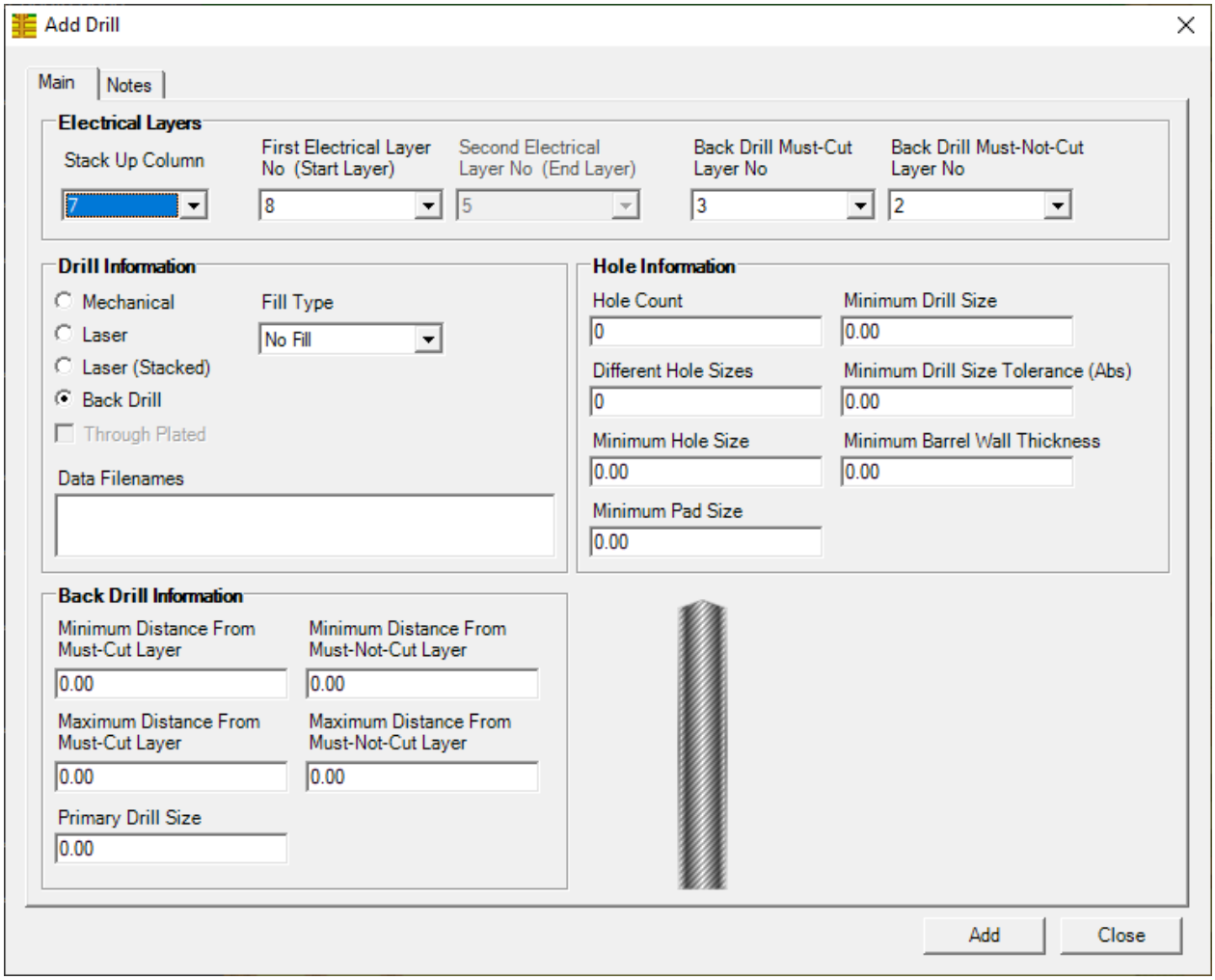
PCB vias provide a conductive path to allow the transition of electrical signals between circuit layers through the walls of plated holes. The most common method of connecting two signal layers is to create a plated through hole through the entire board and then remove the unwanted portion of the plated through hole (the stub – the unused portions of via extending further than the last connected inner layer) by back drilling. Stubs can lead to reflections, discontinuity errors that become critical with increasing propagation speed.) The stackup below shows a plated through hole back drilled, resulting in a via between layers 1 and 2.



Specifying back drills

Add Drill

To add a back drill click Add Drill to display the Add Drill dialog.



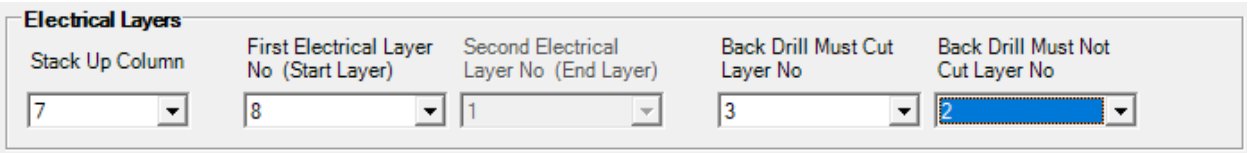
To specify the controlled drilling depth, from the Add Drill dialog:

Choose Back Drill from the Drill Information

Choose the drill column and specify the start layer.

Choose the layer number from the Back Drill Must Cut Layer No.

Choose the layer number from Back drill Must Not Cut Layer No.



Specifying back drill information

Many drill machines are capable of modifying drill depth to accommodate inner layer thickness variations. The Back Drill

Information fields allow designers and suitably equipped board shops to specify controlled stub lengths.

Use the Back Drill Information fields to specify the Minimum and Maximum Distances from Must-Cut Layer and Minimum and Maximum Distances from Must-Not-Cut Layer.

Adding notes

Click the Notes tab and click Add to supply descriptive and explanatory notes.

Deleting a layer

To remove a layer from the stackup select the layer and click the Delete button.

Delete Selected Material

Copying a layer

With layers defined it will often be found more convenient to copy an existing layer and paste it into the stackup than to create a new layer “from scratch”.

Copy Selected Material

Select the layer to be copied and click the Copy Selected Material button.

Click the layer nearest the destination location and choose Paste Above or Paste Below as appropriate

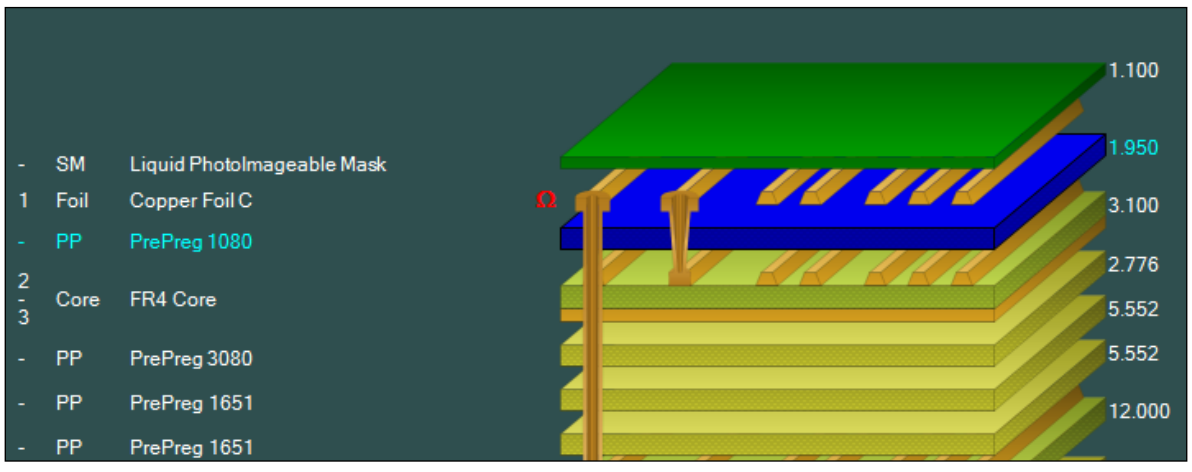
Note: when modifying the stackup it may be necessary to redefine the drill information to reflect the changes.

Copying material properties

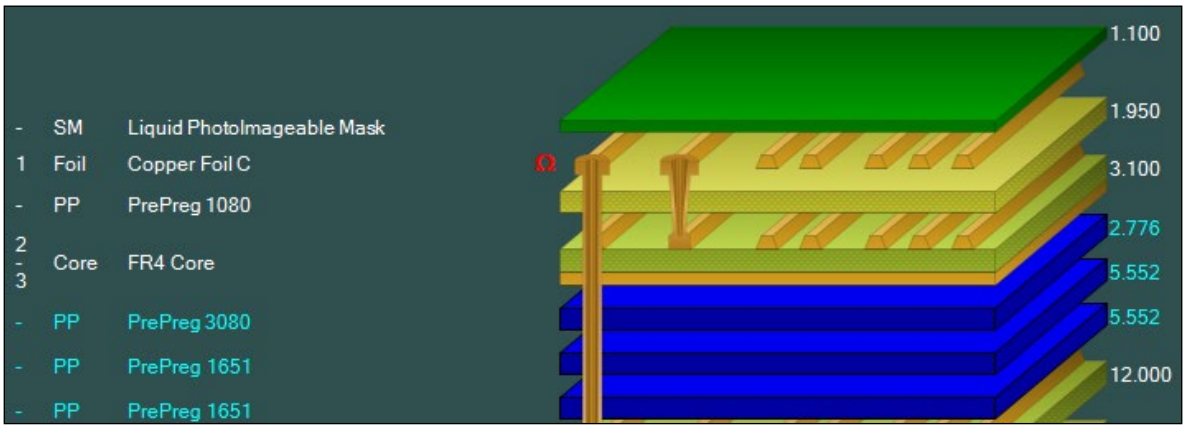
Speedstack can copy material properties from one material in the stackup and paste them onto multiple materials simultaneously.

Copy Material Properties

For example, to replace the three prepreg materials below Layer 3 in the stackup below with the Layer 1 material, PrePreg 1080, select the source material (shown highlighted below) and click Copy Material Properties

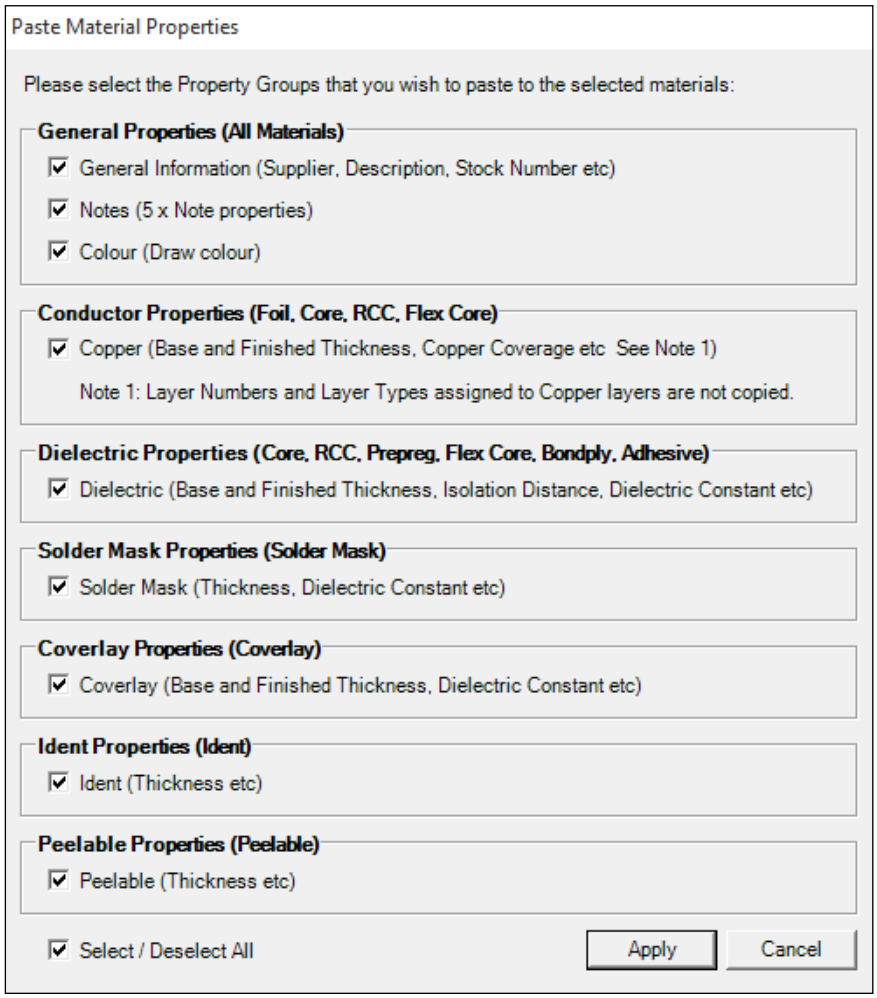


Select the three target layers

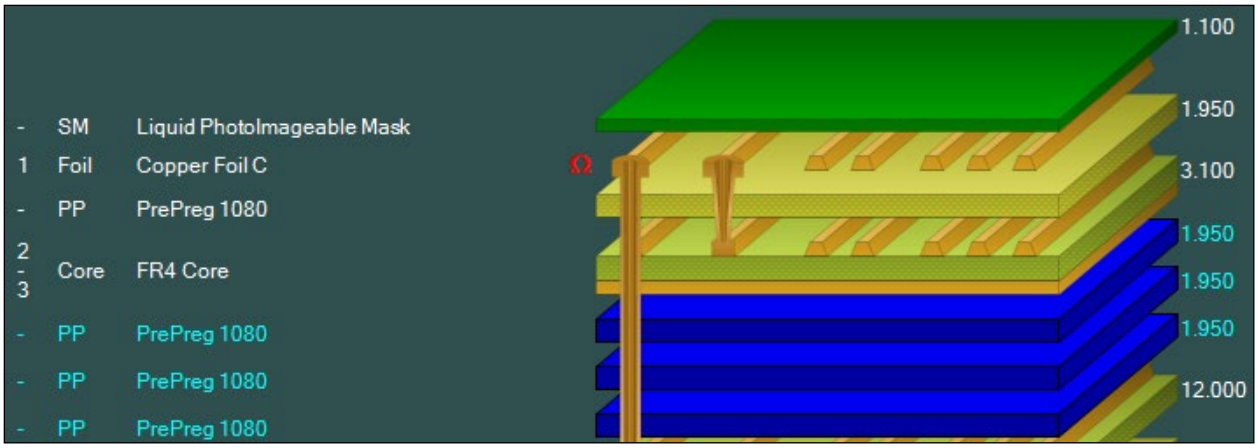


Paste Material Properties

Click Paste Material Properties – the Paste Material Properties dialog is displayed.



Select the property groups that are to be applied to the target materials and click Apply. Properties that do not apply for a material type are ignored.



In this example all material properties have been applied to the three target materials.

Note: When changing multiple materials simultaneously it is important to review the resulting stackup.

It will probably be necessary to recalculate any associated controlled impedance structures, especially if dielectric height and copper thickness parameters have changed.

Moving materials

To move materials within the stackup click Move Selected Material Up and Move Selected Material Down.

When a material is moved it is exchanged with the layer above or below, respectively.

Move Selected Material Up

Move Selected Material Down

Applying finishing

To apply the finished thickness factor throughout the board, click the Apply Finishing button with no material selected.

To reset the finished thickness back to the original base thickness of the materials throughout the board, click the Reset Finishing button with no material selected.

Note: when applying or resetting finishing, if a material is selected it will be necessary to specify whether finishing is to be applied to the selected material only or the whole stack.

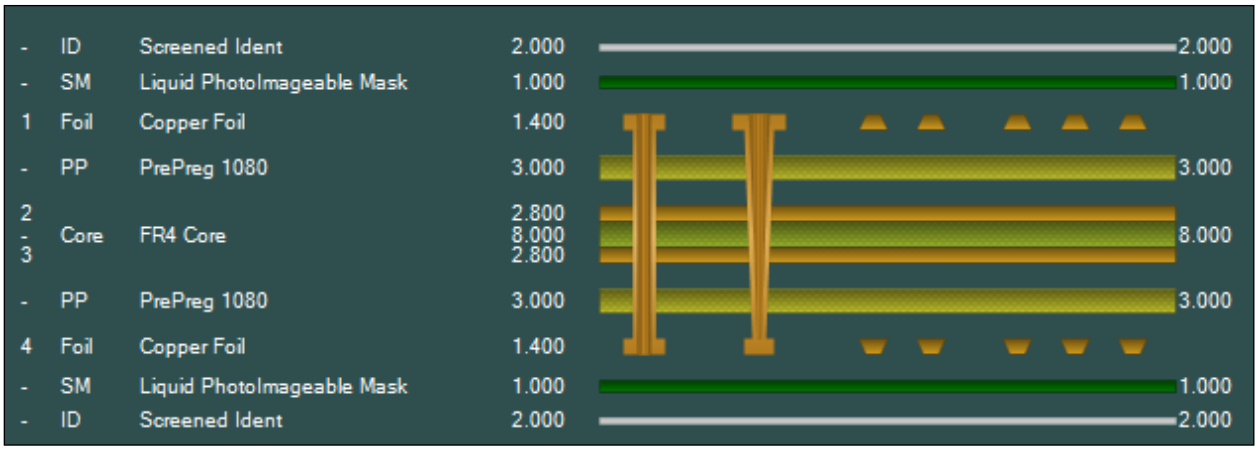
Apply Finishing

Reset Finishing

Displaying the stackup in 2-dimensional view

See 2D View

To change the view of the stackup from its default 3-dimensional aspect, click the See 2D View button. The stackup is displayed in 2-dimensional view.



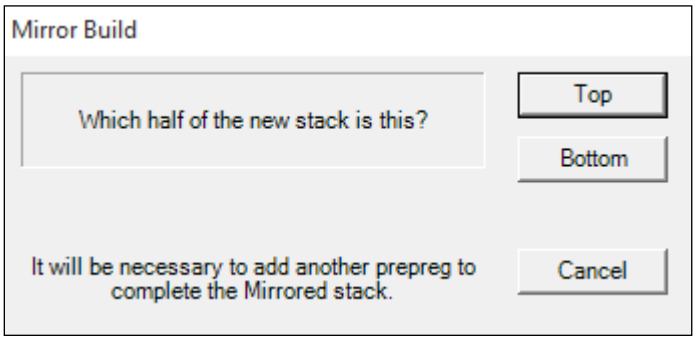
See 3D View

Click the View 3D button to restore the 3 dimensional view.

Mirror Builds

Mirror Build allows the designer to consider the stack in two halves, designing and building, for example, just the top half and mirroring the structure into the lower half.

Build the top half of the stack, including any controlled impedance structures and click the Mirror Build button; specify whether the current set of layers is the upper or lower half of the stack. To maintain symmetry, Speedstack will add a layer of material as appropriate to the stack;



the stack is reflected symmetrically into the lower half.

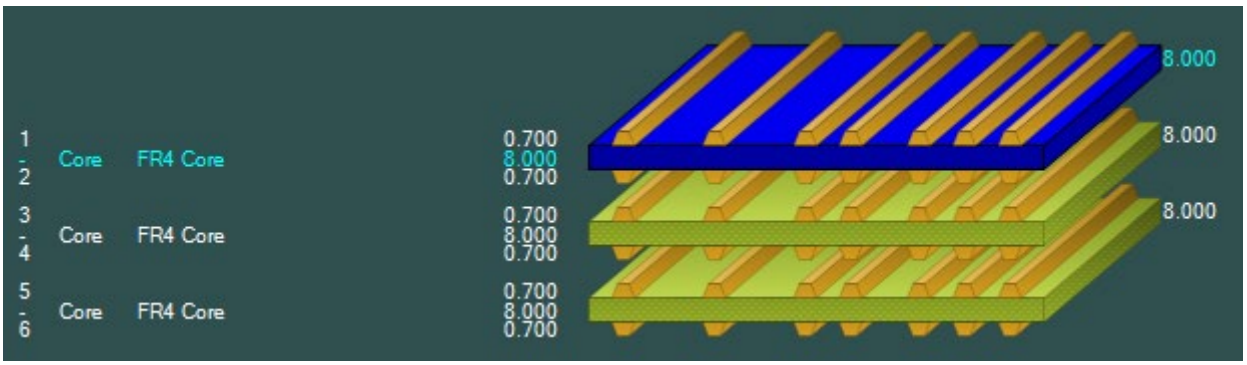
Symmetrical Builds

In Symmetrical Build mode the Speedstack maintains stack symmetry as the stack designer creates or edits a stack. Changes in one half of the stack are reflected in the opposite half of the stack to ensure a symmetrical stack.

This example considers an 8-layer stack – beginning with three cores and then using Symmetrical Build.

Creating a new stack

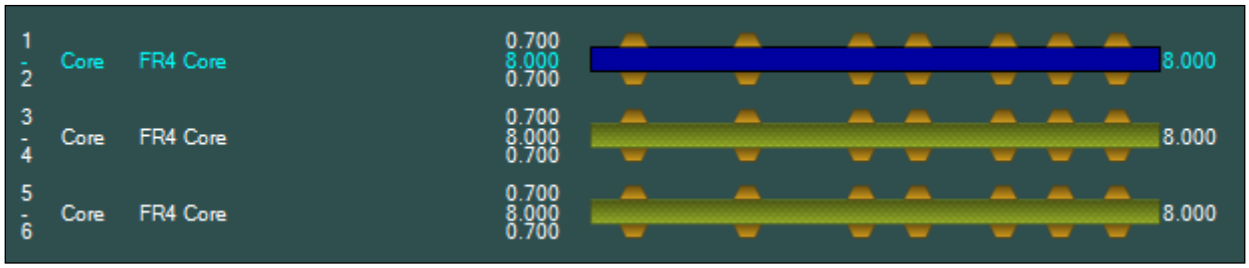
Create a new empty stackup and add three cores.



When constructing complex structures it will often be found easier to use the two dimensional aspect.

View 2D button

To change the view of the stackup from its default 3-dimensional aspect, click the See 2D View button. The stackup is displayed in 2-dimensional aspect.



Adding a prepreg layer in Symmetrical Mode

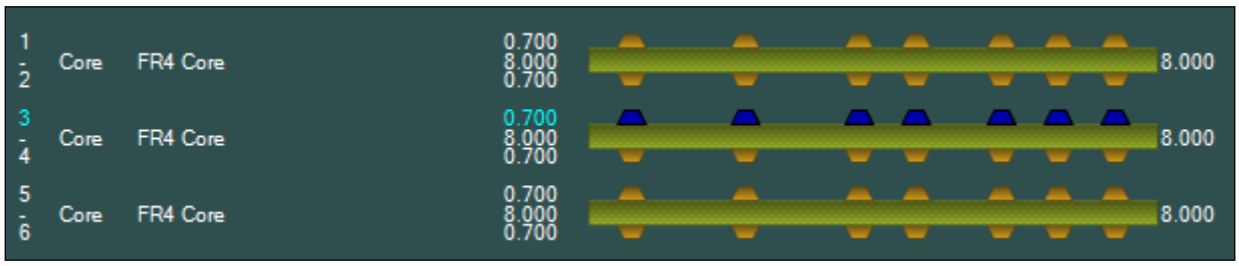
In this example it is necessary to add prepreg layers between cores to achieve the required dimensions.

Symmetrical OFF

Symmetrical ON

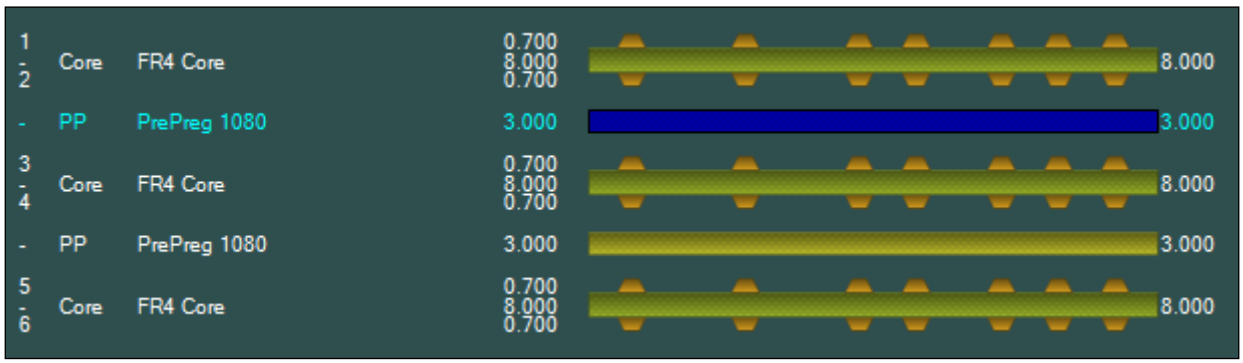
Switch to Symmetrical Mode and work in the top half of the stack – in Symmetrical Mode as layers are added to the top half of the stackup the Speedstack will add layers to the lower half of the stackup to maintain stack symmetry.

To add a layer of prepreg between Layers 2 and 3 select Layer 3 (the selected layer is shown highlighted in the figure below.)



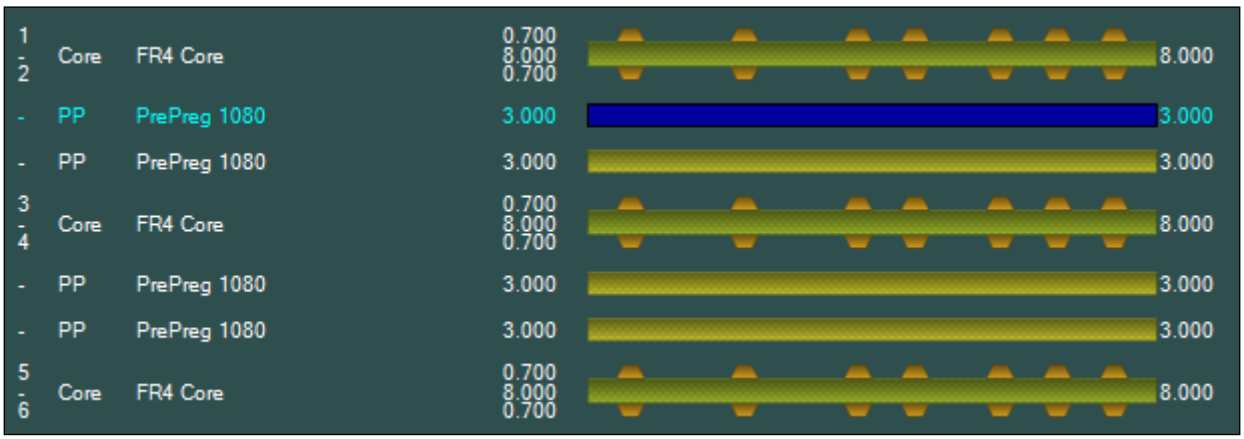
Click the Add Material button and add a layer of prepreg above Layer 3 (shown highlighted in the figure below).

In Speedstack's symmetrical mode the prepreg layer is automatically reflected in the lower half of the structure.



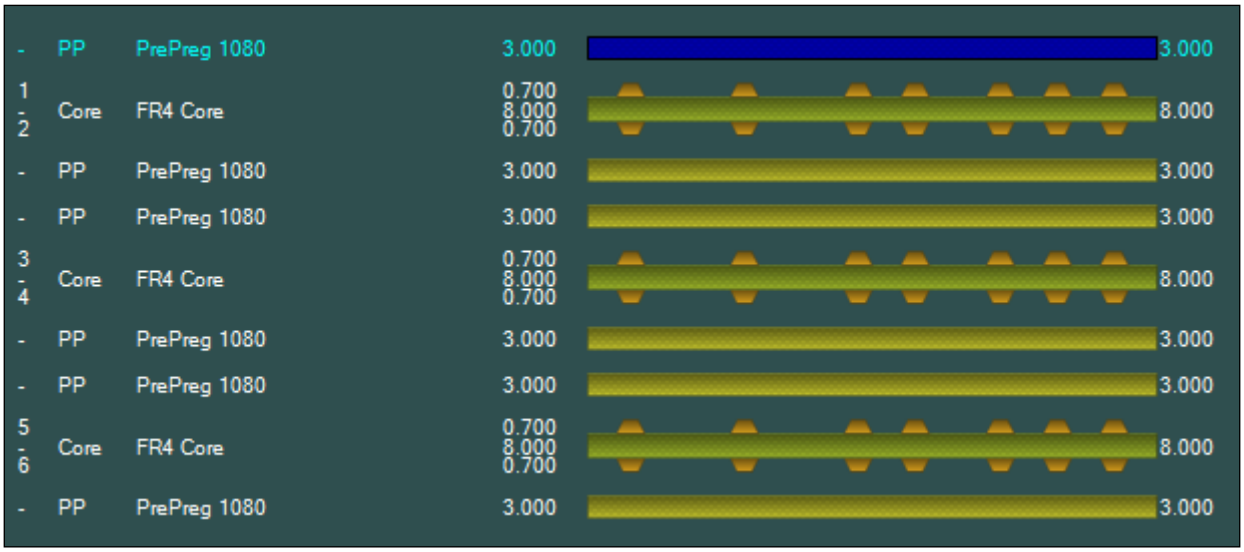
Adding a second prepreg layer

Now add a second layer of PrePreg 1080 above the layer just added; the new prepreg layer is reflected in the lower half of the stack as shown below.



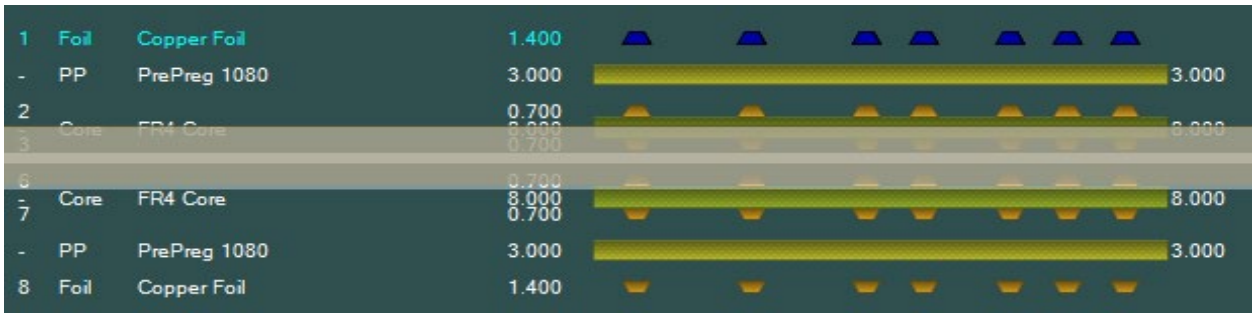
Next, add a layer of prepreg above layer L1 in the upper half of the stackup.

Speedstack in symmetrical mode automatically maintains stack balance by adding the corresponding layer below L6.

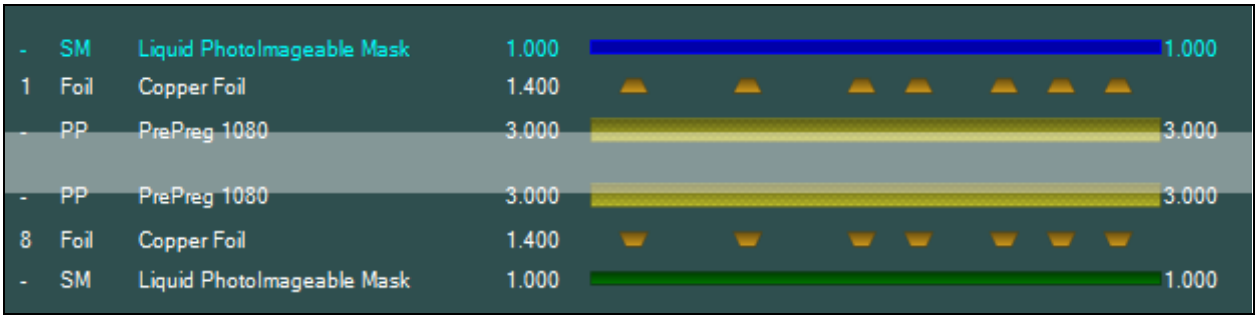


Adding foil, LPI Mask and Ident layers

Next, add a foil layer (L1 below) which is mirrored as L8; as part of the process Speedstack inverts layer L8.

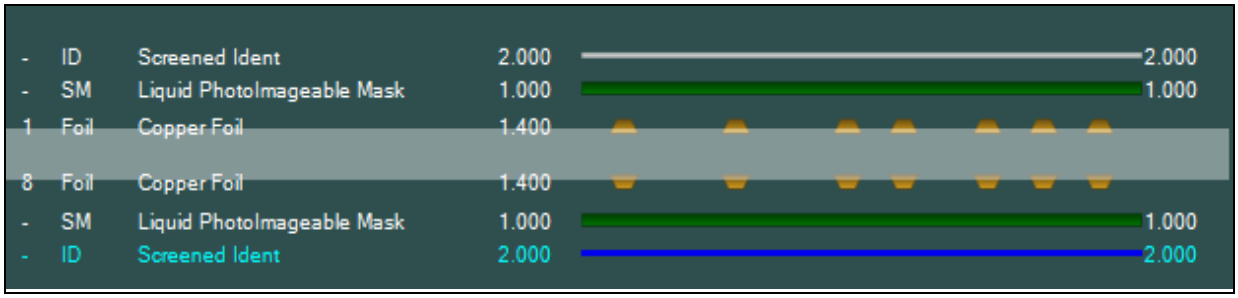


Next, LPI solder mask is applied to the top side of the stackup and reflected on the bottom side.



Ident layers (which are not considered components of electrical symmetry) will not be automatically reflected by Speedstack as they are added and must be applied separately to each side of the board.

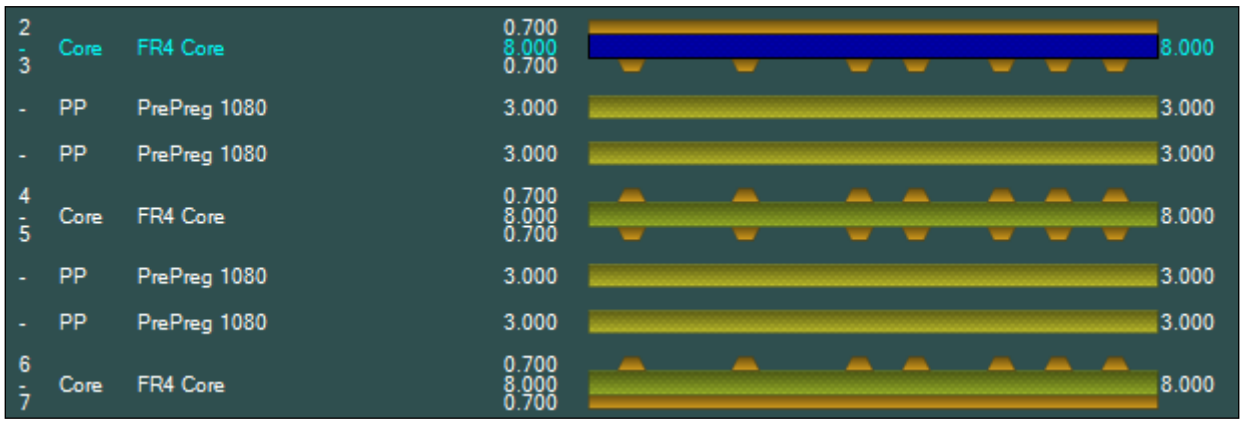
Select the upper solder mask and add an Ident material above; select the lower solder mask and add an Ident material below.



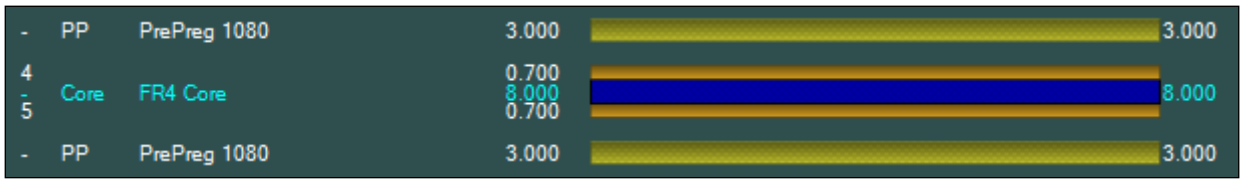
Assigning ground planes

Set Layer To Plane

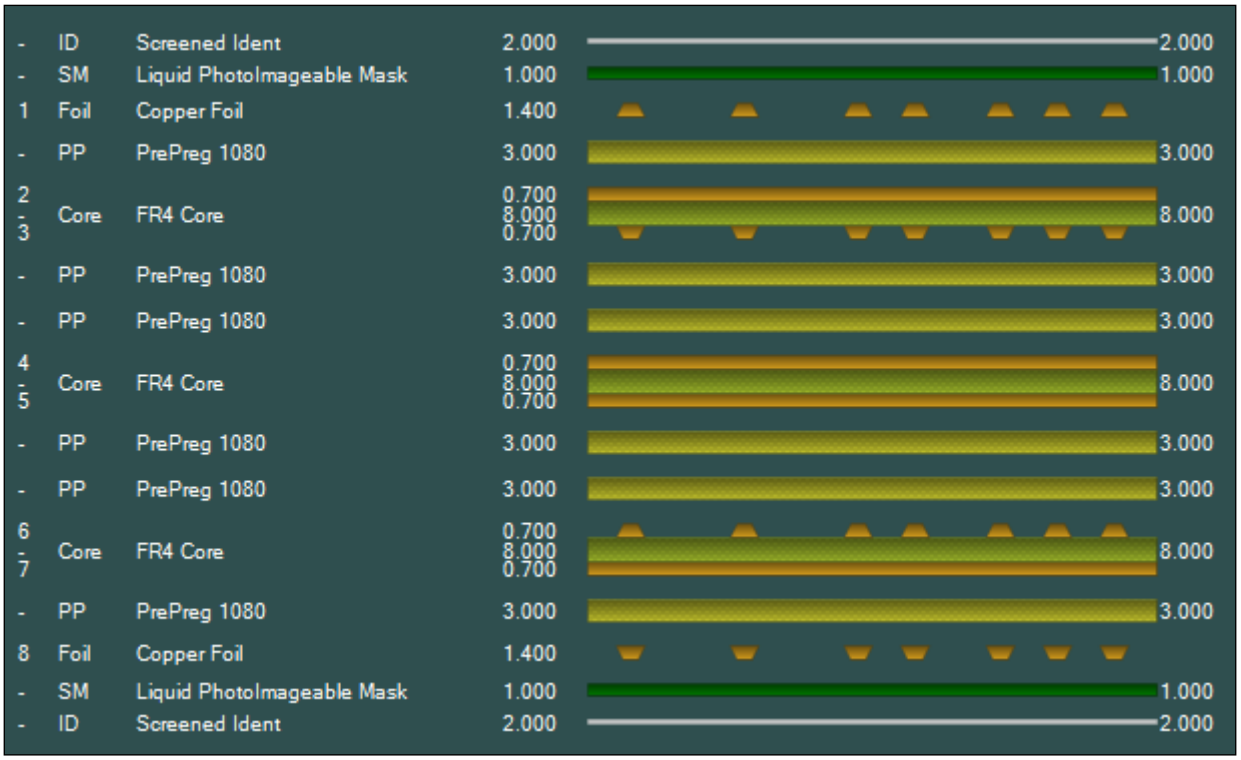
With all the material in place, assign ground planes; begin with layer L2 – it's reflected in layer L7. Right click the copper (L2) in the top core and choose Set Layer to Plane.



Repeat the process for the other ground plane layers; layer L4 is designated a ground plane, the change is reflected in L5 in the lower half of the stack.



The completed stack is shown below



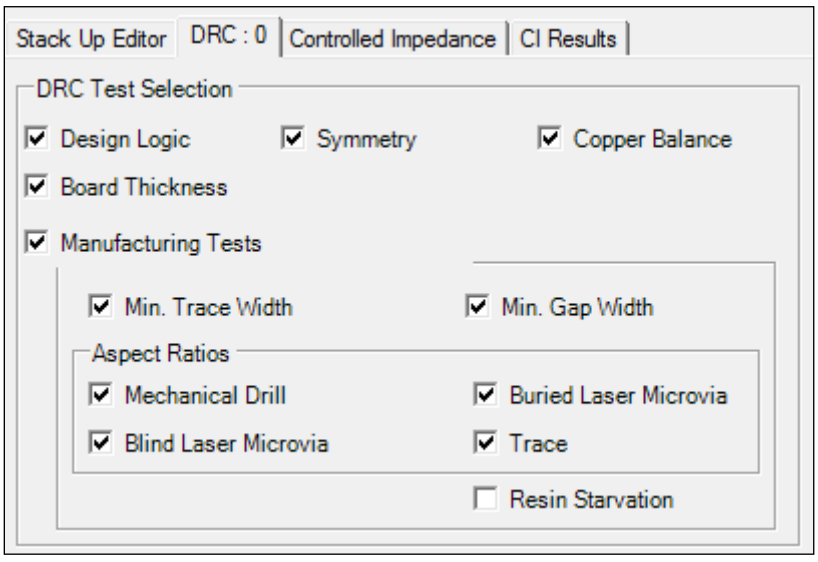
Design rule checking

Speedstack includes facilities to check for errors in stackup design, such as layers placed in invalid order or asymmetrical structures. The condition of the design rule checkboxes is carried over from session to session.

The Design Rule Checker (DRC) displays results in the DRC dialog. As each design rule is broken the Speedstack increments the error count on the DRC tab.

Viewing design rule errors

Click the DRC tab to view errors.



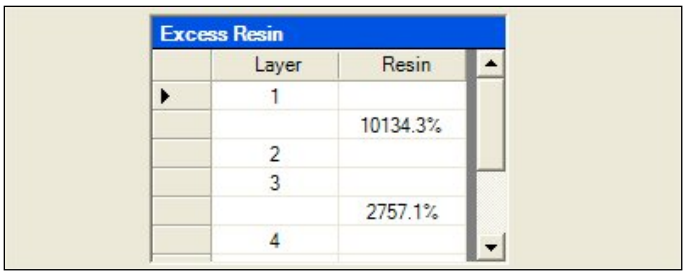
The Design Rule Checker checks include checking for:

- Two adjacent copper layers
- Resin coated copper on internal layer
- External prepreg layers
- Internal solder mask material
- Internal ident material
- Internal peelable mask
- Symmetry – different material types
- Copper not balanced
- Board thickness (if the board is outside tolerance the Stack Information in the Stack editor is displayed in red)

Manufacturing tests

- Minimum trace width (the test is carried out when calculating controlled impedance)
- Minimum trace separation (the test is carried out when calculating controlled impedance)
- Drill aspect ratios for plated holes
- Track aspect ratio
- Excess resin test (Resin Starvation)

If the Resin Starvation check box is ticked values are shown as below; scroll through the layers as required

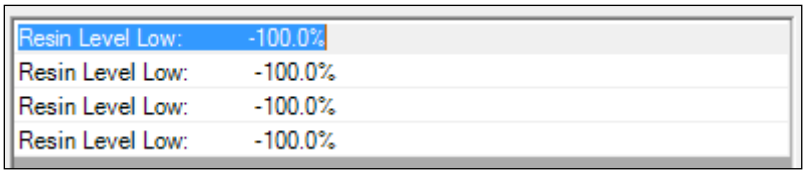


Note: If the Resin Starvation check box is ticked, all prepregs must include valid values for the excess resin field.

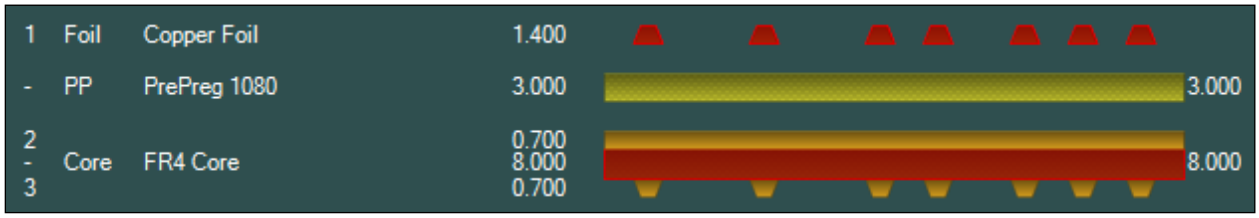
Polar Application Note AP509 includes a discussion on calculating excess resin.

Users can choose to display all errors or to select from a combination of design errors, symmetry errors and copper balance errors, etc.; check the boxes as required.

Click on the errors shown in the list to highlight the errors in the stackup screen.



Errors are highlighted in red.



Correcting design rule errors

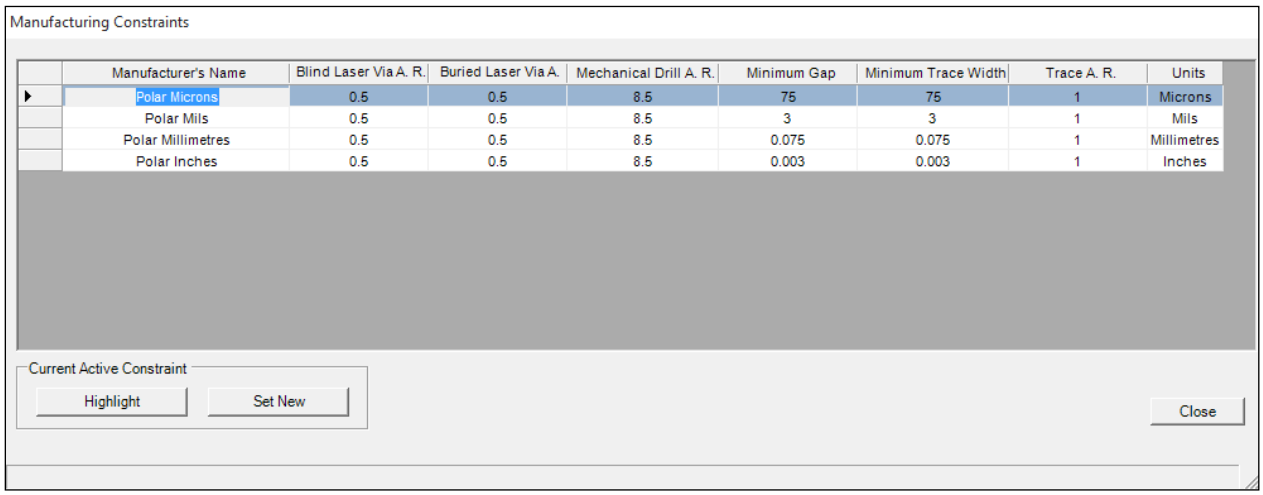
Users are strongly recommended to work through and correct errors in the order in which the errors are listed. Note that clearing each error may clear other errors in the process.

Manufacturing tests should be fixed before sending the PCB for manufacture. Hole sizes should be adjusted to comply. Failures with track and gap should be corrected, possibly by changing prepreg thickness and/or dielectric constants.

A collection of manufacturing constraints can be defined and the required one selected.

Creating and using manufacturing constraints

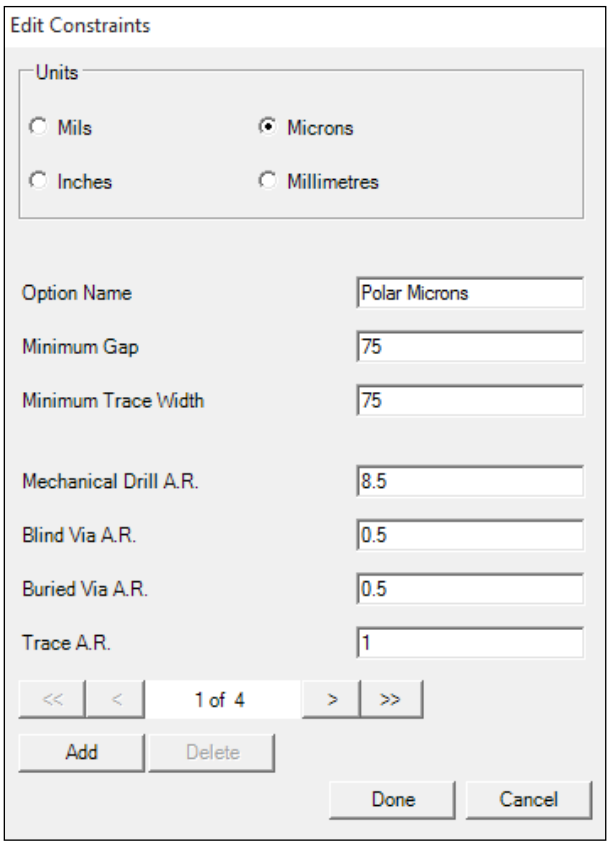
From the Tools menu, select Manufacturing Constraints: the Manufacturing Constraints window opens, displaying any manufacturing constraints added.



By default there will always be at least one. It is important to always have one constraint set active.

Editing constraints

Double-click on a constraint row will bring up the Edit Constraints dialog; use the dialog to add, delete or edit constraints (gaps, trace widths, aspect ratios, etc.)



To edit a constraint set, use the navigation buttons to select the set to be modified, change the values as required and then press Done.

To delete a constraint set, use the navigation buttons to select the set, then press Delete.

To add a new constraint set, press the Add button, this will add a new (empty) constraint row, enter the name and constraint values and press Done.

Adding controlled impedance structures

Speedstack incorporates the facility to add controlled impedance structures to a layer in the stackup.

Speedstack is integrated with the Polar Instruments Si8000m/9000e controlled impedance field solvers so impedance values for a structure may be calculated at the click of a button.

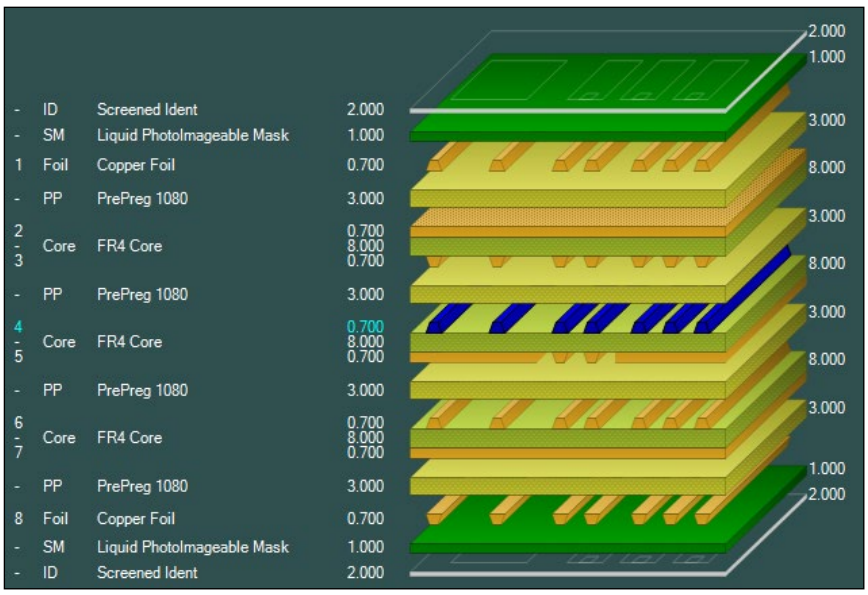
Structure parameters may be copied to the field solver for processing (for example by the Si8000m/9000e Goal Seeking function) and calculated values pasted back into Speedstack for insertion into the stackup.

Each structure can be assigned up to five net class names. These net class names provide a link to the matching impedance nets inside the ECAD PCB layout system.

Speedstack Si caters for frequency dependent calculations, adding comprehensive insertion loss capability into Speedstack. Bidirectional copy and paste from Speedstack Si into Si9000e includes all the relevant loss tangent, roughness and roughness modeling methods along with frequencies of interest.

Adding a controlled impedance structure

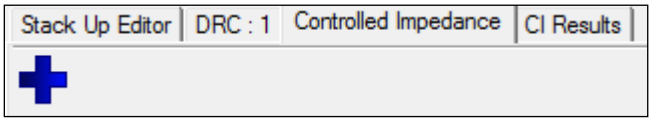
For the example stack below, add a controlled impedance structure to signal layer 4.



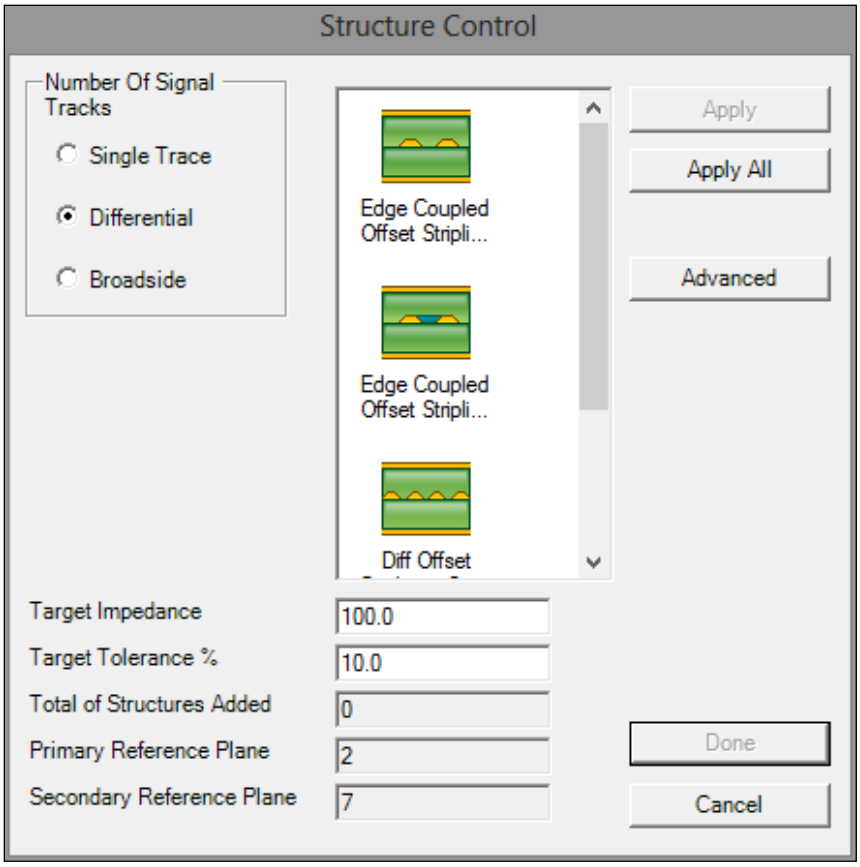
Sample stackup (showing signal layer 4 selected)

Note that in this example Layer 5 is a mixed signal/plane layer. Potential reference planes for Signal Layer 4 are therefore Plane Layer 2, mixed Signal/Plane Layer 5 and plane Layer 7.

With Layer 4 selected, click the Controlled Impedance tab. The Add Structure button is displayed.



Click the Add Structure button; the Structure Control dialog is displayed containing the controlled impedance structures applicable to the selected layer in the stack. Choose values for the target impedance and tolerance. If necessary, resize the Structure Control dialog to view all structures.



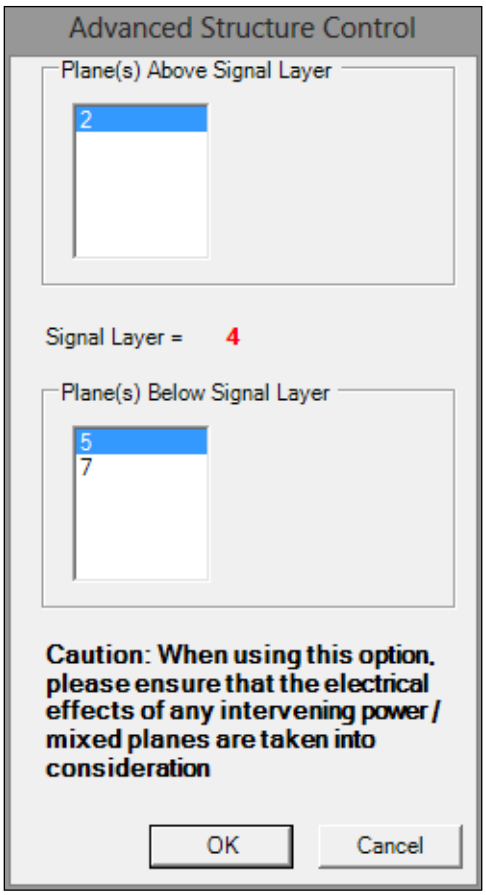
Click the Single Trace, Differential or Broadside option button as appropriate (in this case, choose Single Trace|Offset Stripline 1B1A with a 50 Ohm impedance.)

Note: Broadside only appears as an option where the signal trace is between two reference planes and Differential is selected.

Specify the values for Target Impedance and Tolerance.

Choosing reference planes

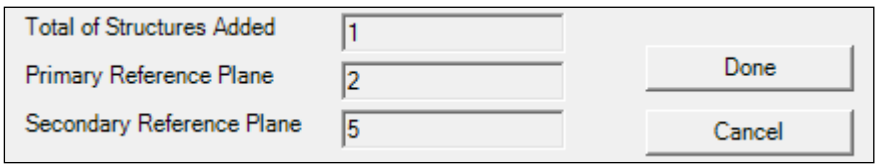
As there are multiple reference planes available (layers 2, 5 and 7, it will be necessary to specify which planes to use for this structure. Click Advanced.



Choose a reference plane from the list of available planes. In the example structure plane layer 2, mixed plane 5 and plane layer 7 are available for reference.

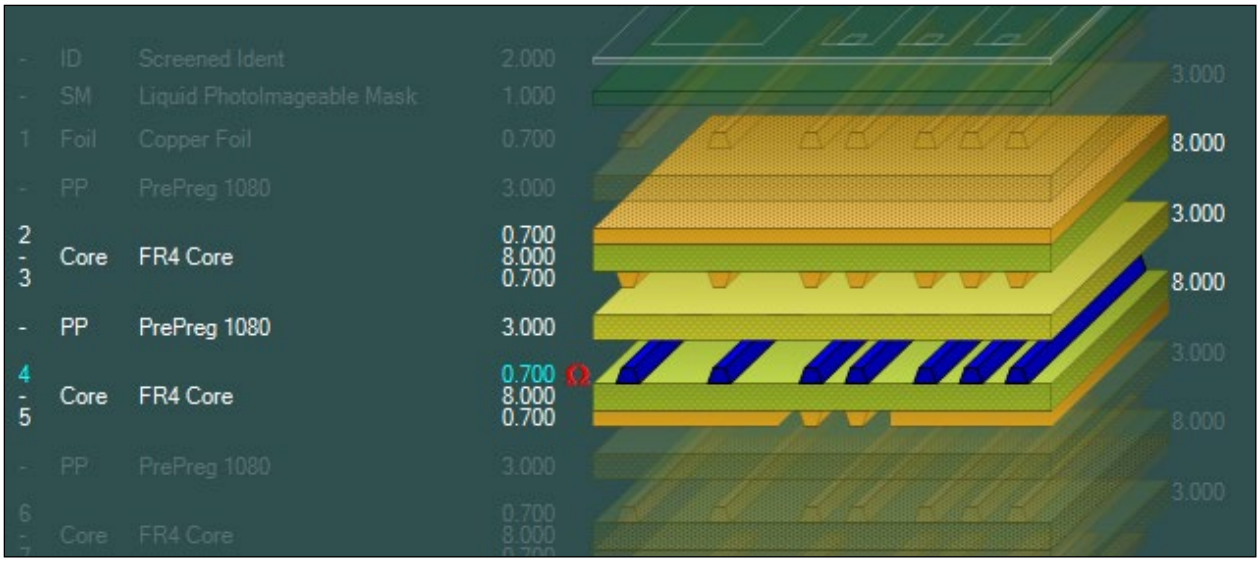
Note: if plane layer 7 is chosen as reference, it will be necessary to take into account the electrical effects of mixed signal/layer plane 5.

In this example choose mixed signal/plane layer 5. Press OK to confirm. The chosen reference planes are shown below.

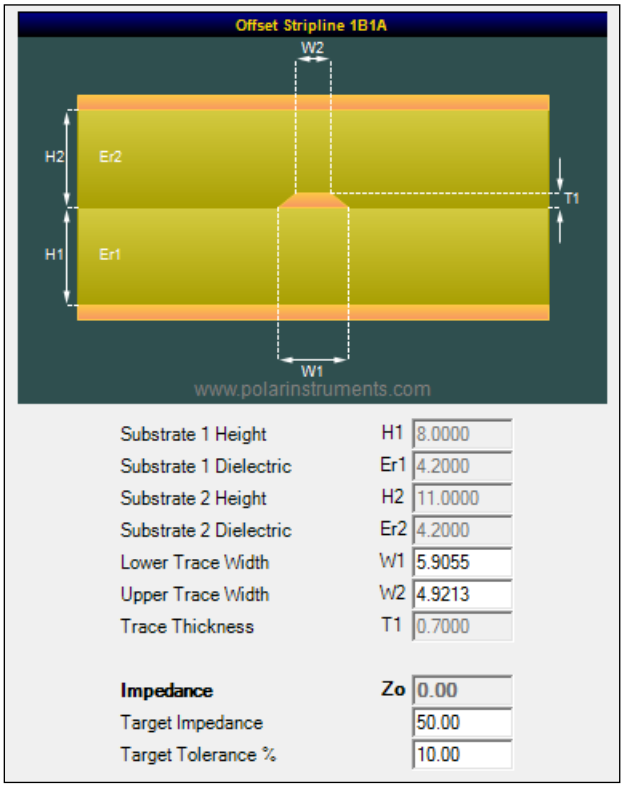


Repeat for all structures to be added. Click Apply for each structure then click Done to finish. In this example, choose a single structure.

Layers with controlled impedance structures are indicated by a red Ohms symbol.



The stackup window changes to reflect the selected signal layer and its associated reference planes. The applied structure is displayed in the Controlled Impedance pane.



The window displays the parameters of the controlled impedance structure. Fields shown "greyed out" are values derived from the choice of materials in the stackup. For this structure, enter the appropriate values for lower and upper trace widths.

Calculate Displayed Structure

Click the Calculate Displayed Structure button to display the impedance value of the structure with the current parameters. The parameters may then be varied to alter the value of the final impedance. In the example above the trace width can be fine-tuned in order to approach the value of the target

impedance; other parameters are changed by modifying the stackup dimensions (for example, core thickness, H1.)

Hint: clicking Apply All in the Structure Control dialog adds a single instance of all structures matching the stackup layer and the chosen criteria; the designer can then choose the structure producing the value nearest the target impedance and delete the structures that are not needed.

Controlled impedance toolbar

Controlled impedance operations are performed via the Controlled Impedance toolbar.

 Add controlled impedance structure to current layer

 Delete structure from current layer

 Clear all structures from current layer

 Rebuild and recalculate all structures

 Calculate displayed structure

 Mirror structures

 Goal seek

 Set CITS test

Free hand notes

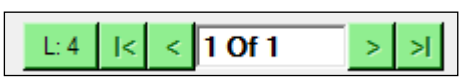
 Structure layer properties

 Structure validation

 Structure Net Classes

Frequency Dependent Properties

Use the structure browse control to display the structure on each layer and navigate through the structures



Changing parameter values

Clicking the Calculate function yields a value for impedance. Parameters (for example, the dielectric height) may be amended to yield a value for impedance closer to the target impedance.

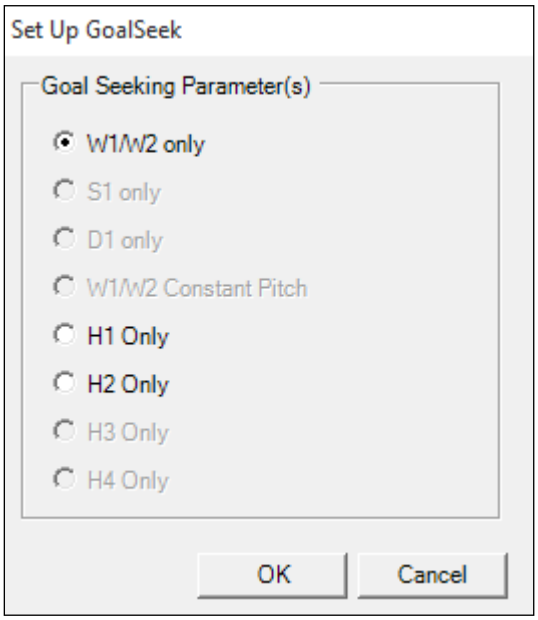
For this example, select the core layers; click the Swap Selected Material button and choose a different core (ensure the same dimensional units are used throughout the structure) and click the Refresh and Calculate Impedance button. The impedance is recalculated to its new value.

To achieve an impedance acceptably close to the target impedance, use the goal seeking function of the Si8000m to alter other parameters (in this case, change the upper and lower trace widths).

Goal seeking with Speedstack

Speedstack provides the facility to solve for horizontal parameters (e.g. trace width and separation, ground strip separation, etc.) to produce the target impedance (or calculate that the target impedance is unachievable with the current values).

Click the Goal Seek button to display the Set Up GoalSeek dialog; the options available will depend on the controlled impedance structure.



Click OK; the Speedstack attempts to arrive at the target impedance by iteratively modifying the specified parameters. It may be necessary to add or delete prepregs to achieve the target impedance.

Goal seeking with the Si8000m/9000e

Speedstack Stackup Builder is fully integrated with the Si8000m/Si9000e Controlled Impedance Field Solvers. Users can transfer Stackup layer dimensions to the Field Solver, solve for stackup parameters to produce the target impedance (or calculate that the target impedance is unachievable with the current values) then transfer the solved dimensions back to Speedstack.

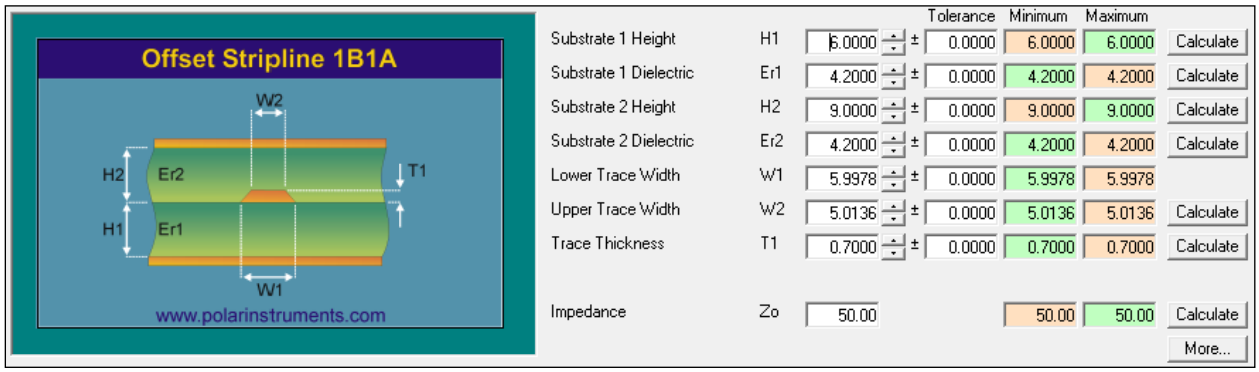
Ensure the Field Solver is running and that its units match the Speedstack units.

To Field Solver

With the stackup parameters displayed in the Controlled Impedance window, click To Field Solver to transfer the current Speedstack parameters to the Si8000m/Si9000e.

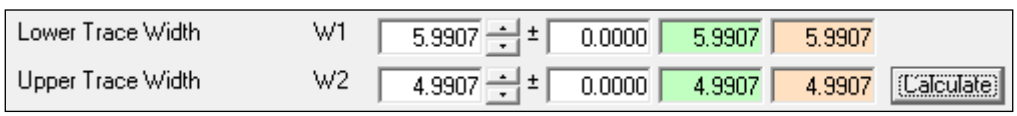
Paste from Speedstack

Switch to the field solver and click the Paste from Speedstack button to load the parameters into the associated field solver fields. The field solver reflects the structure and parameters of that selected in Speedstack.



For the data shown above seek a final value for impedance of 50 Ohms; H1, Er1 and T1 are fixed, so goal seek on W1,W2.

Click the Upper Trace Width (W2) Calculate button to goal seek on trace width. The field solver returns new values for trace width to produce 50 Ohms final impedance.



Copy to Speedstack

Click the Copy to Speedstack button, switch to Speedstack and click the From Field Solver button to display the solved parameters for the target impedance.

From Field Solver

Note: it may be necessary to round some dimensions (for example, the dielectric heights) to the nearest practical values and recalculate the impedance.

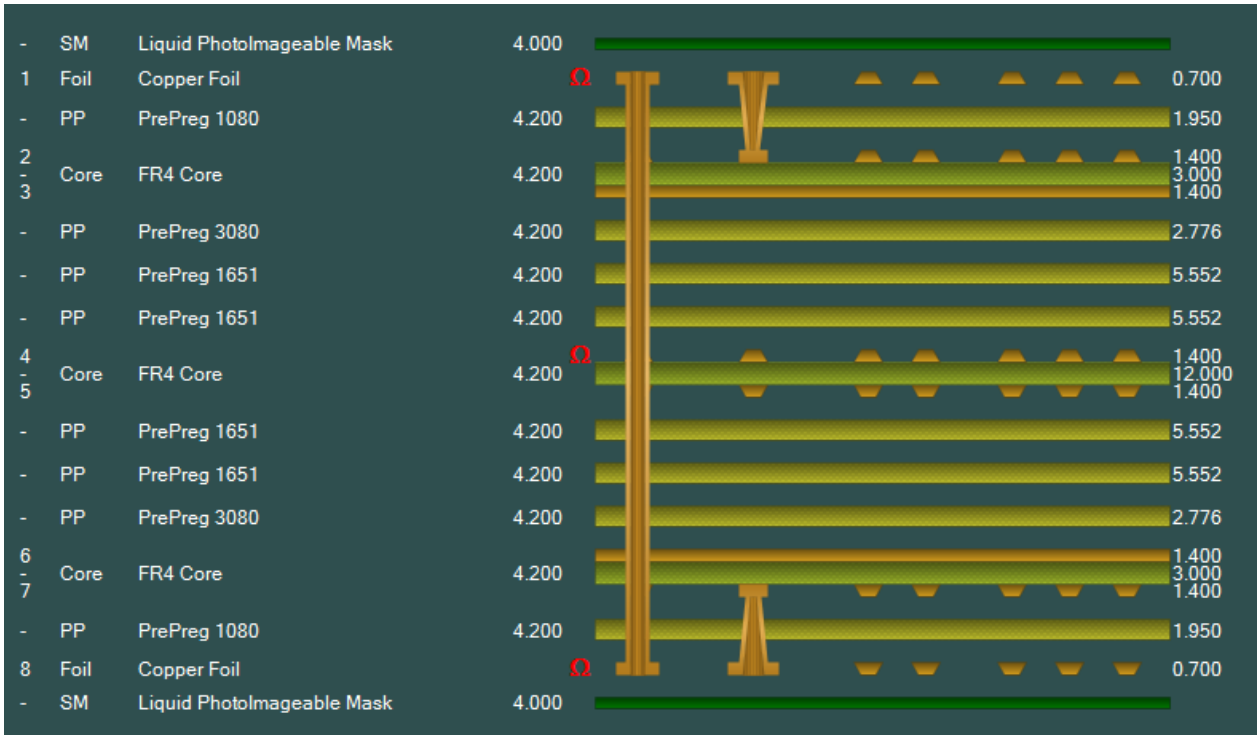
Changing layer functionality

It is often convenient to base a new design on an existing stackup and then add or remove electrical layers to create the new stack, leaving the previous existing structures intact or to switch between layer types (Signal, Plane, Mixed, Hatched) without removing structures.

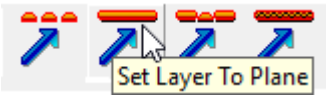
Speedstack allows the designer to retain and re-allocate structures when changes are made to the electrical layers of the stackup. This enables reallocation of structures after the following stackup changes:

- Adding foils and/or cores – increasing the layer count
- Deleting foils and/or cores – reducing the layer count
- Moving foils and cores up and down, even beyond another copper layer – maintaining the layer count but, for example, exchanging two different thickness cores within the stackup
- Copying and pasting foil or core – increasing the layer count
- Changing layer type – signal to plane, plane to signal, mixed to signal or plane, signal to hatch, hatch to signal
- Deleting a rigid core and adding a flex core – to maintain layer count but swapping material type
- Deleting a rigid core and adding two foils – to maintain layer count but switching to an HDI type build

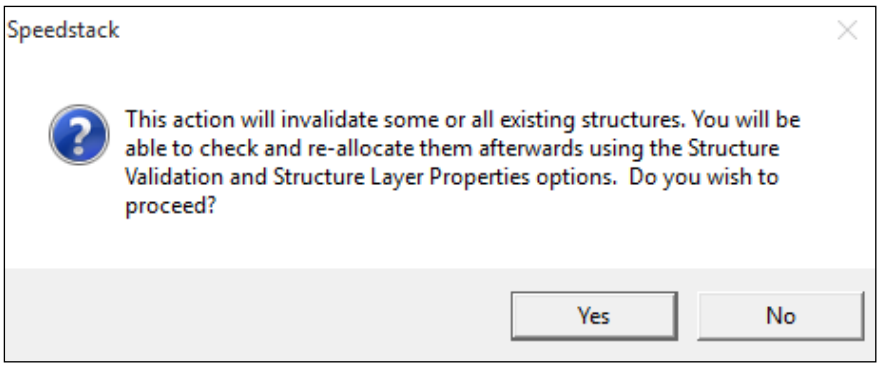
For the following examples, consider the stack below.



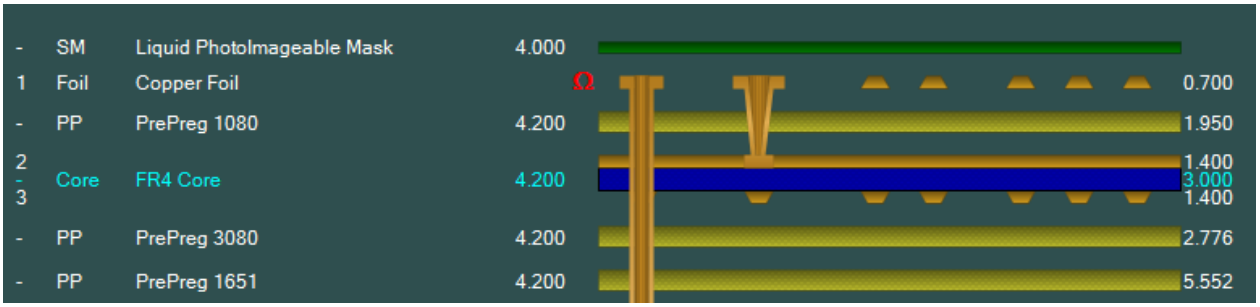
Switching layer types and reallocating structures



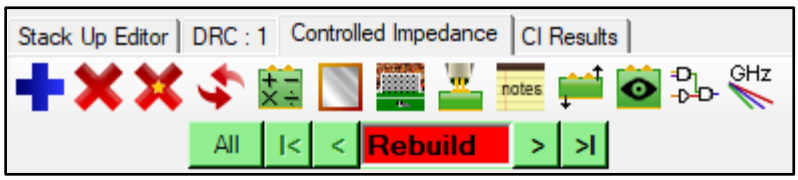
Switch signal layer 2 to a plane layer and plane layer 3 to a signal layer. Speedstack issues a warning indicating that continuing with the change will require the existing structures to be re-allocated.



Select Yes to confirm the change to the stackup. The stack editor reflects the change in the stackup, layer 2 is a plane layer and layer 3 a signal layer.

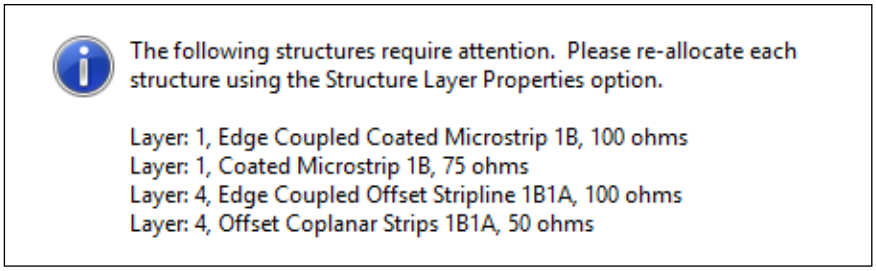


Speedstack also displays a flashing Rebuild indicator; due to the changes to the stackup it is necessary to refresh the structures.

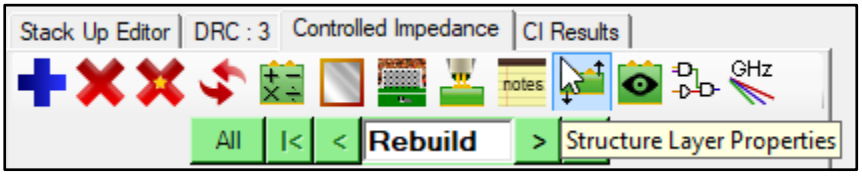


 Rebuild and Recalculate

Click the Rebuild and Recalculate icon – Speedstack displays an information dialog indicating which structures need re-allocating.

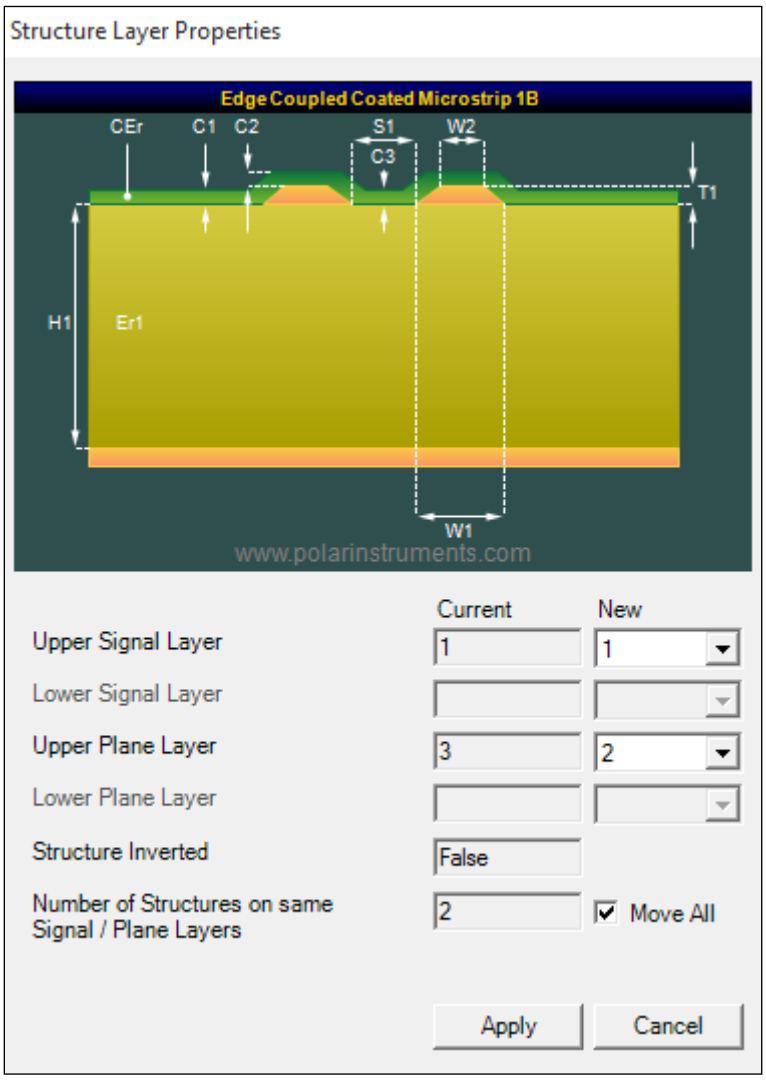


Click OK then click the Structure Layer Properties icon to reallocate the structures to the correct signal and plane layers.



The Structure Layer Properties dialog includes two layer columns, the Current layer column and the New layer column. The Current column shows the Signal / Plane stackup layers assigned to the structure before the stackup was changed.

The New column allows the structure to be re-allocated to reflect the new stackup layer types.

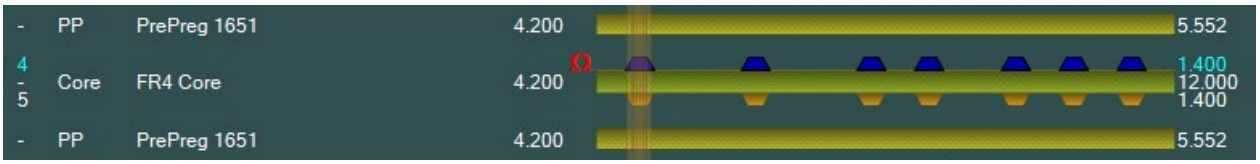


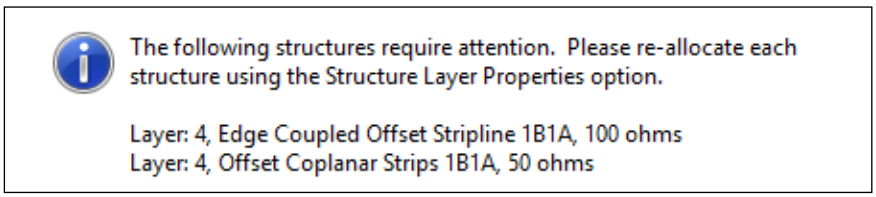
In this case notice the Upper Plane Layer is changed from layer 3 to layer 2.

In many cases multiple structures will have the same Signal / Plane layer assignments. In the example above Speedstack indicates that there are two structures affected. Click the Move All check box to re-allocate all matching structures in a single operation then click Apply.


Rebuild and Recalculate

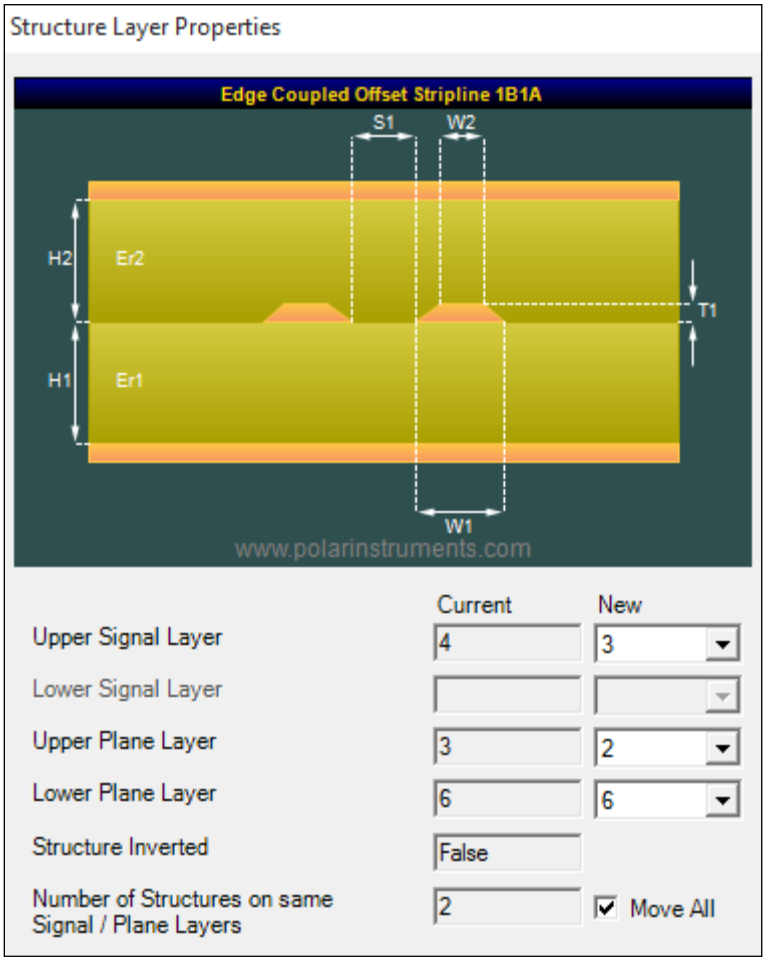
Rebuilding the stack indicates that other structures (i.e. the two structures on layer 4) also require layer reallocation.






Structure Layer Properties

Use the structure selection arrow keys to step through to the structures on layer 4 then click Structure Layer Properties.



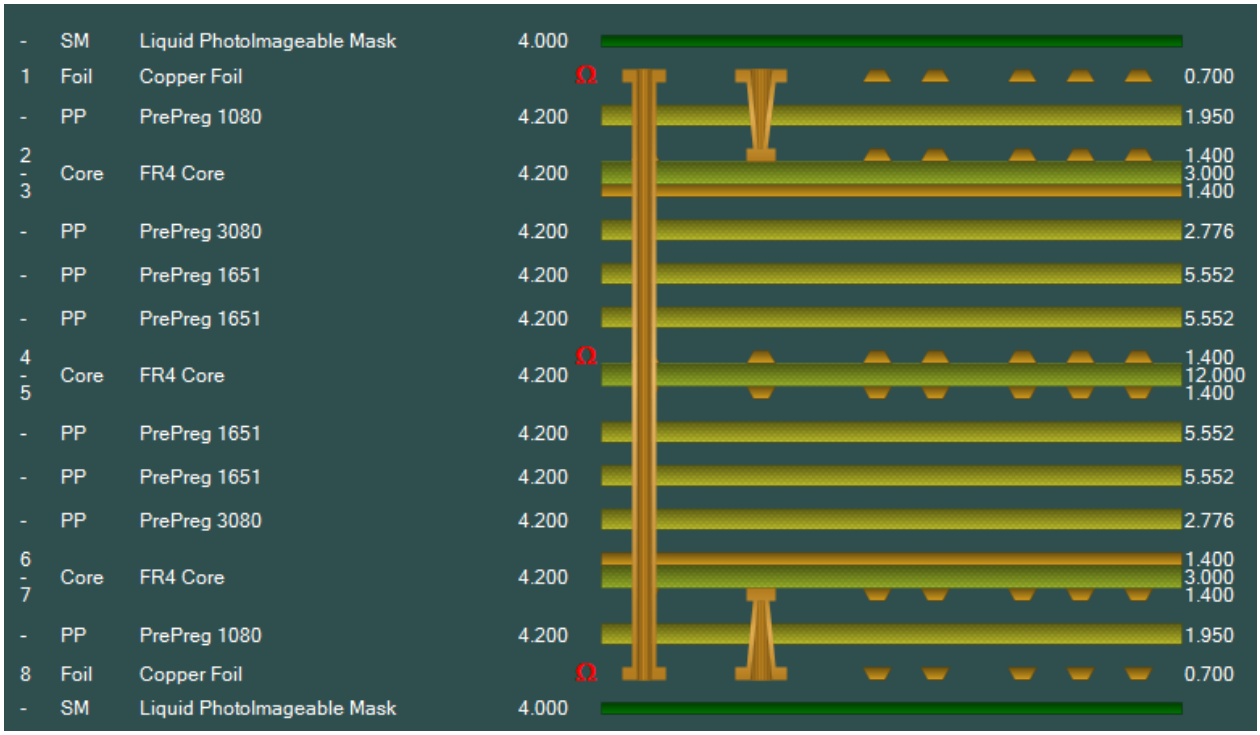
Reallocate the layers as required then click Apply. With the structures re-allocated Rebuild and Calculate the structures as describer earlier.

Note that structure Trace Width and Separation parameters are retained at their original values together with the Target Impedance and Tolerance. (Depending upon how the structures have been re-allocated it may be necessary to goal seek the trace width and separation parameters to meet the target impedance.)

Increasing the layer count

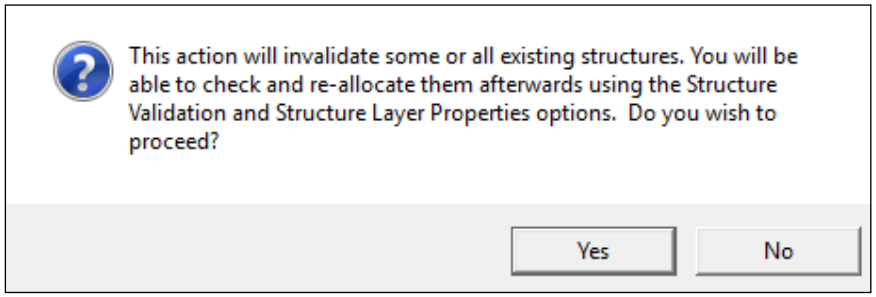
It is a common requirement for designers to base a new design on an existing proven stackup and then add or remove electrical layers to create a new stack, leaving the previous existing structures intact.

Consider the 8 layer stack below.



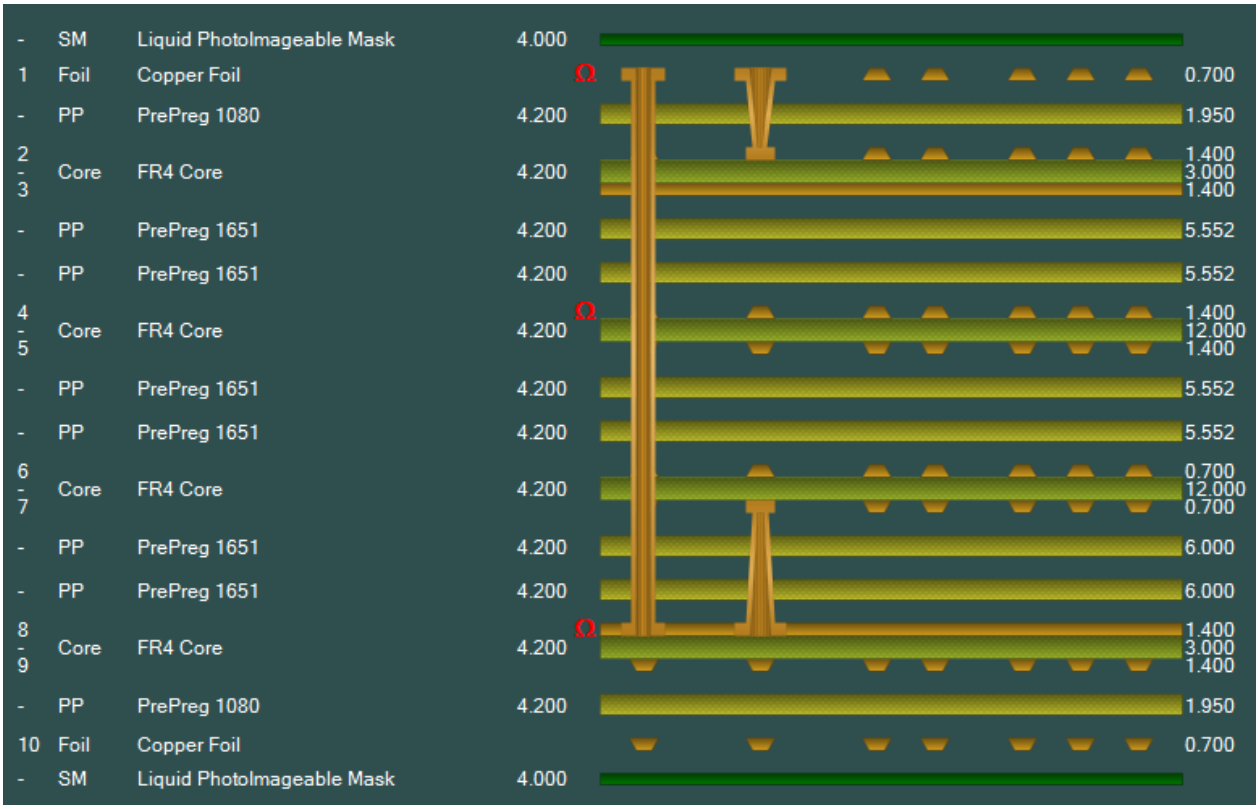
For this example, add a core between layers 5 and 6.

Speedstack will display a warning that proceeding with the change will require the existing structures to be reallocated.



Click Yes to proceed.

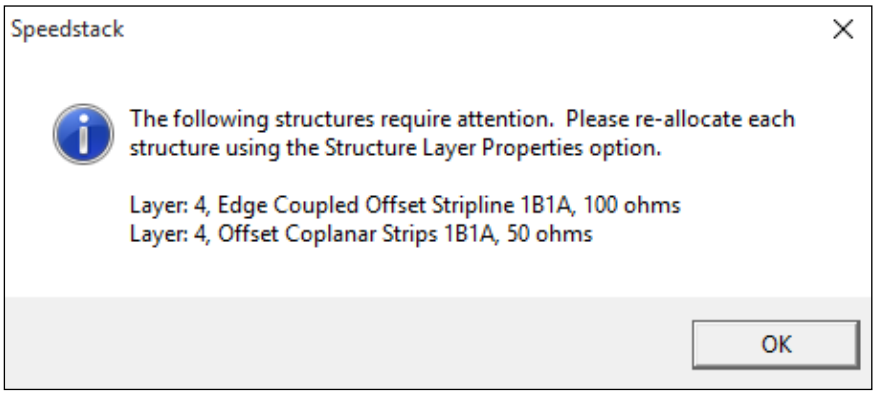
In order to maintain a symmetrical stack, delete the Prepreg 3080 materials and add Prepreg 1651 materials to create a symmetrical 10 layer stack.




Rebuild and Recalculate

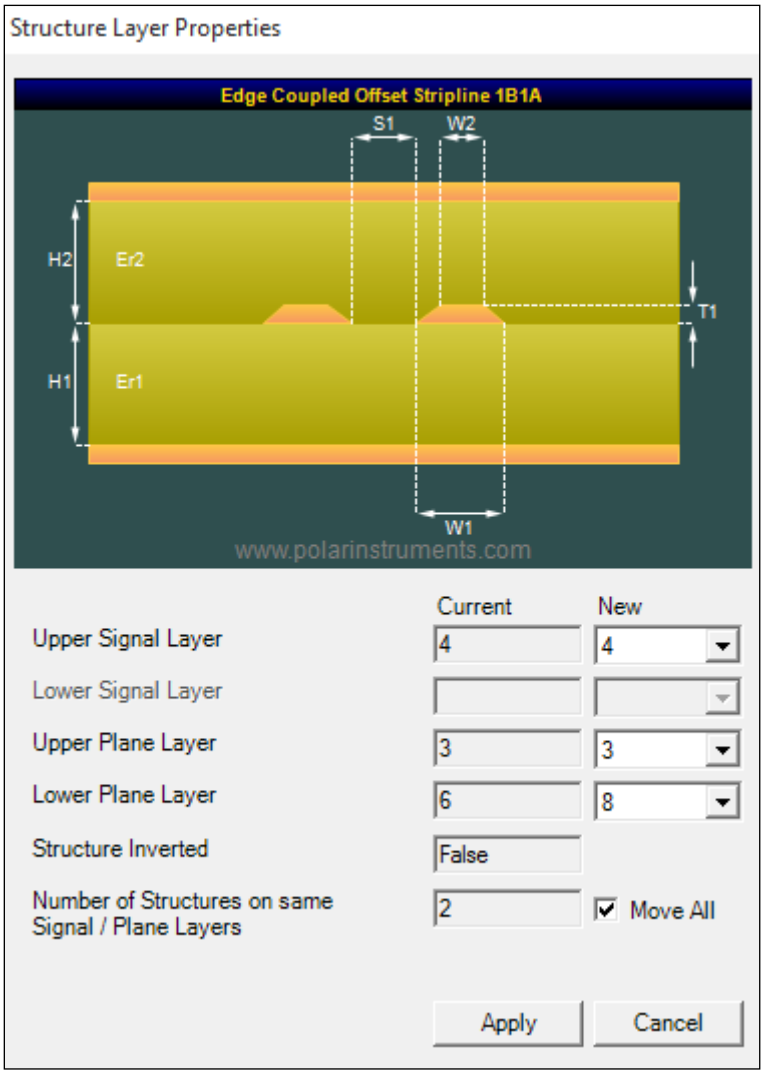
Click Rebuild and Recalculate

Speedstack displays an information dialog indicating the structures that need reallocating.



Click OK.

Use the structure navigation buttons to select the structure layer then click the Structure Layer Properties button to display the Structure Layer Properties dialog.



Note that for the modified stack the lower plane layer has been reallocated to layer 8.

Click Apply and then Rebuild and Recalculate.

If necessary, goal seek on line widths to bring the impedance within specification.

For the above stack edit the Drill Properties to finalise the stack changes.

Repeat the procedure for each structure as necessary.

Structure net classes

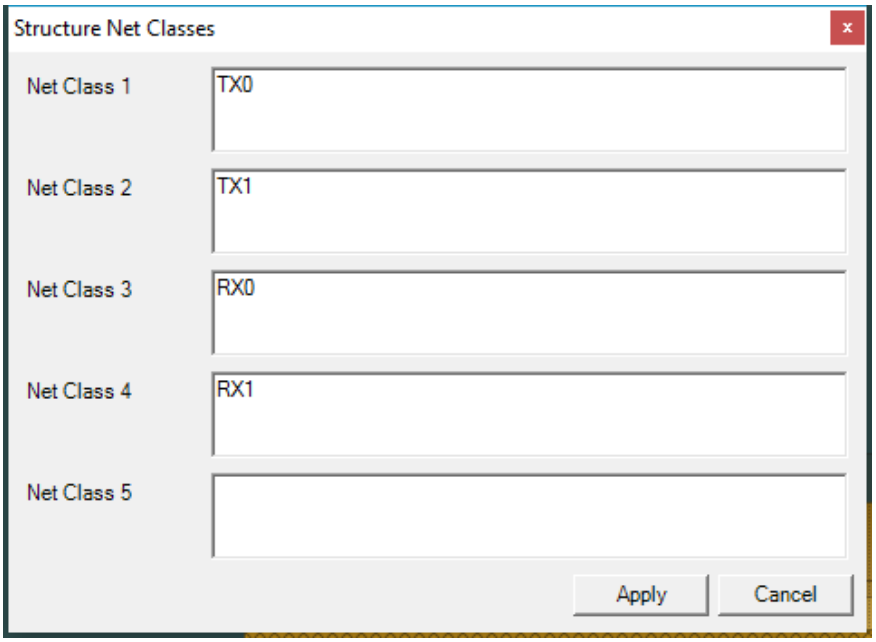
Speedstack allows up to five Net Class names to be stored with each structure. These net class names provide a link to the matching impedance nets inside the ECAD PCB layout system. Net classes are supported in Speedstack's import / export file formats.

Net class columns can be selected for display on the technical report.

Net classes

To display the Structure Net Classes dialog click the Net Classes button

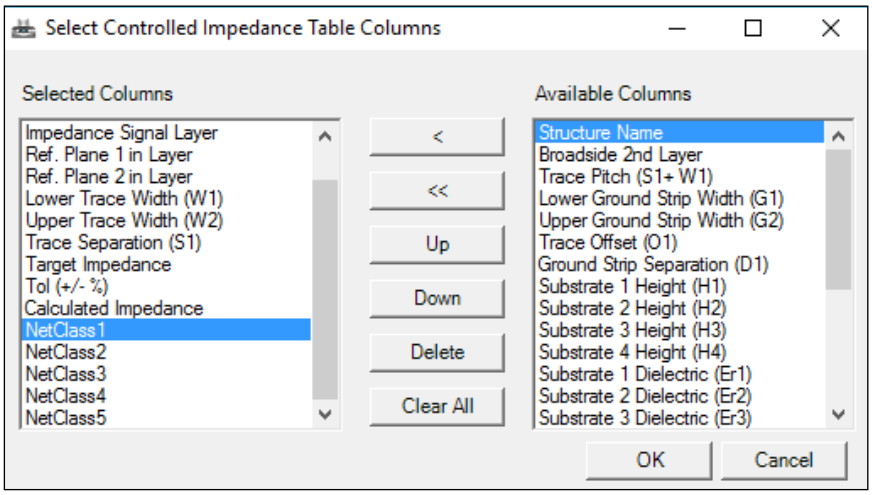
Enter the net class names in the text boxes and click Apply.



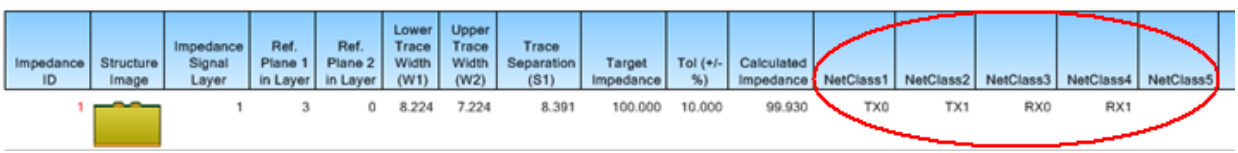
Up to five net class names may be stored with each structure.

Select Impedance Columns

Click the Select Impedance Columns button and Select the Net Class columns to display the net classes on the Speedstack technical report.



The chosen columns are displayed in the selected order.



Working with Si Projects in Speedstack and Si8000m/Si9000e

Si Projects

The Si Projects feature incorporated in Speedstack and Si8000m/Si9000e allows for easy transfer of controlled impedance structures from the Speedstack stackup design tool into the Si8000m and Si9000e field solvers.

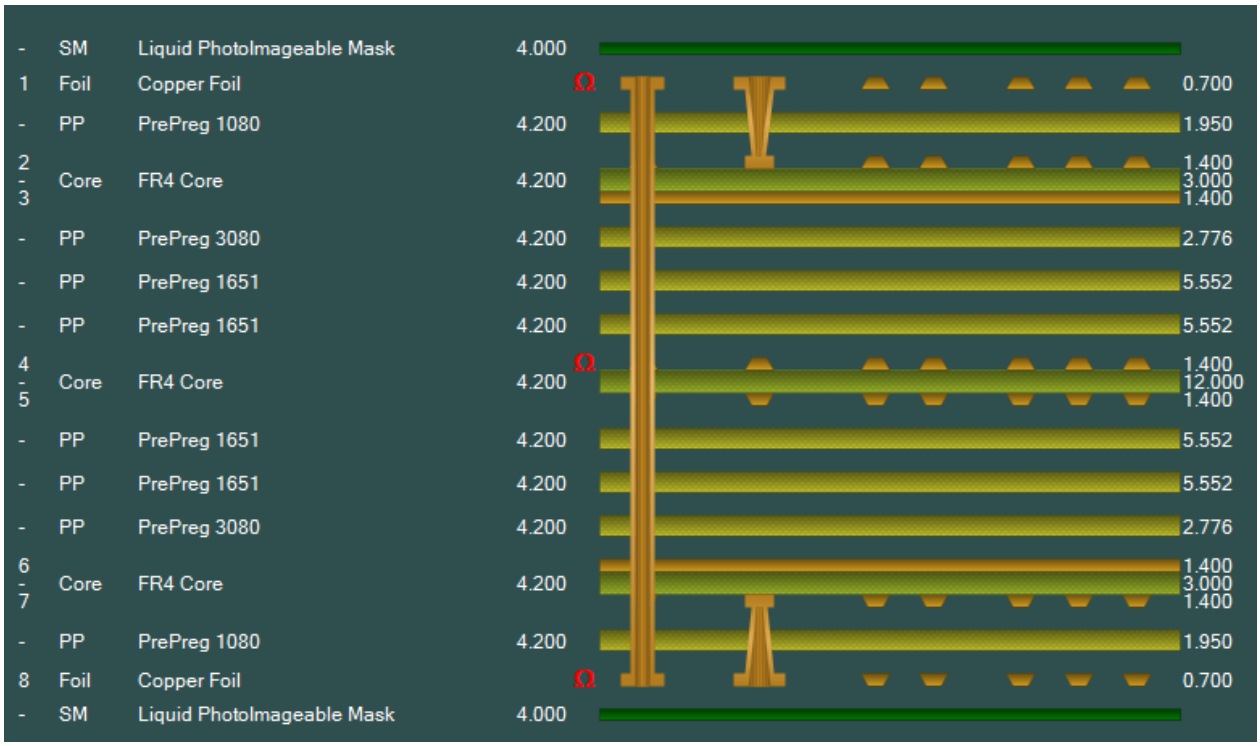
Si Projects allows groups of structures to be saved and recalled in Si8000m/Si9000e and entire stackups of structures to be pasted from Speedstack into Si8000m and Si9000e with just a few clicks of the mouse.

To Si Project

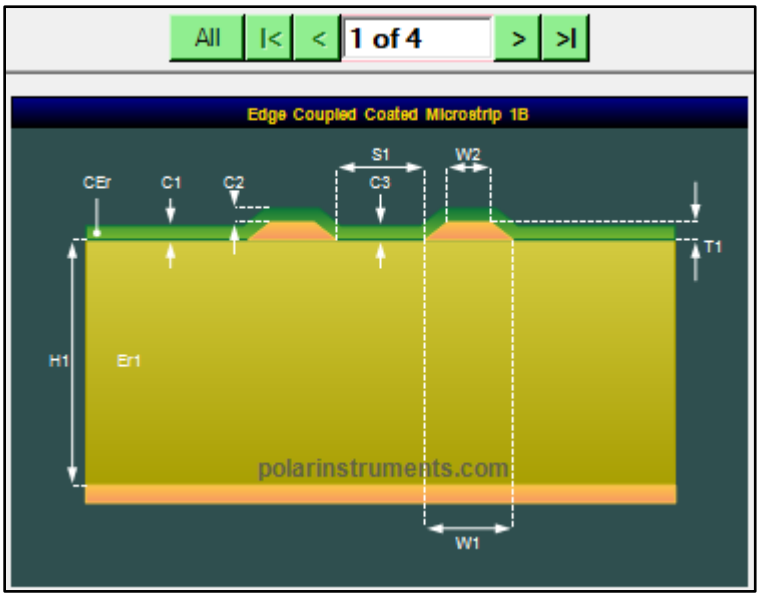
The To Si Project toolbar icon copies a group of structures from Speedstack and places them onto the clipboard, these structures can then be pasted directly into the Si8000m or Si9000e Project group

Transferring structures from Speedstack to the field solver

The stackup below in Speedstack's Stackup Editor contains controlled impedance structures in the layers indicated by the Ohms symbol.



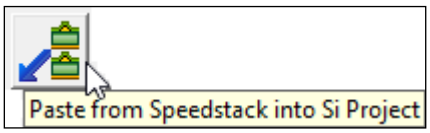
Click Speedstack's Controlled Impedance tab and use the structure navigation controls to step through and display the structures.



To Si Project

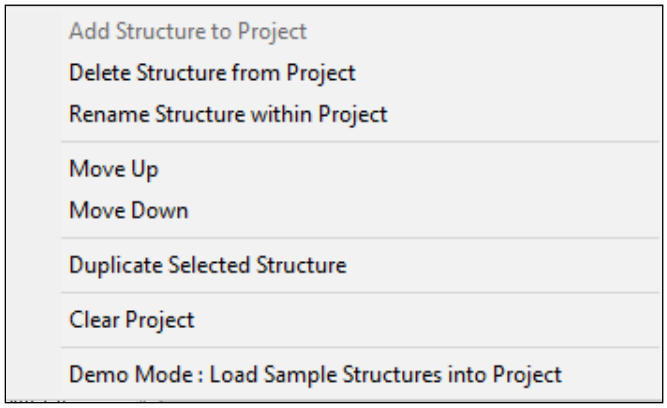
Use the Si Project toolbar buttons in the Speedstack and the Si8000m/Si9000e interface to transfer the structures via the Windows clipboard to the field solver.

Switch to the field solver and paste the structures from the clip board into the field solver Si project.



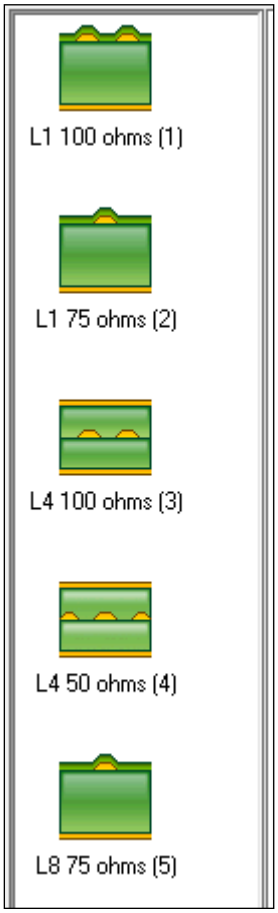
The complete set of structures appears in the field solver's Project window.

The Si Project window lists the transferred structures in layer order, showing the layer number and value along with a thumb nail graphic indicating the structure configuration. Right click on a structure in the structure list to view the structure options.

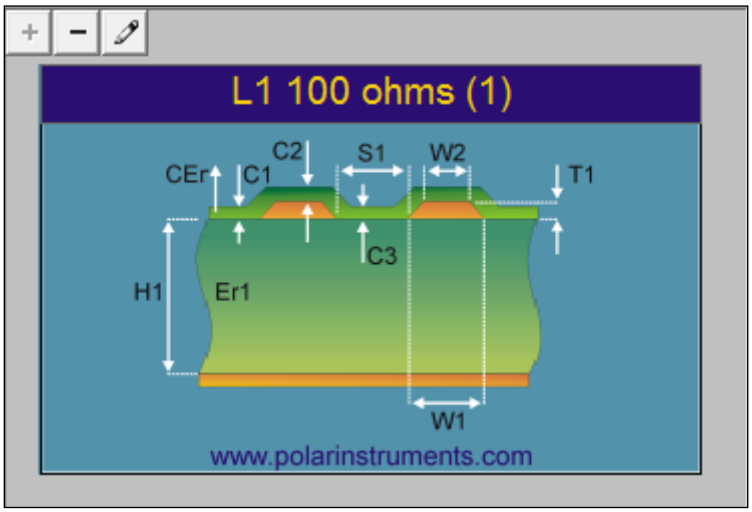


Adding/deleting and modifying structures

Selecting each structure displays its associated graphic in a grey background.



Click the + and – buttons in the structure graphic to add additional structures from the Si structure library or remove selected structures from the Project folder. Click the Rename Structure (the pencil icon) to assign the structure a descriptive name.



With a structure selected the structure parameters can be modified as required and the impedance recalculated.

Frequency dependent loss calculations (Speedstack Si only)

Note: Frequency dependent loss calculations are available in Speedstack only when used in conjunction with the Si9000e Transmission Line Field Solver.

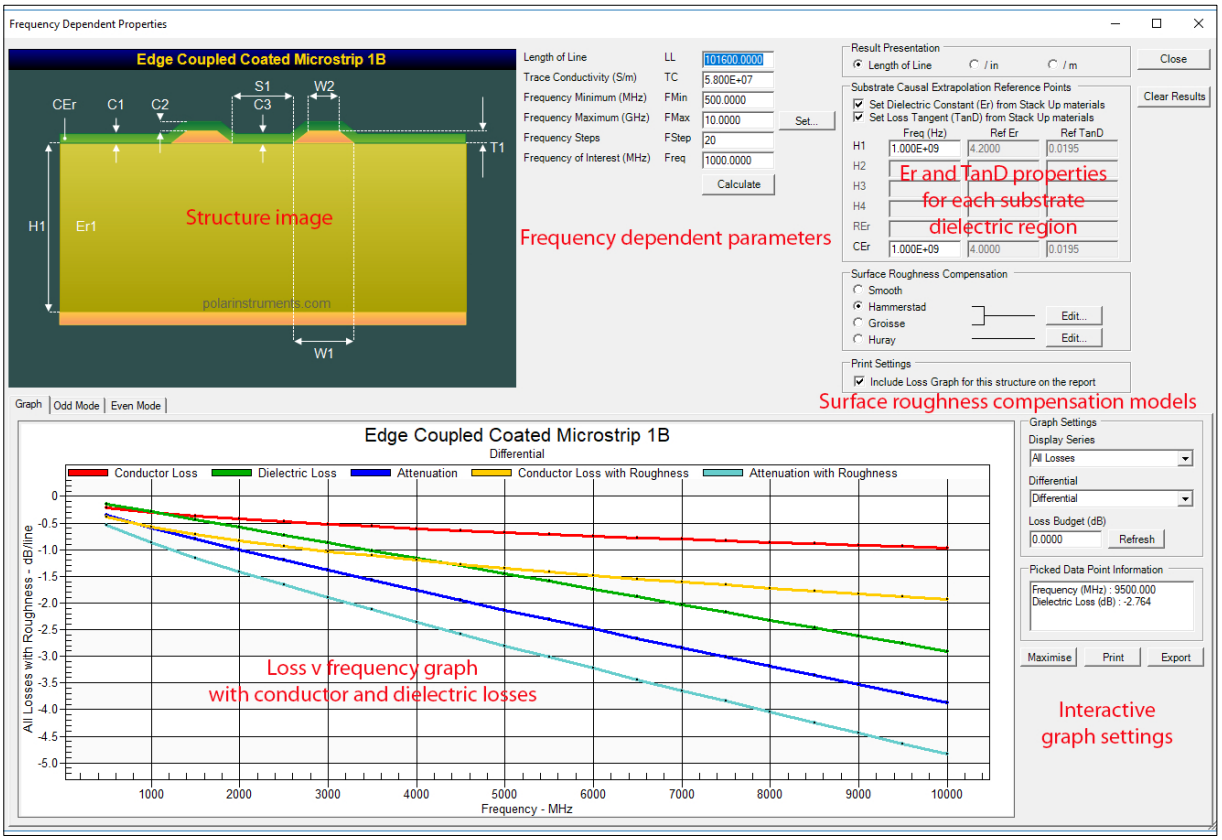
Speedstack Si (Speedstack stackup builder plus Si9000e transmission line field solver) provides for calculations of frequency dependent loss given the information applicable to loss in the transmission line structure. The information includes material properties, comprising dielectric constant and loss tangent, conductor properties such as trace conductivity and surface roughness and the frequency range over which the transmission line structure will operate

Graphing against frequency is provided for impedance magnitude, conductor loss and dielectric loss (with or without roughness compensation,) inductance, capacitance, resistance, conductance and skin depth. Graphing for differential structures include differential, odd and even modes.

Frequency Dependent Properties

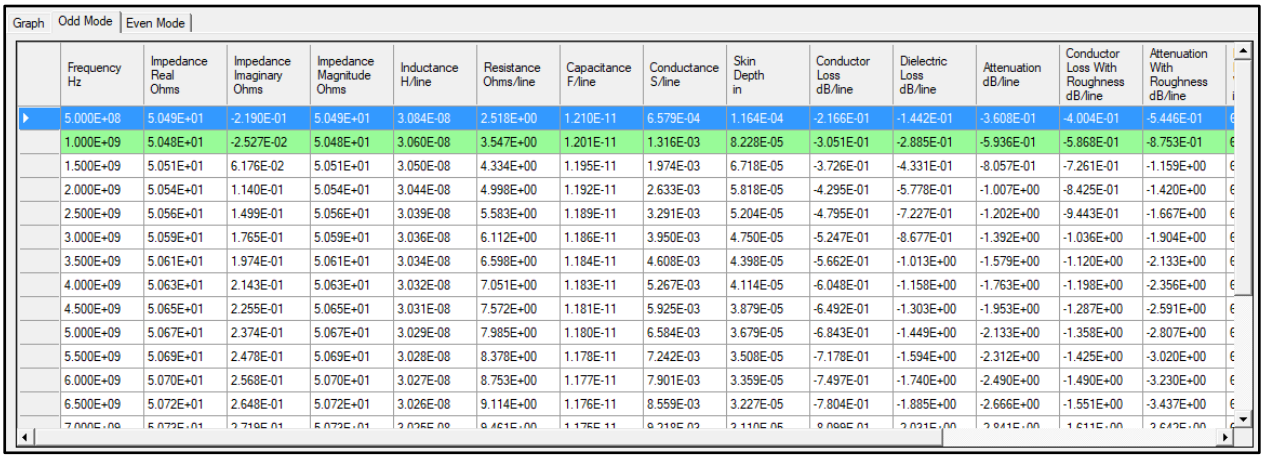
Each structure in the stack includes a set of frequency dependent properties.

Click the Frequency Dependent Properties icon to load the Frequency Dependent Properties dialog.



The Frequency Dependent Properties dialog includes:

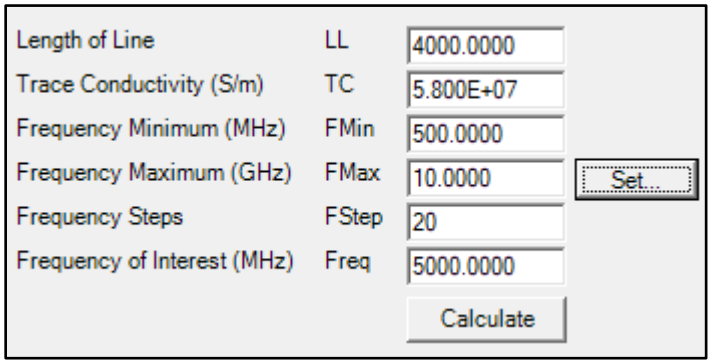
- the structure image of the selected structure
- frequency dependent parameters for the user defined frequency range and *frequency of interest*
- a table of substrate causal extrapolation reference points for each substrate dielectric/region
- surface roughness compensation model selection between Hammerstad, Groisse and Cannonball-Huray methods
- the loss v frequency graph showing the data series for conductor and dielectric losses and total attenuation
- interactive graph setting with data point selection allowing drilling down to the underlying loss data
- data tables for the selected frequency range



Frequency Hz	Impedance Real Ohms	Impedance Imaginary Ohms	Impedance Magnitude Ohms	Inductance H/line	Resistance Ohms/line	Capacitance F/line	Conductance S/line	Skin Depth in	Conductor Loss dB/line	Dielectric Loss dB/line	Attenuation dB/line	Conductor Loss With Roughness dB/line	Attenuation With Roughness dB/line
5.000E+08	5.049E+01	-2.190E-01	5.049E+01	3.084E-08	2.518E+00	1.210E-11	6.579E-04	1.164E-04	-2.166E-01	-1.442E-01	-3.608E-01	-4.004E-01	-5.446E-01
1.000E+09	5.048E+01	-2.527E-02	5.048E+01	3.060E-08	3.547E+00	1.201E-11	1.316E-03	8.228E-05	-3.051E-01	-2.885E-01	-5.936E-01	-5.868E-01	-8.753E-01
1.500E+09	5.051E+01	6.176E-02	5.051E+01	3.050E-08	4.334E+00	1.195E-11	1.974E-03	6.718E-05	-3.726E-01	-4.331E-01	-8.057E-01	-7.261E-01	-1.159E+00
2.000E+09	5.054E+01	1.140E-01	5.054E+01	3.044E-08	4.998E+00	1.192E-11	2.633E-03	5.818E-05	-4.295E-01	-5.778E-01	-1.007E+00	-8.425E-01	-1.420E+00
2.500E+09	5.056E+01	1.499E-01	5.056E+01	3.039E-08	5.583E+00	1.189E-11	3.291E-03	5.204E-05	-4.795E-01	-7.227E-01	-1.202E+00	-9.443E-01	-1.667E+00
3.000E+09	5.059E+01	1.765E-01	5.059E+01	3.036E-08	6.112E+00	1.186E-11	3.950E-03	4.750E-05	-5.247E-01	-8.677E-01	-1.392E+00	-1.036E+00	-1.904E+00
3.500E+09	5.061E+01	1.974E-01	5.061E+01	3.034E-08	6.598E+00	1.184E-11	4.608E-03	4.398E-05	-5.662E-01	-1.013E+00	-1.579E+00	-1.120E+00	-2.133E+00
4.000E+09	5.063E+01	2.143E-01	5.063E+01	3.032E-08	7.051E+00	1.183E-11	5.267E-03	4.114E-05	-6.048E-01	-1.158E+00	-1.763E+00	-1.198E+00	-2.356E+00
4.500E+09	5.065E+01	2.255E-01	5.065E+01	3.031E-08	7.572E+00	1.181E-11	5.925E-03	3.879E-05	-6.492E-01	-1.303E+00	-1.953E+00	-1.287E+00	-2.591E+00
5.000E+09	5.067E+01	2.374E-01	5.067E+01	3.029E-08	7.985E+00	1.180E-11	6.584E-03	3.679E-05	-6.843E-01	-1.449E+00	-2.133E+00	-1.358E+00	-2.807E+00
5.500E+09	5.069E+01	2.478E-01	5.069E+01	3.028E-08	8.378E+00	1.178E-11	7.242E-03	3.508E-05	-7.178E-01	-1.594E+00	-2.312E+00	-1.425E+00	-3.020E+00
6.000E+09	5.070E+01	2.568E-01	5.070E+01	3.027E-08	8.753E+00	1.177E-11	7.901E-03	3.359E-05	-7.497E-01	-1.740E+00	-2.490E+00	-1.490E+00	-3.230E+00
6.500E+09	5.072E+01	2.648E-01	5.072E+01	3.026E-08	9.114E+00	1.176E-11	8.559E-03	3.227E-05	-7.804E-01	-1.885E+00	-2.666E+00	-1.551E+00	-3.437E+00

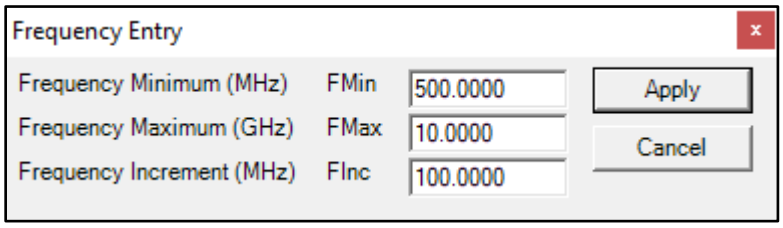
Frequency dependent parameters

Speedstack Si runs a detailed analysis of the transmission line structure for controlled impedance and insertion loss. Each structure in Speedstack can store a complete set of frequency dependent parameters: Length of Lines, Frequency Minimum, Frequency Maximum, Frequency Steps, substrate data, surface roughness and loss budget. Supply the values in the dialog below.



Specify the line length and trace conductivity along with the frequency range and *frequency of interest*.

To specify the frequency range click the Set… button and enter the minimum frequency (in MHz) and maximum frequency (in GHz); specify the frequency increment (in MHz) then click Apply.



With all parameters entered, click Calculate. Results are displayed in graphical and tabular form.

To provide for applications where the insertion loss requirements or loss budget specifications are needed for a given frequency the results for the specified frequency of interest are highlighted in green in the table of data.

Presentation of results

Use the Result Presentation dialog to choose units in which to present plots and tables of results.

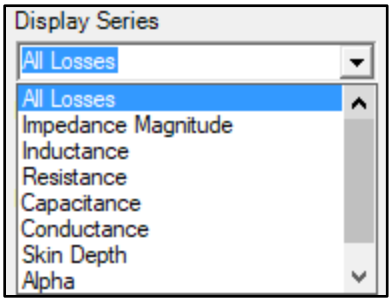
The graphs are able to display results in dB/line length, dB/inch or dB/metre.

Click the unit of choice and click Calculate to refresh the graphical display of data.

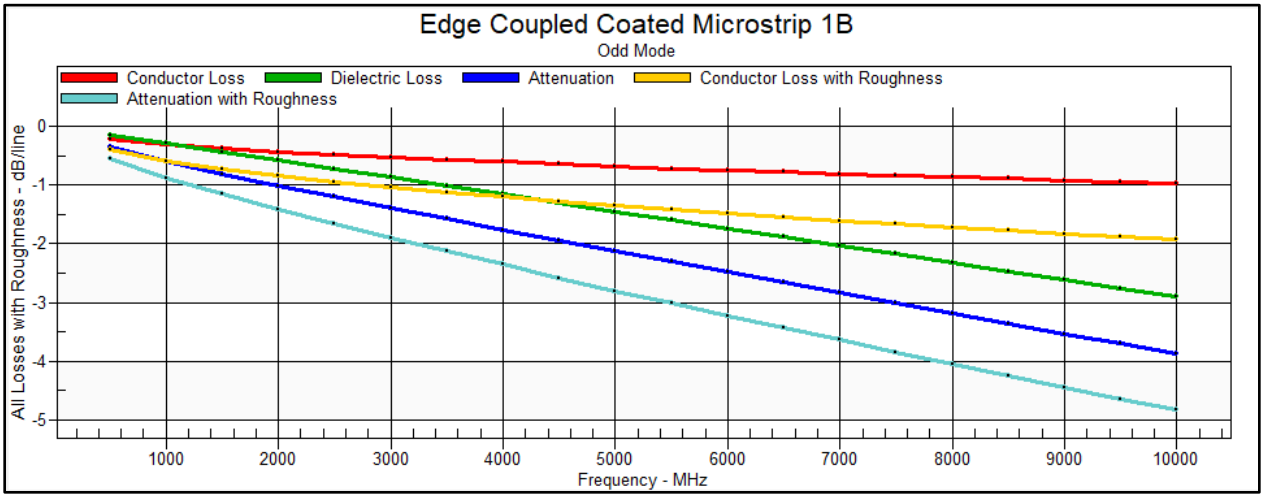
Graph settings

Use the Graph Settings dialog to choose the display series.

Speedstack Si graphs All Losses – conductor loss, dielectric loss and total attenuation.

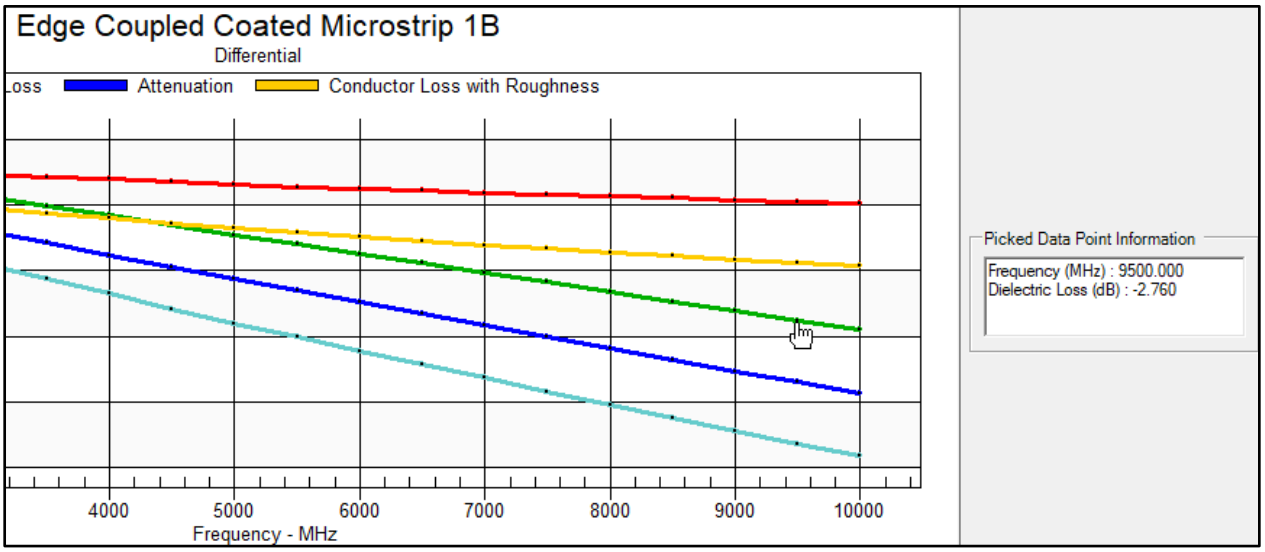


If roughness compensation is applied the data series conductor loss with roughness and attenuation with roughness are added to the graph.

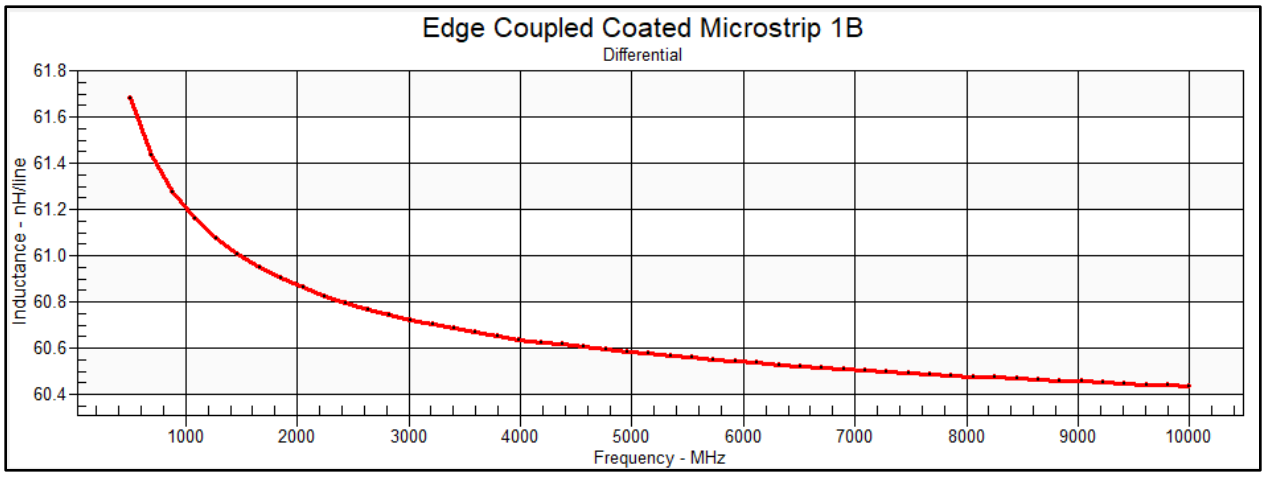


All losses with roughness

Speedstack charts are interactive. Click on a point on the data series of interest to display the data point value in the Picked Data Point Information text box



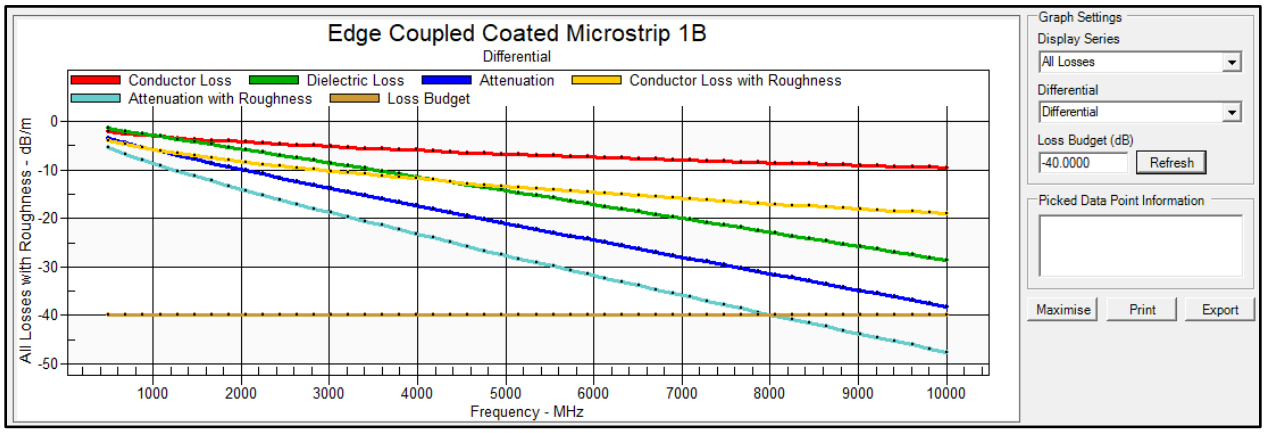
The range of data series includes losses, impedance magnitude, inductance, capacitance and skin depth: Choose the data series from the Display Series drop down.



Graph of inductance v frequency

Displaying the loss budget

A value for loss budget can be added to a graph. A loss budget line will allow losses that exceed the budget to be easily identified.



The plot above indicates that the loss budget is exceeded by the total attenuation (cyan) beyond 8000Mhz (8GHz.)

Setting the Loss Budget stores the value with the structure for future use. This would prove useful if the stack up is changed and it is necessary to ensure that the structure still meets the loss requirements after the changes.

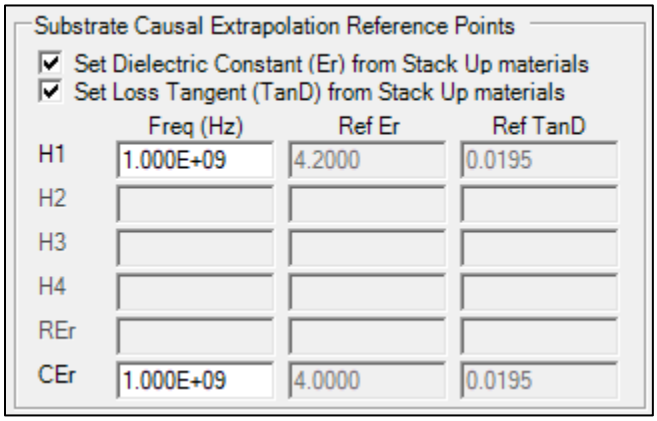
Material and surface roughness properties

The Speedstack graph above charts all losses, the dielectric loss and the significant increase in the overall loss due to surface roughness, allowing the materials supplier to isolate the contributions of the different loss mechanisms.

Dielectric loss

In order accurately to calculate dielectric loss it is necessary to understand the material / substrate properties.

Speedstack Si allows substrate properties including dielectric constant (Er) and loss tangent (TanD) to be specified for each structure substrate region.



Speedstack Si causally extrapolates Er and TanD over the specified frequency range using a single value of Er and TanD to enable Svensson-Djordjevic frequency dependent permittivity modelling for each dielectric layer in the current controlled impedance structure. The table above therefore provides the ability to specify the extrapolation reference points for each substrate region; the reference point data is usually available from the material supplier data sheets. The values of Er and TanD can, optionally, be derived from the materials in the stack. (See the Polar Application Note AP8184 or the Si9000e User Guide for a more detailed discussion of causally extrapolating substrate data.)

The fields shown active in the table in the dialog reflect the structure selected; inapplicable fields are shown greyed out.

The fields shown above allow values to be specified for the frequency of interest, the dielectric constant, Er, and loss tangent, TanD for the prepreg dielectric and the coating. Enter the parameters and click Calculate to refresh results.

Conductor losses – surface roughness compensation
In order to provide good adhesion between copper and dielectric materials in core layers PCB materials vendors control the roughness of the associated copper layers (typically by chemical treatment). Speedstack Si provides industry standard methods of compensation for surface roughness in frequency dependent calculations; the compensation methods include:

Smooth copper, (no compensation for Cu loss at all)

Hammerstad modelling

Groisse modelling

Huray modelling

Speedstack charts dielectric losses along with conductor losses and attenuation values that optionally include compensation for surface roughness. Roughness is a random quantity and is commonly specified in terms of the rms (root mean square) height *h* of the surface unevenness for the Hammerstad and Groisse compensation methods. Huray modeling is based on a non-uniform distribution of stacked copper nodules shapes resembling “snowballs”.

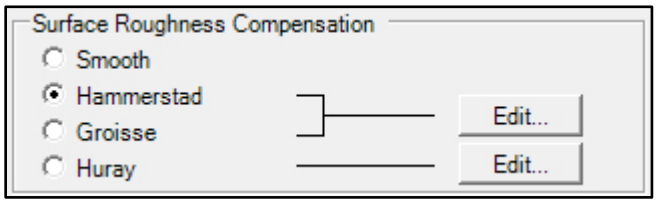
Surface roughness compensation methods
Accurate calculation of conductor loss requires the surface roughness parameters for each method:

The Smooth copper option provides for no compensation for copper loss.

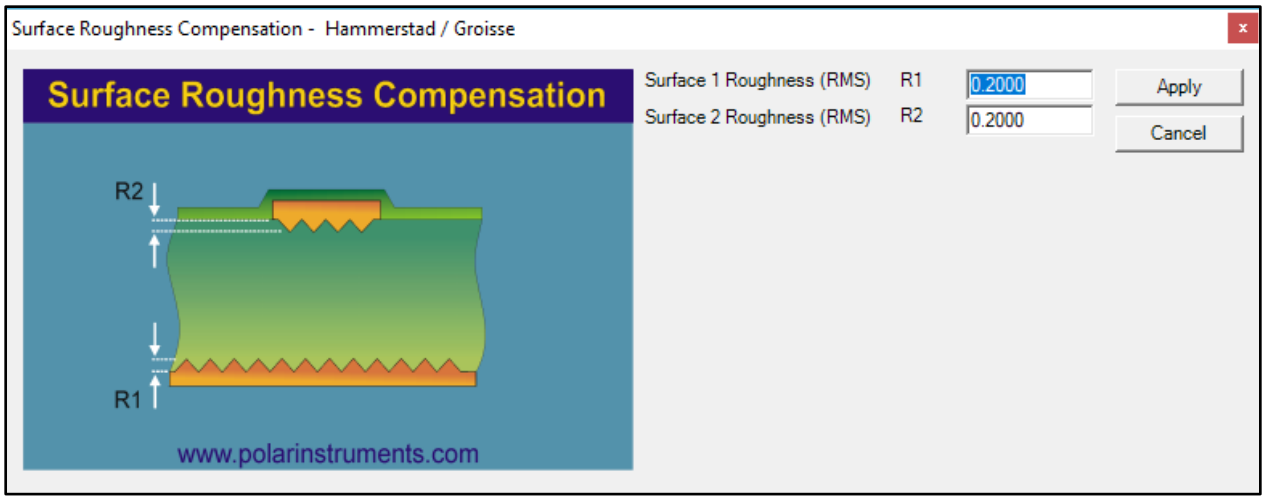
Hammerstad modelling is a proven technique that has stood the test of time but has practical limitations when used over 4GHz as the model tends to saturate.

Groisse modeling can, with care, be used to extend the modelling up to 7 to 10 GHz before saturation in the model blunts its accuracy.

Hammerstad/Groisse methods
To specify the roughness parameters for the Hammerstad or Groisse methods, click the option button for the method:



Click the Hammerstad/Groisse Edit button.

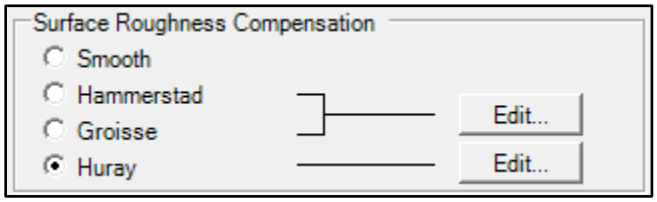


Enter the values for roughness in the R1 and R2 fields and click Apply. Click Calculate to refresh results.

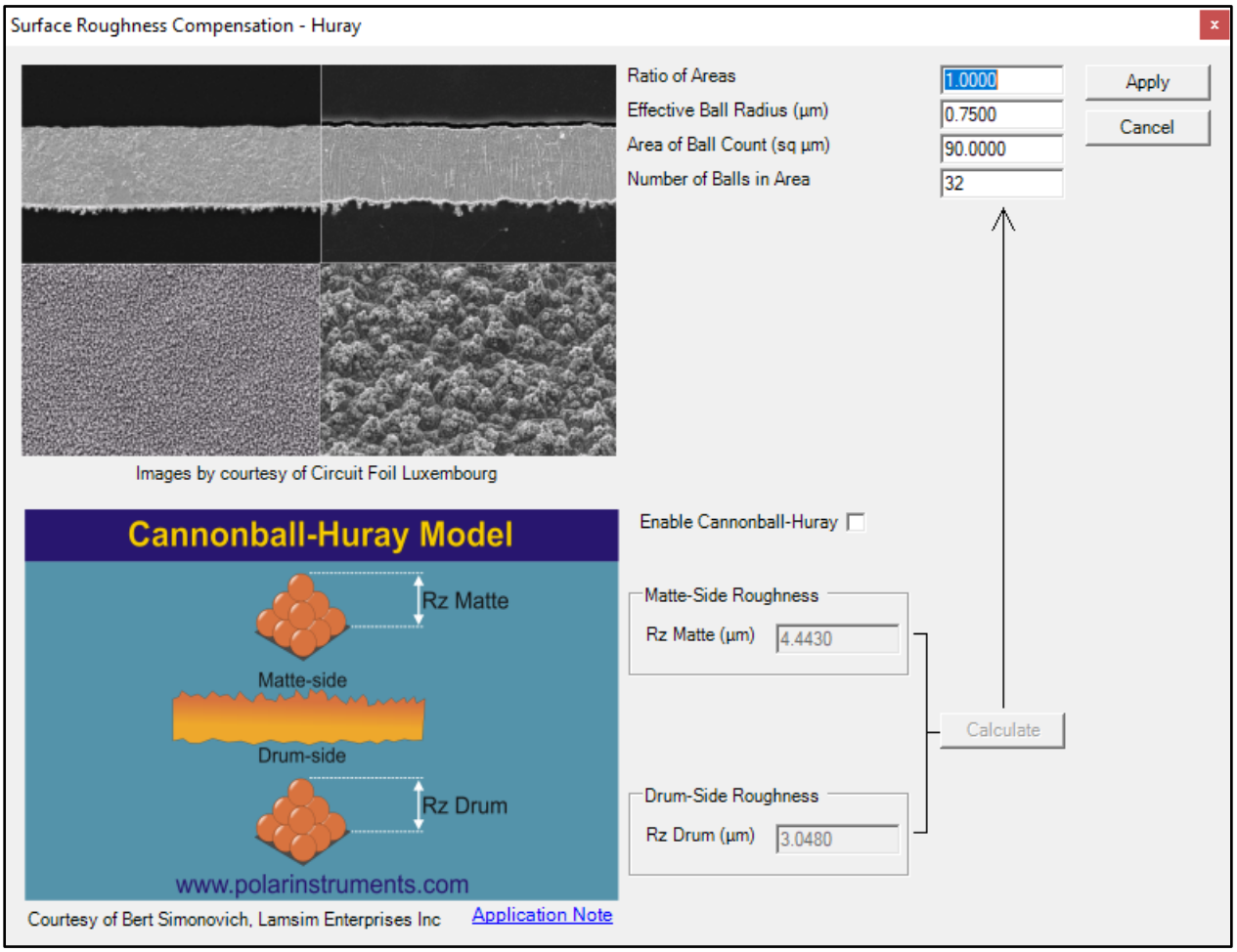
Huray method

Huray modelling extends the roughness modeling validity up to 40 to 50GHz (and possibly beyond).

Click the Huray option button:



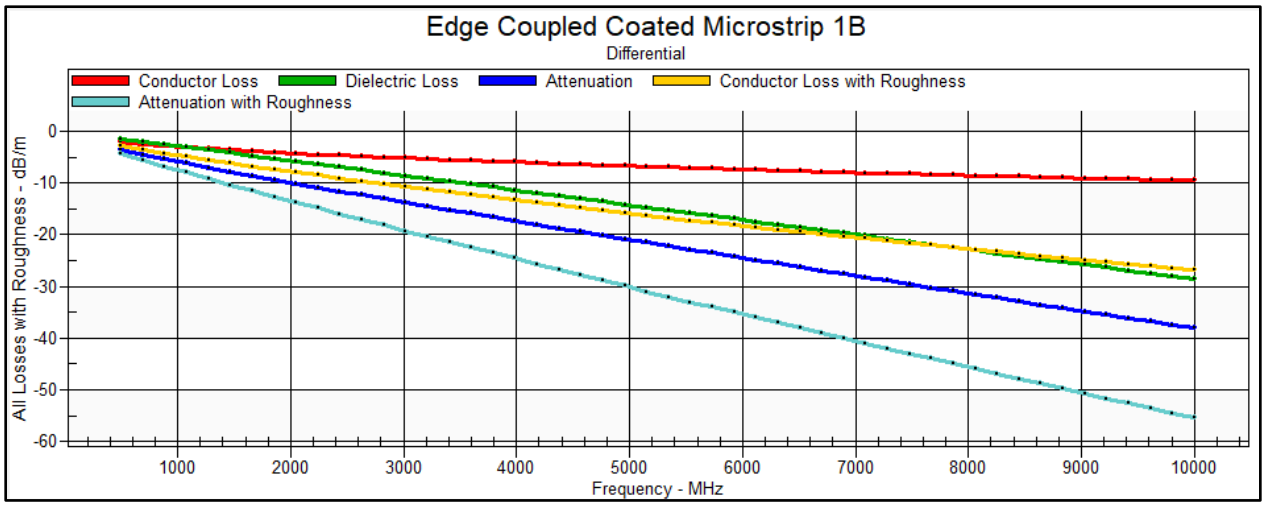
Click the Huray Edit button and specify the parameters for the Huray spheres (snowballs.)



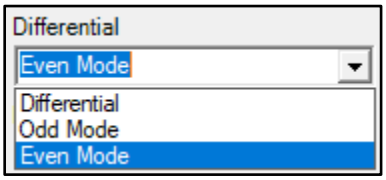
Supply the values in the associated fields and click Apply.

If the Huray values are not available, click Enable Cannonball-Huray and supply the Rz values for matte and drum side roughness and click Calculate to populate the Huray fields, then click Apply.

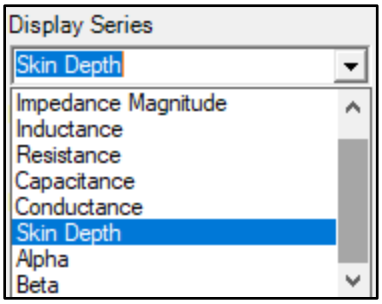
Click the Application Note link to access the paper *Practical Modeling of High-speed Channels Based on Data Sheet Input* (Bert Simonovich, LamSim Enterprises Inc.) which includes a description of roughness modelling using the Cannonball-Huray Model.



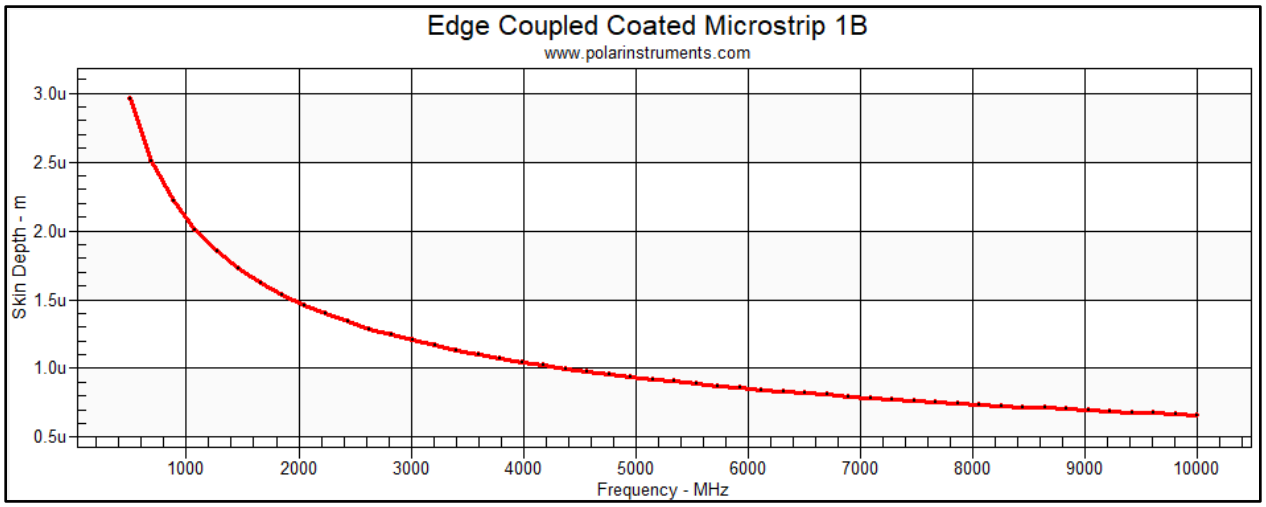
Speedstack charts a range of data series, including losses, impedance magnitude, inductance, resistance, capacitance and conductance; for differential structures select the transmission line mode, differential, odd or even mode.



Click on the Display Series drop down to select the data to be charted.



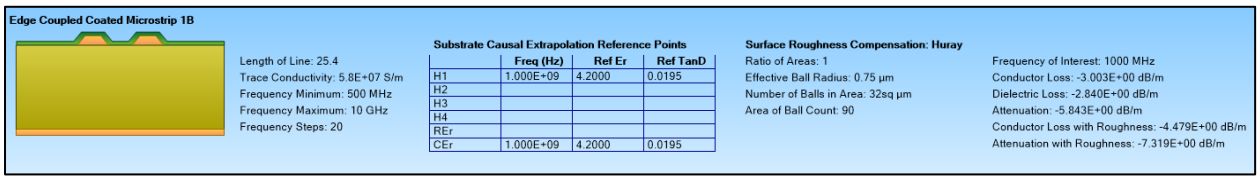
The chart below displays skin depth v frequency



Printing the technical report

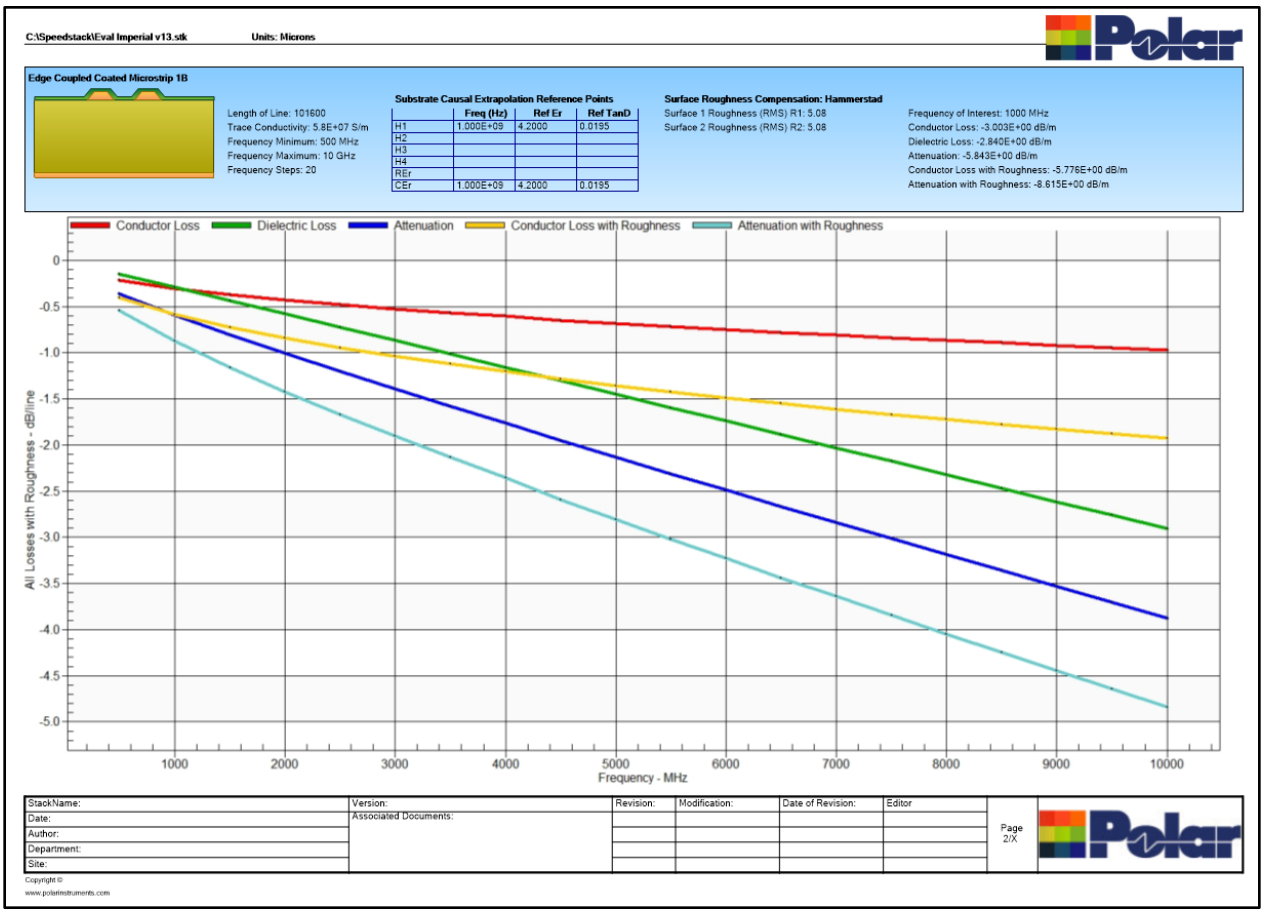
The Speedstack Si technical report includes the stackup with its stack data, the controlled impedance structures and structure data, the drill data and loss data for each structure in the stack.

Displayed loss data for each structure reflects the structure type, the frequency dependent parameters, the substrate causal extrapolation reference points, the surface roughness method and settings, frequency of interest and associated loss values for dielectric and conductor losses and total attenuation and losses with roughness.



Click File|Print|Print Technical Report, Speedstack refreshes the loss data results and displays them in high quality graphical form.

Step through the pages to view the stack, impedance and drill data and the frequency dependent loss graphs for each structure in sequence in the stack.



Speedstack Si to Si9000e data transfer

Speedstack and Si9000e incorporate the facility to realise bidirectional transfer of all structure parameters (i.e. both lossless and frequency dependent) for a single structure or all structures via the clipboard.

Parameter transfer is accomplished via the data transfer icons:

Single structures

To Field Solver

Use Speedstack's To Field Solver icon to transfer the parameters of a single structure via the clipboard from Speedstack to the Si9000e

From Field Solver

Use Speedstack's From Field Solver icon to transfer the parameters of a single structure via the clipboard from Si9000e to Speedstack

Paste Structure from Speedstack

Use the Si9000e's Paste Structure from Speedstack to paste the whole structure with all its parameters into the Si9000e – the currently displayed structure will be replaced

Copy Structure to Speedstack

With all calculations complete click the Copy Structure to Speedstack to return the structure to the stackup in Speedstack.

Multiple structures

To Si Project

Use Speedstack's To Si Project icon to transfer all structures as a project from Speedstack to the Si9000e

Paste from Speedstack into Si Project

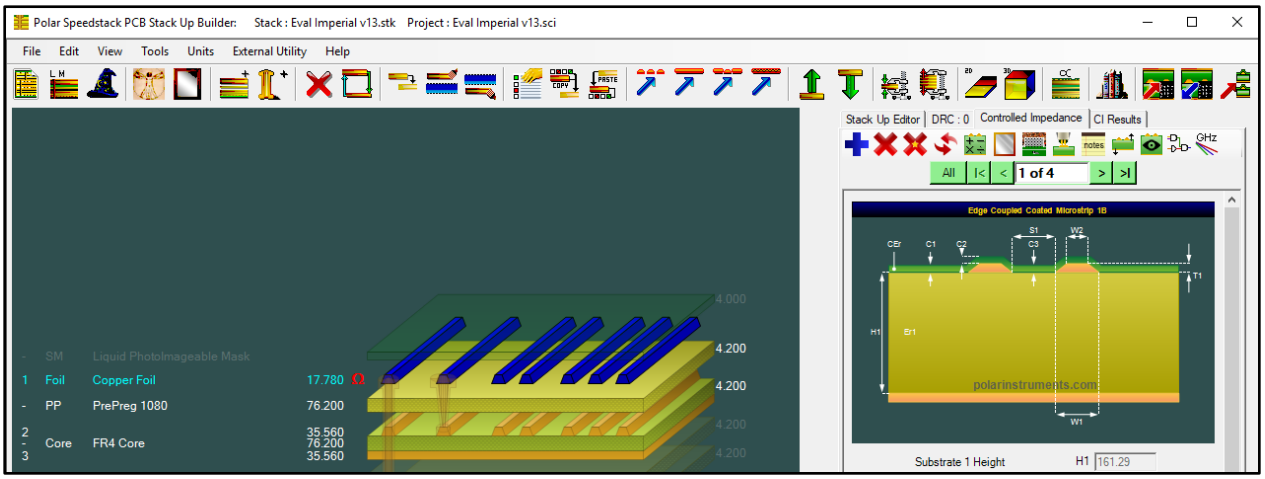
Use the Si9000e's Paste from Speedstack into Si Project to paste the set of structures into the Si9000e as a project.

Sharing structure properties

Each structure in Speedstack can store a complete set of frequency dependent parameters, so each structure can have its own Length of Line, range of frequencies (FMin, FMax, FSteps and Frequency of interest) substrate data, surface roughness compensation and loss budget.

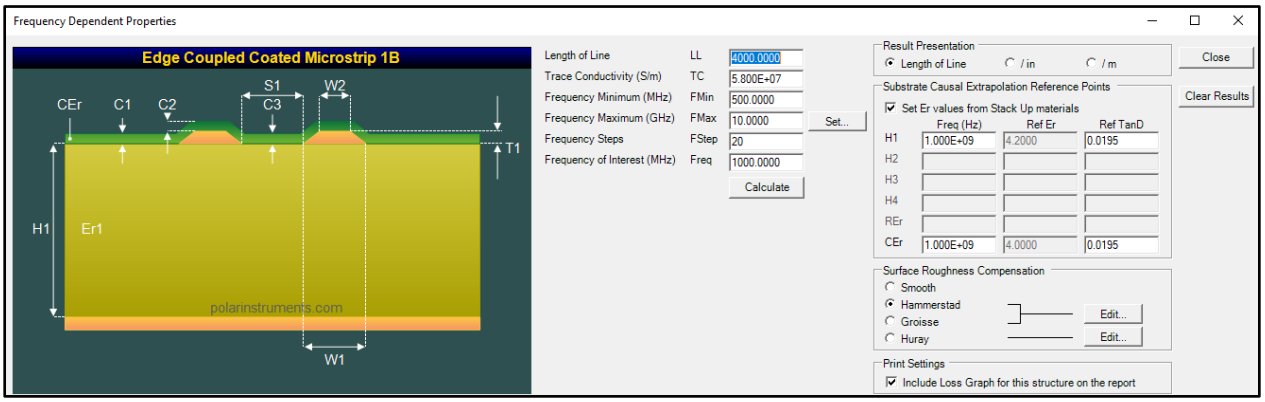
Using the data transfer icons within Speedstack allows a selected set of structure properties to be shared between other structures on the same electrical layer on the stackup.

To share parameters between structures, select the source structure (structure 1, Edge Coupled Coated Microstrip 1B.)



Frequency Dependent Properties

Select the Frequency Dependent Properties button to display the frequency dependent properties.



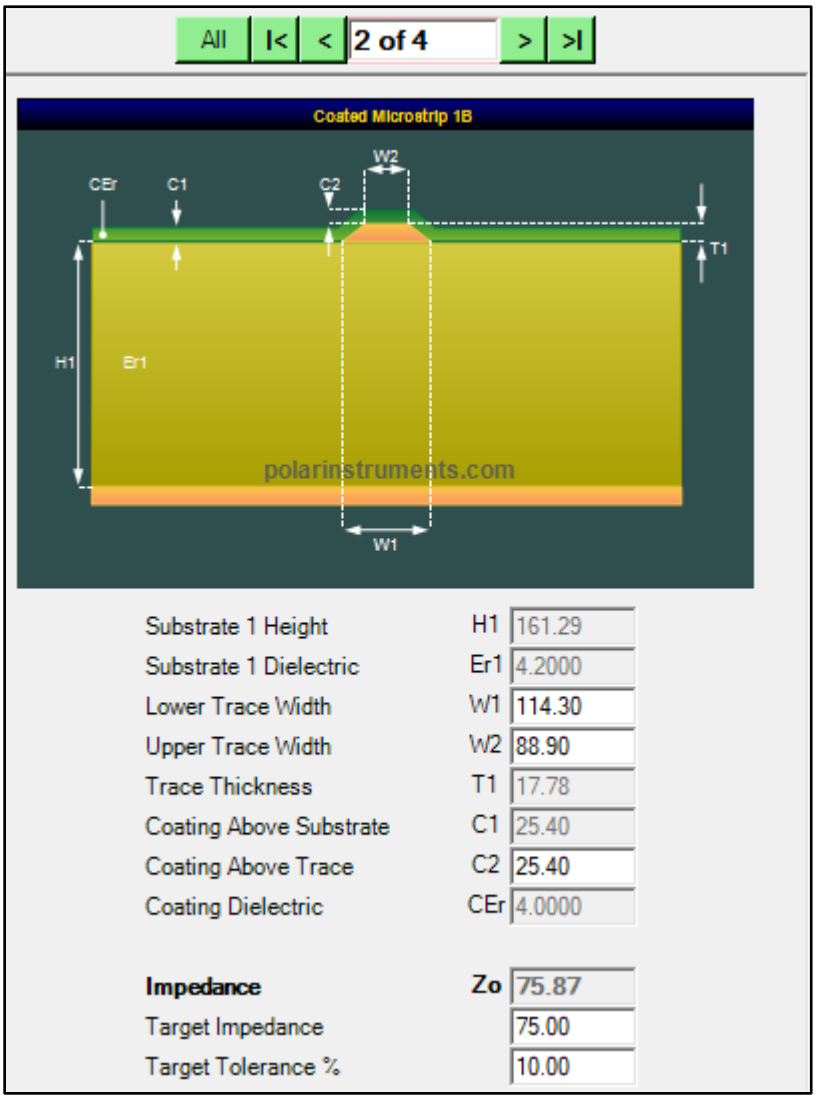
All the structure's properties, including all the frequency dependent parameters, will be available for sharing with the target structure.

To Field Solver

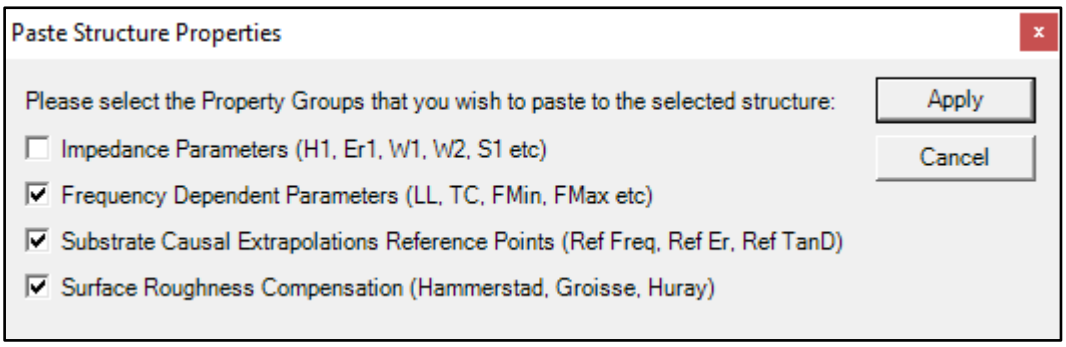
Close the dialog and click the To Field Solver button to copy the parameters to the clipboard.

From Field Solver

Select the target structure (in this example, structure 2, single ended Coated Microstrip 1B as shown below) and click the From Field Solver button.



Speedstack displays the Paste Structure Properties dialog



Select the properties to be pasted – in this case, the impedance parameters are unchecked as the source structure's 100 ohm differential impedance does not apply.

The frequency dependent parameters, along with the causal extrapolation reference points (frequency, Er and TanD) and surface roughness compensation method are applied to the target structure.

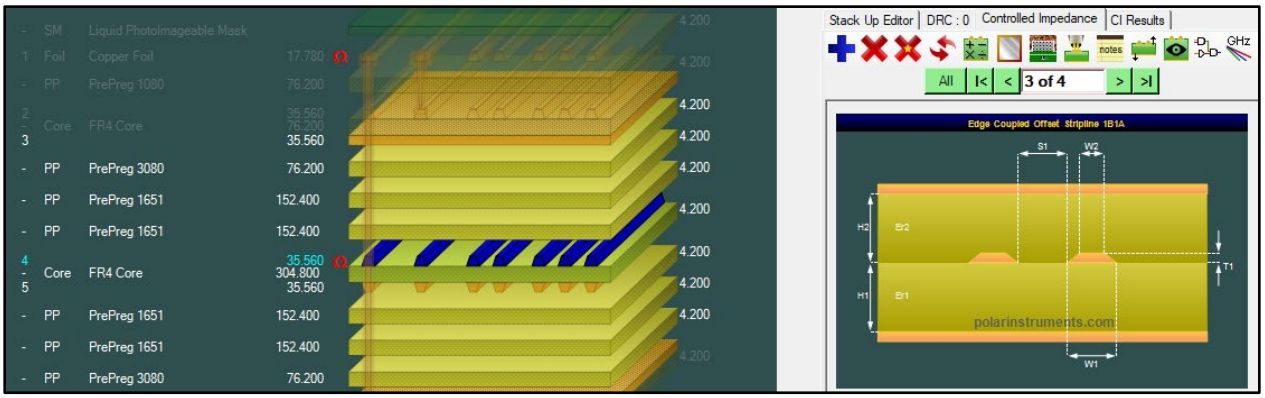
Transferring structures between Speedstack and Si9000e

Speedstack Si is fully integrated with the Si9000e transmission line field solver.

Users can transfer structures to the field solver for processing then transfer the solved properties back to Speedstack Si.

Transferring a single structure

Ensure the field solver is running. Select the structure to be copied to the Si9000e




To Field Solver

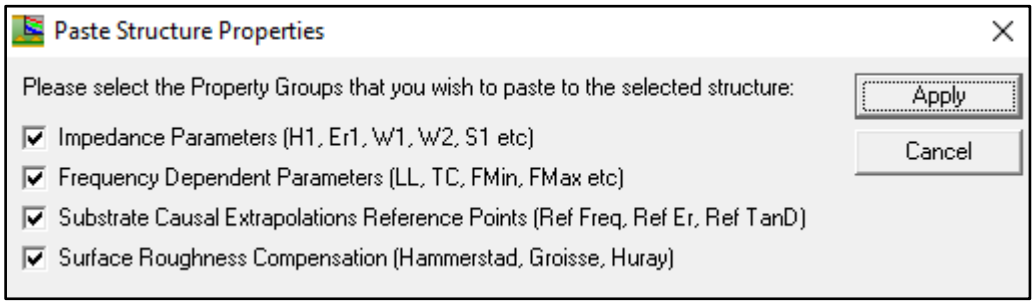
Click the To Field Solver button to transfer the structure and all parameters to the Si9000e.

Switch to the Si9000e.


Paste Structure from Speedstack

Click the Si9000e's Paste Structure from Speedstack button to paste the structure complete with all impedance and frequency dependent parameters into the Si9000e.

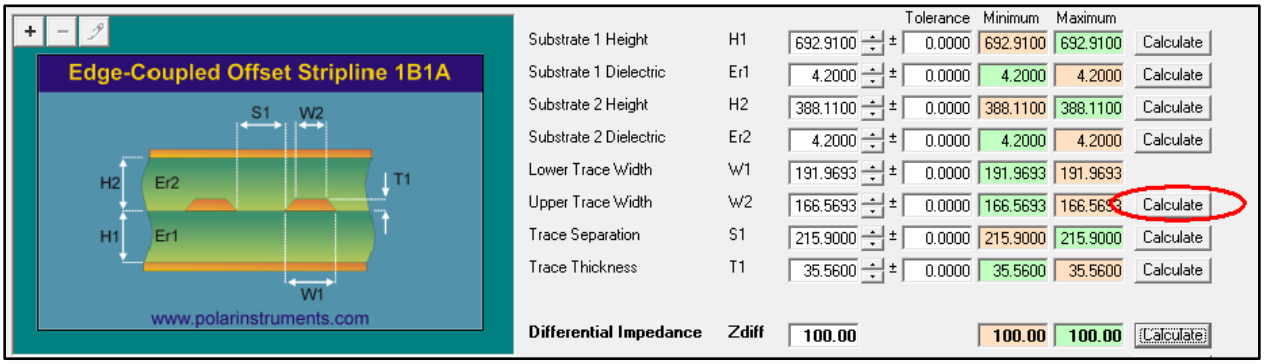
The Si9000e displays the Paste Structure Properties dialog.



Choose which groups of properties are to be pasted into the field solver and click Apply. The impedance, lossless and frequency dependent properties are pasted into the field solver for processing. The units setting in Speedstack will replace the setting in Si9000e.

Solving for impedance

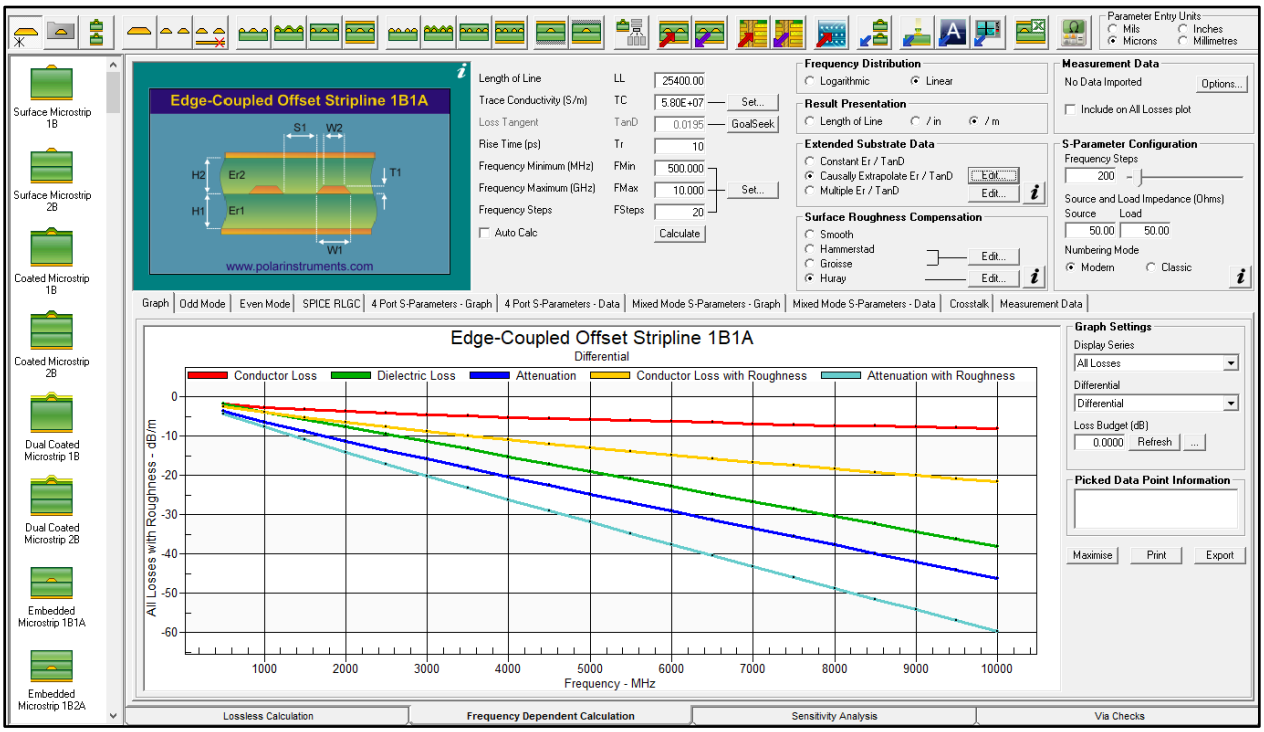
With the structure loaded into the Si9000e switch to the Lossless Calculation tab to display the structure graphic and lossless parameters.



Specify the target impedance then click the Calculate button for the parameter to be used in the goal seek (e.g. trace width); with the target impedance reached switch to the Frequency Dependent Calculation tab.

Running frequency dependent calculations

Enter the frequency dependent parameters, the extended substrate data settings, the surface roughness compensation method and values and click Calculate to refresh the results.

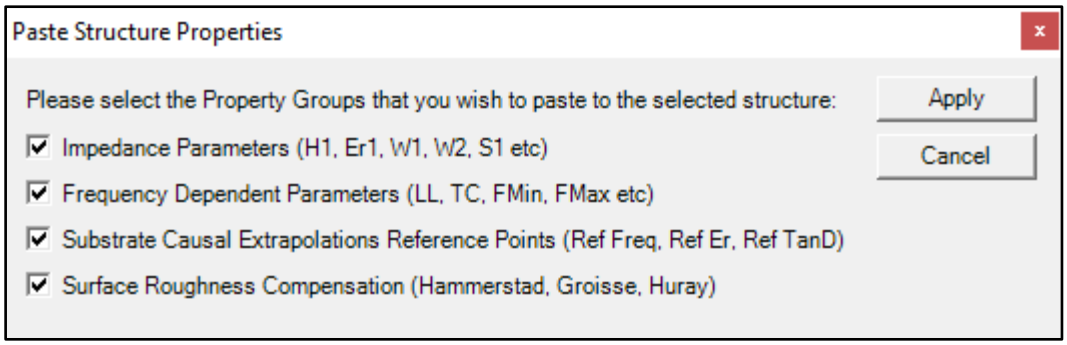


For detailed Si9000e operation see the Si9000e User Guide.

Copy Structure to Speedstack

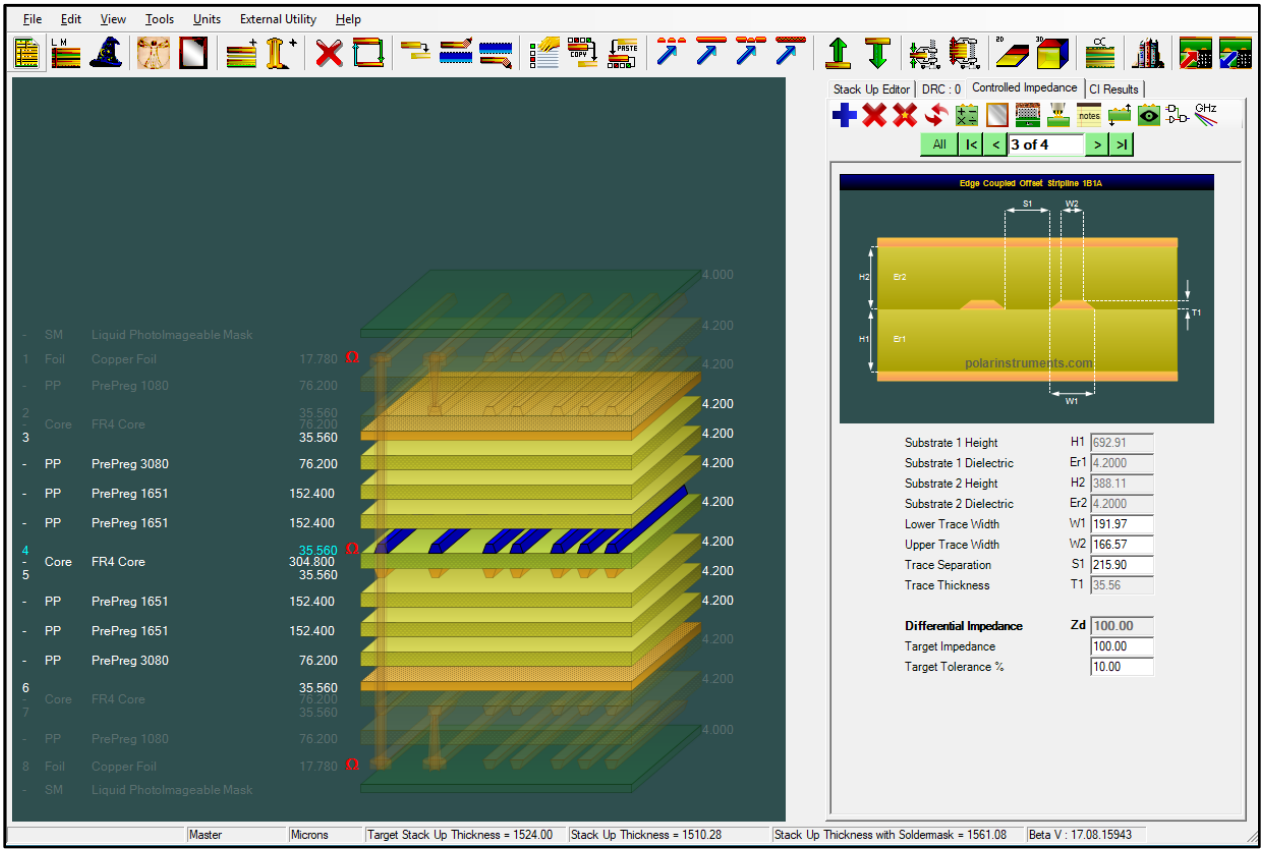
With all calculations complete click the Copy Structure to Speedstack to return the structure to the stackup in Speedstack.

The Paste Structure Properties dialog is displayed.



Choose which properties are to be updated and click Apply.

Rebuild and calculate the structure in Speedstack. The structure reflects the updated values.



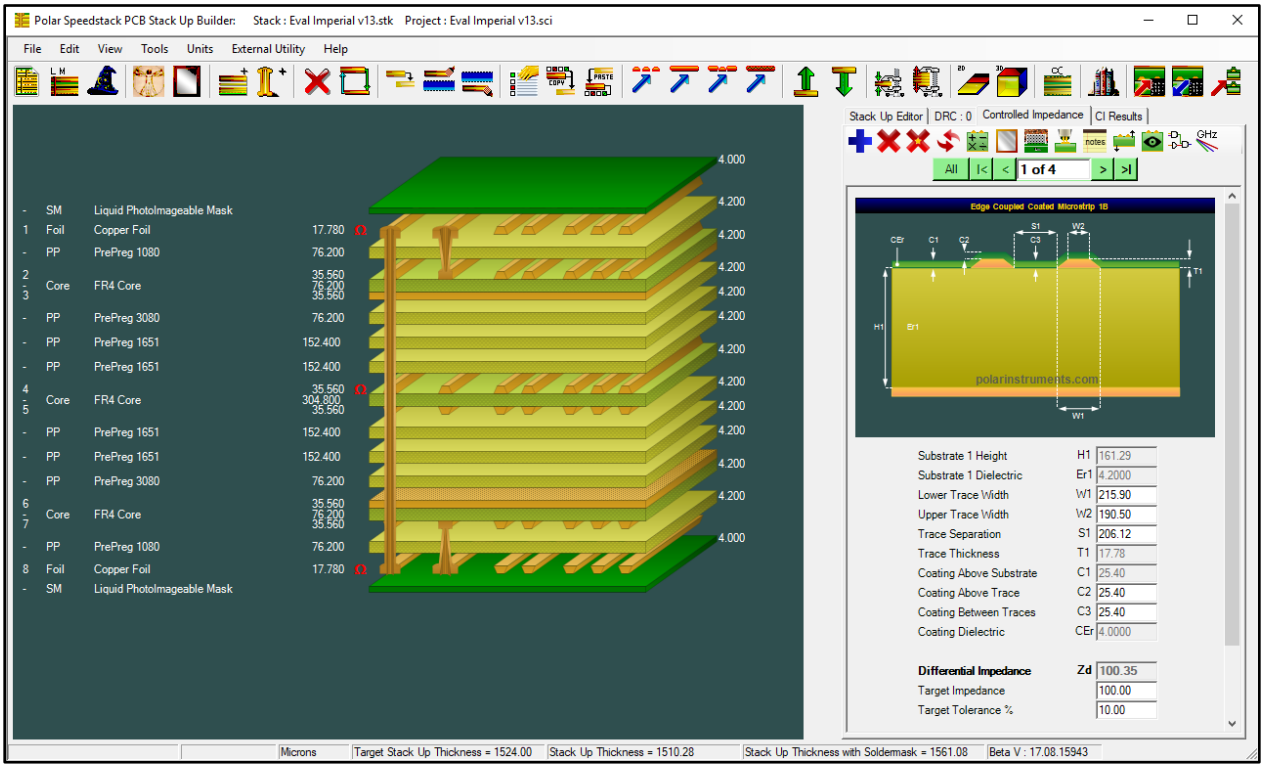
Transferring multiple structures via Si Projects

To transfer all the structures in a stack use the Si Projects transfer function incorporated in Speedstack Si and Si9000e.

Si Projects allows for transfer of all controlled impedance structures along with all lossless and frequency dependent parameters from Speedstack Si into the Si9000e field solver.

Si Projects allows groups of structures to be saved and recalled in Si9000e and the updated structures pasted back into Speedstack.

The stackup in the example below contains four structures.

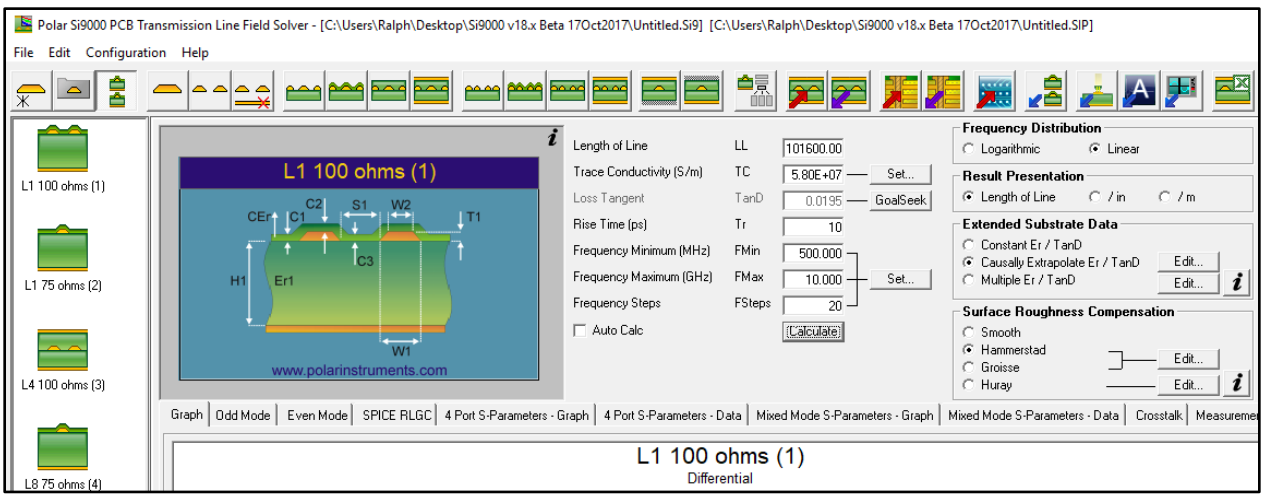


To Si Project

Use the To Si Project toolbar icon to copy the group of four structures from Speedstack Si and place them onto the clipboard; these structures can then be pasted directly into the Si9000e as a new project.

Paste from Speedstack into Si Project

Switch to the Si9000e and use the Si9000e's Paste from Speedstack into Si Project to paste the set of four structures into the Si9000e as a project.



The Si9000e and Speedstack should automatically switch to the units that were in use when the structure was copied. (For instance, if Speedstack is in Mils and Si9000e is in Microns and a structure is copied from Speedstack to Si9000e the Si9000e should automatically switch to Mils.)

The complete set of structures appears in the field solver's Project window in the same order as shown in Speedstack.

The Si Project window lists the transferred structures in Speedstack's display order, showing the order number and impedance value along with a thumb nail graphic indicating the structure configuration.

Modifying structures

Selecting each structure displays its associated graphic in a grey background.

With a structure selected the structure parameters can be modified as required and all values recalculated. The recalculated structures can be pasted back into Speedstack.

To paste a structure back into Speedstack select the target structure in Speedstack, switch to the Si9000e, select the structure for transfer and use the transfer icons to update the selected structure in Speedstack.

Rebuild and Recalculate Displayed Structure

Click the Rebuild and Recalculate Displayed Structure to refresh the displayed structure.

Rebuild and Recalculate All Structures

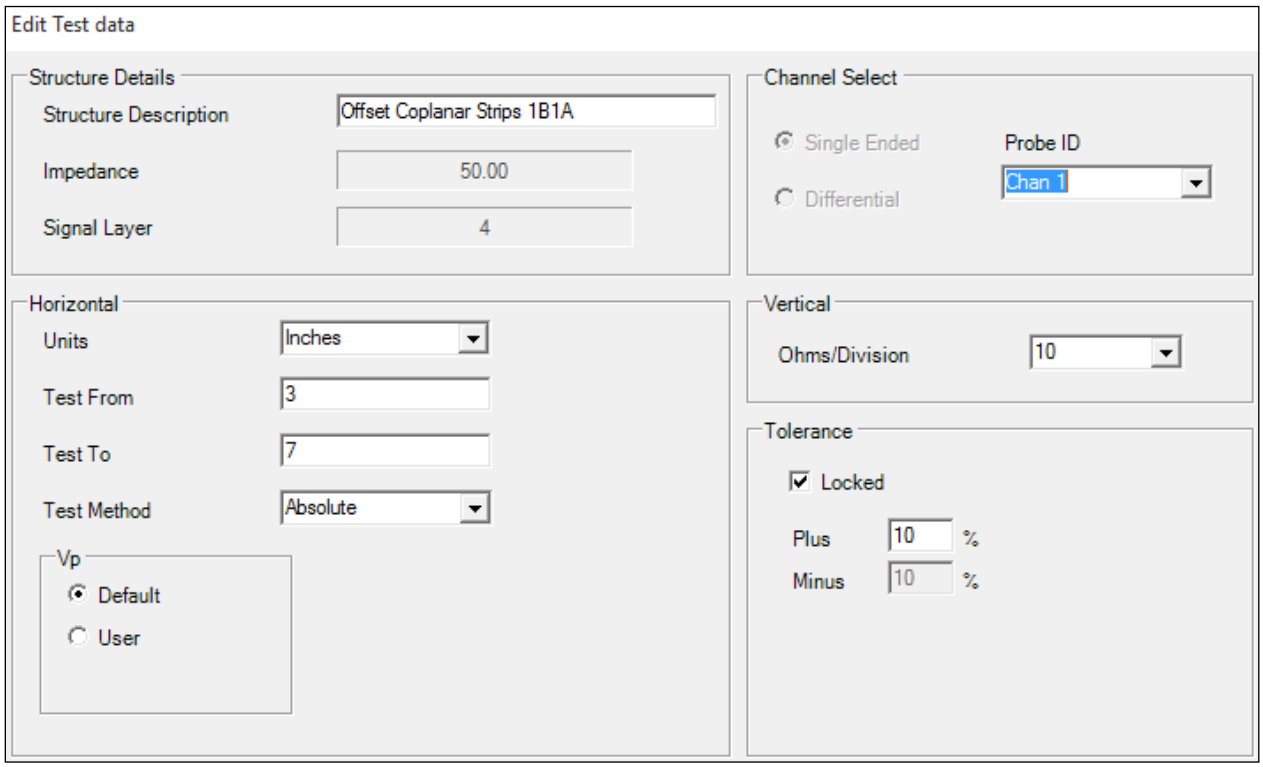
Click the Rebuild and Recalculate All Structures to update all structures in the stack

Creating CITS test files

Speedstack can create CITS test file data for each controlled impedance structure in the stack.

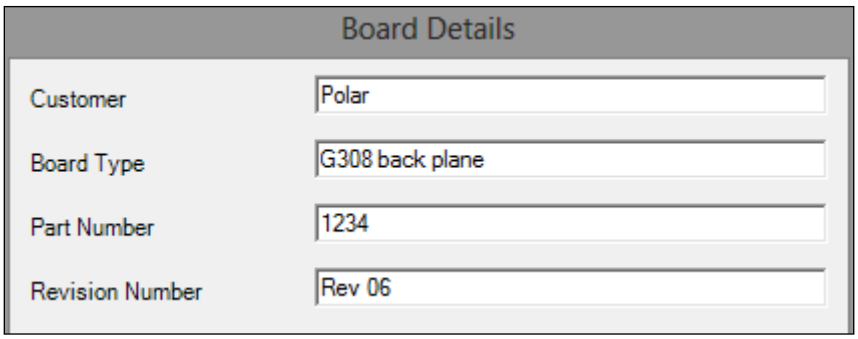
Set CITS Test

Select each structure and click Set CITS Test to display the Edit Test data dialog; specify the CITS test parameters for each structure to be tested and click OK.



Exporting the CITS test file

With the test data specified for each structure, from the File menu choose Export To|Export CITS File. Add descriptive Board Details and notes as required.



Click Make File and navigate to a suitable folder and save the CITS (.cif) test file.

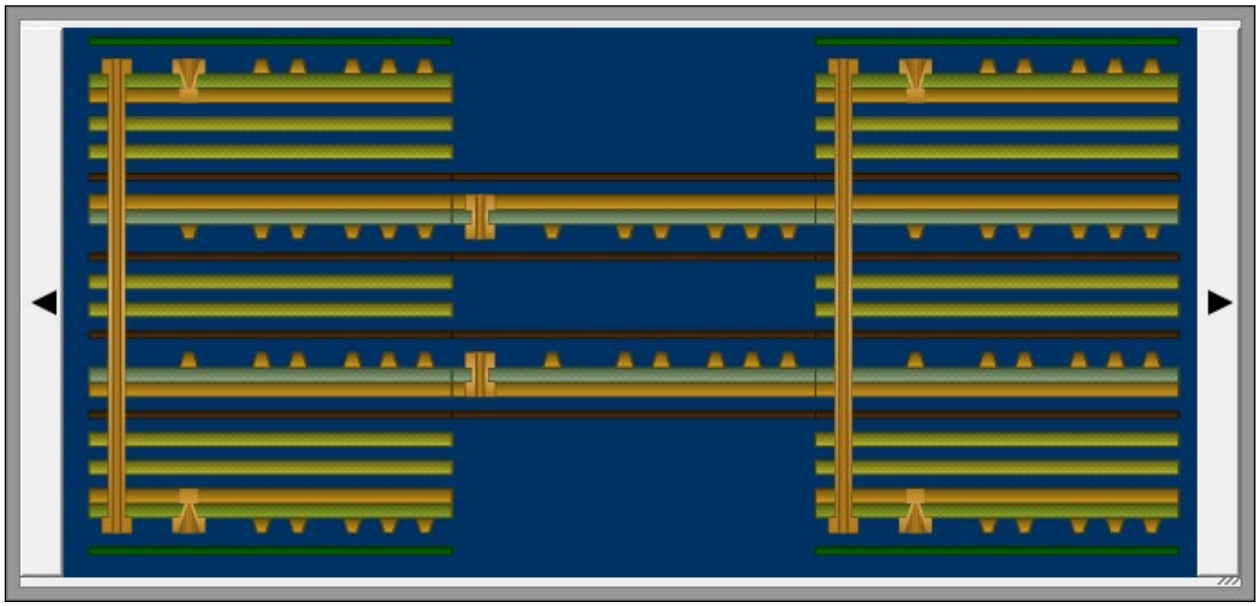
Working with flex-rigid stackups

Speedstack Flex

Speedstack Flex allows PCB fabricators and OEM engineers quickly to create and document accurate and efficient flex-rigid PCB layer stackups.

The graphical stackup display
The Speedstack Flex Navigator enables the board designer to link and document as many cross sections as necessary in order to fully document a flex-rigid build up.

Speedstack Flex supports documentation of common flex-rigid constructions, including *doublets* where stacked pairs of flex link two rigid sections of the flex-rigid construction together (see graphic below.)



Speedstack's Navigator works from a master stack comprising the full set of materials used in the final stackup and documents each rigid and flex-rigid section with as many "sub-stacks" as needed for the design. There are no limits to the number of sub-stacks or layer count of the total build.

A range of materials including flexible adhesives, bondply and FlexiCore can be enabled or disabled for each layer, and impedance structures can be added to each sub-stack.

Mesh / Crosshatch ground planes

When used with Polar's Si8000m and Si9000e field solvers, Speedstack Flex permits modelling and documenting mesh/crosshatch ground planes from within the Speedstack Flex environment. Mesh geometry and structure data can be easily shared between Si8000m and Si9000e.

Internal Coverlays

Advanced rules allow impedance structures to be added when coverlays exist internally within a stack. When a coverlay is beyond the outer copper it will behave like a coating, when internal it will behave like a bondply or prepreg.

Definable colours per material

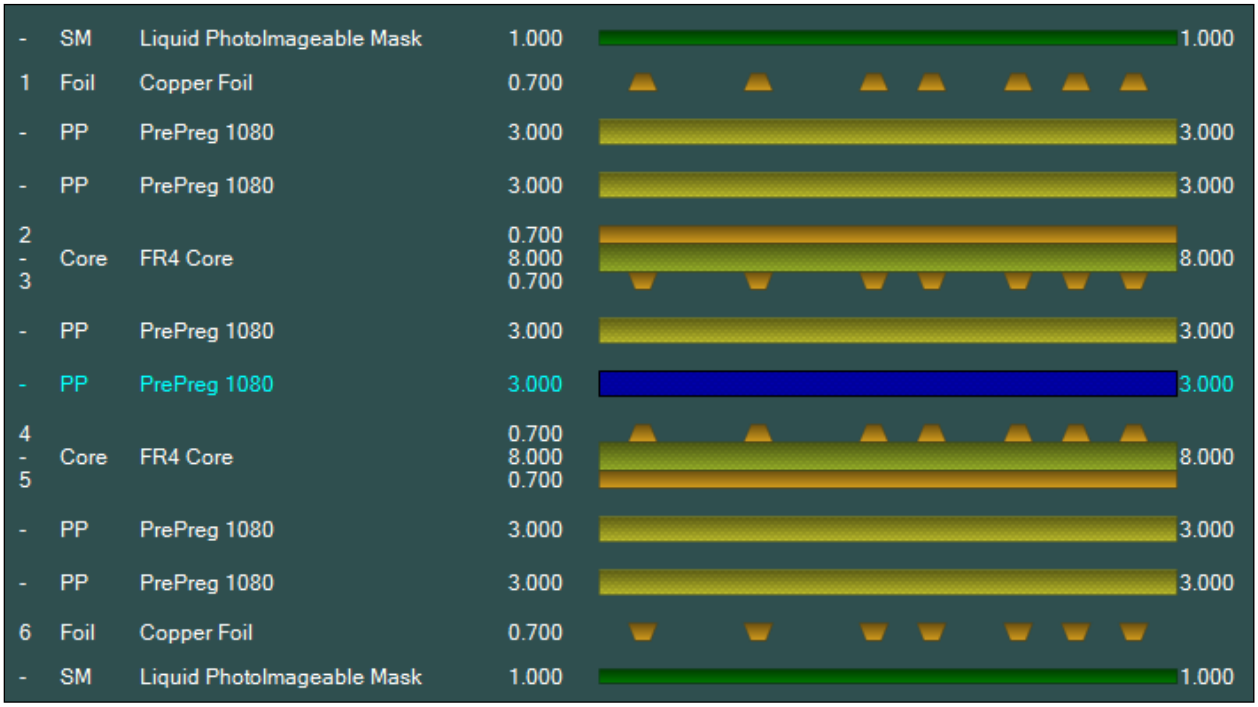
Speedstack Flex can set and store individual material colours via the material Properties dialog. This will help ensure that special build requirements are obvious during fabrication. This will be found useful for documenting plated layers or highlighting specific material usage such as no-flow prepregs and flexible cores.

Enabling Speedstack Flex/HDI

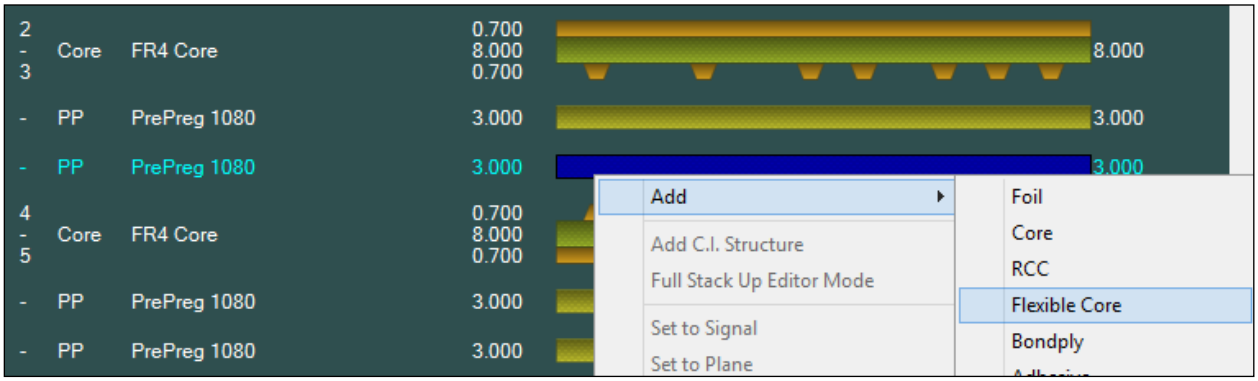
To enable Speedstack Flex/HDI select Tools|Options and ensure the Licensing pane purchasable option Speedstack Flex/HDI License check box is ticked.

Adding a flexible core

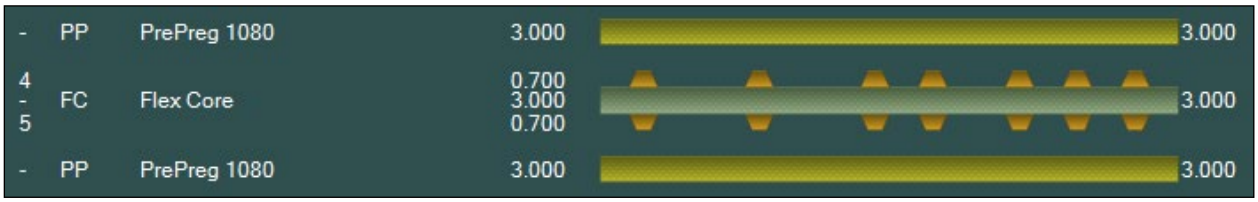
Create and save a symmetrical 6-layer stackup as shown in the sample stack below



Ensure Symmetrical mode is off, right click the prepreg above Layer 4 copper and add a flexible core:

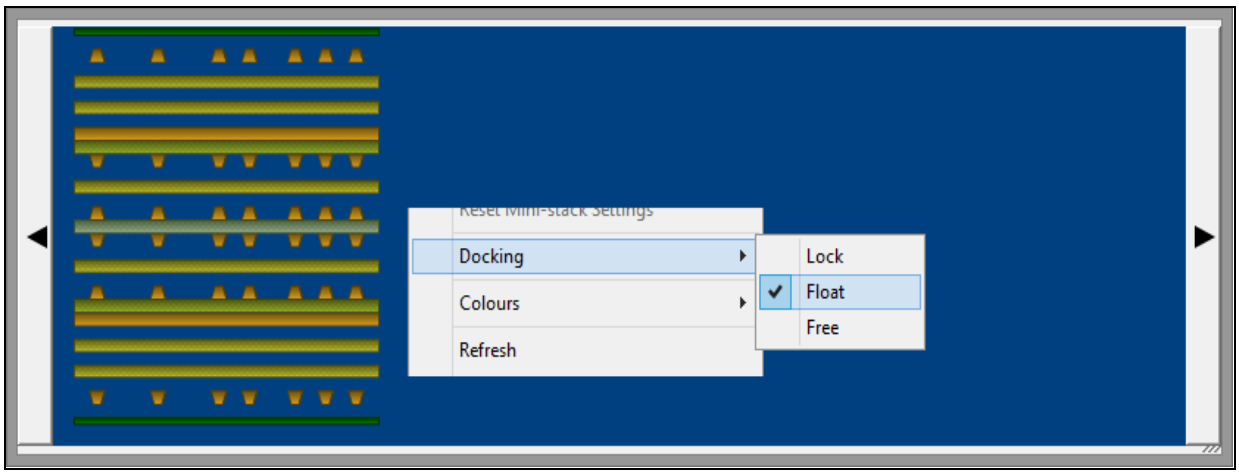


The flexible core is added as the new layers 4 and 5.



Using the Navigator

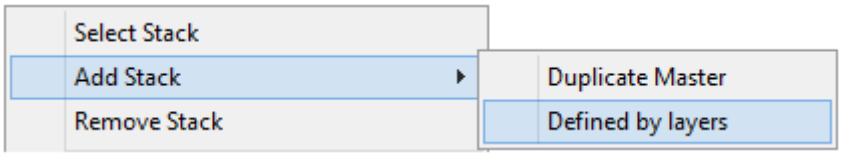
Press F4 to display the Navigator



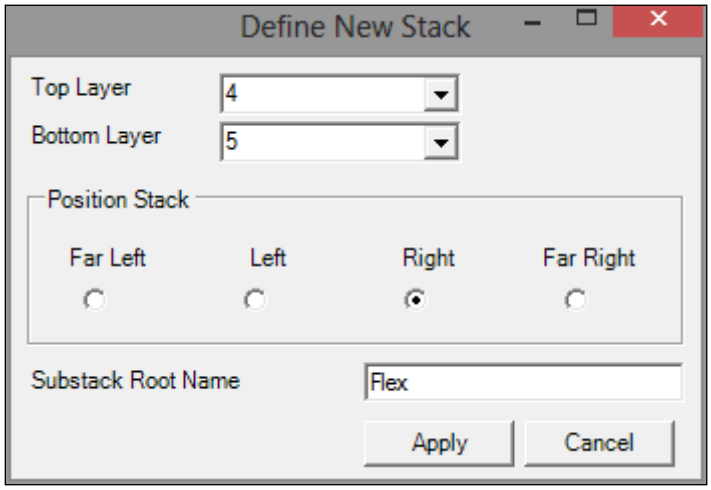
Right click the Navigator and choose Docking|Float to allow the Navigator window to be resized. The Navigator will move with Speedstack's Stack Editor. Choose Free to allow the Navigator to move independently of the Stack Editor.

Adding stacks

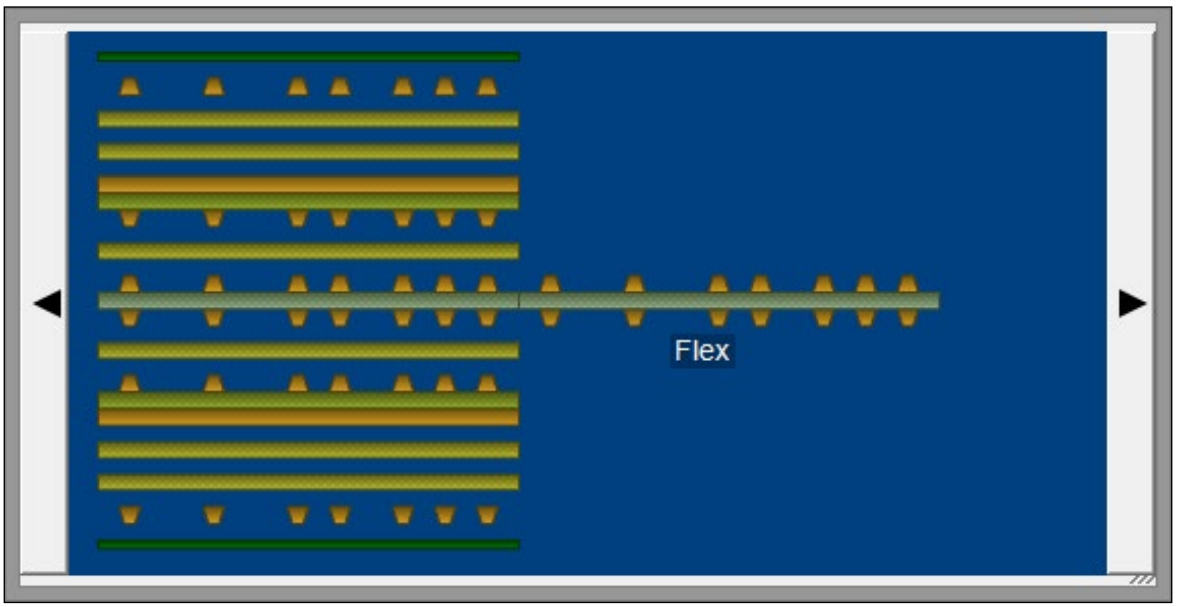
Select the stack in the Navigator window and click Add Stack and choose Defined by Layers



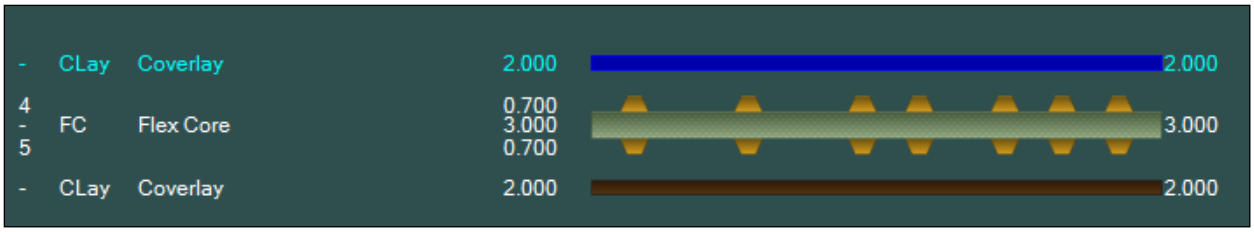
From the drop-down list choose Layer 4 as the Top Layer and Layer 5 as the Bottom Layer as shown below and enter Flex as the Substack Root Name.



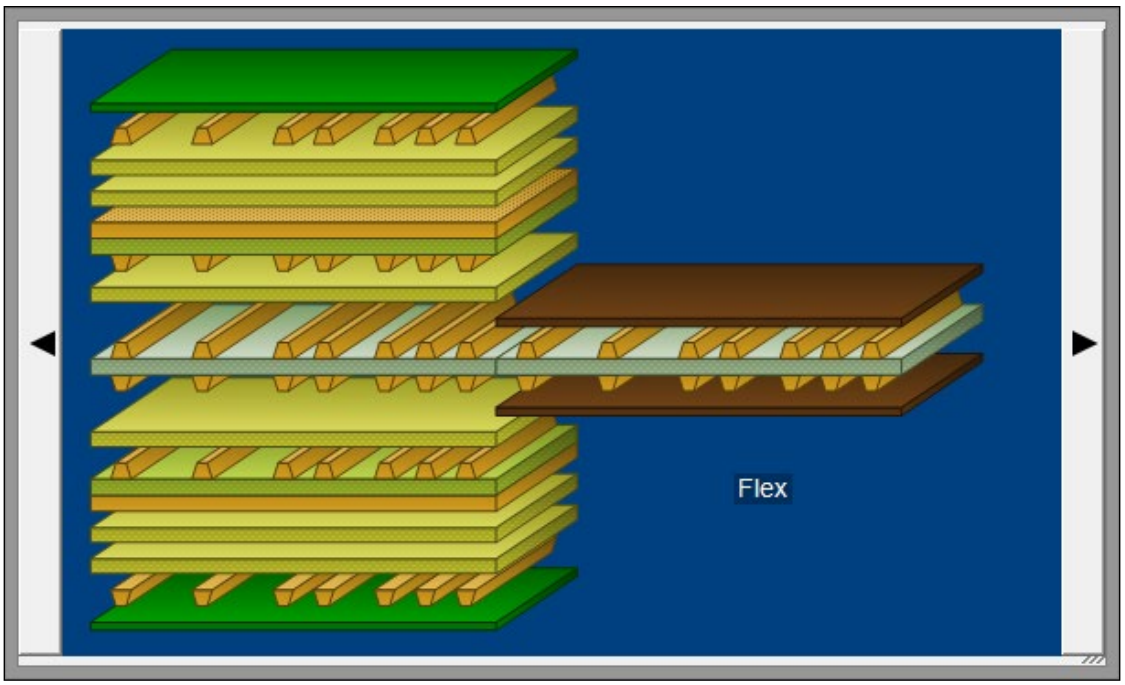
The new stack is added to the Navigator. Each sub-stack can be renamed individually as required.



Click the new stack – the selected stack is reflected in the Stack Editor and listed in the status bar. Select Symmetrical mode, in the Stack Editor click the new core and add a coverlay above.



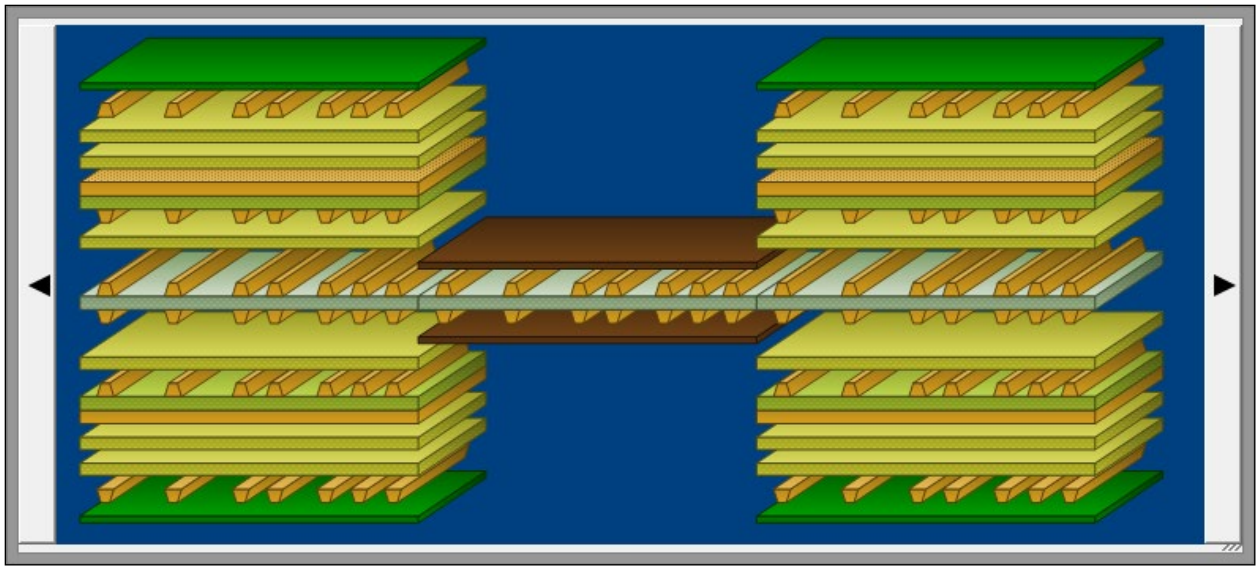
The coverlays are added symmetrically about the core. Changes made in the Stack Editor are reflected in the Navigator. Click into the Navigator – use the mouse wheel to resize. The Navigator can display in 2D or 3D views.



The new stack with its added materials appears in the Navigator; clicking each stack in the Navigator displays it in the Stack Editor and allows editing as described earlier to add controlled impedance structures, change layer types, add non-copper layers, etc.

Adding a new stack

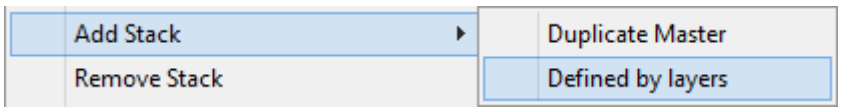
Right click the Navigator and choose Add Stack|Duplicate Master, rename the new stack and click OK.

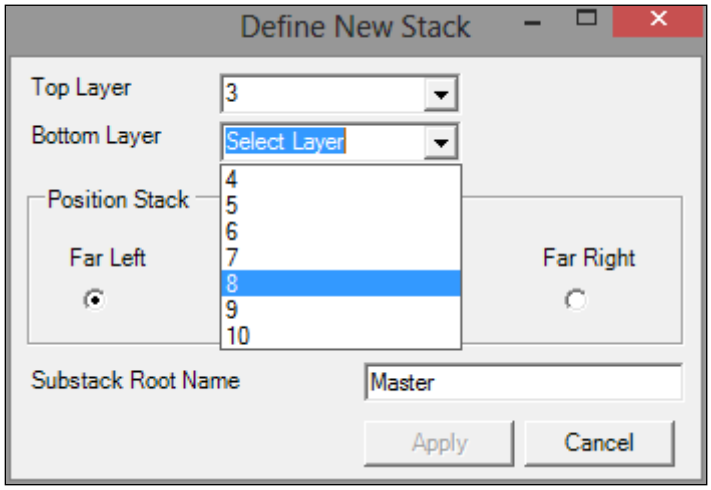


The new stack is added to the Navigator. Click on each stack to display it in the Stack Editor and then edit as required.

Defining new stacks

New stacks may be added defined by layers of the master stack. Choose Add Stack|Defined by Layers:

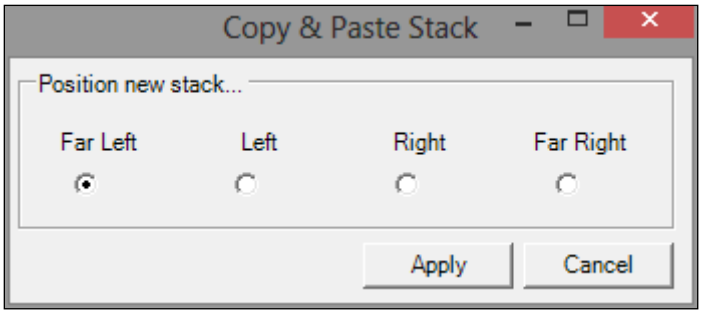




Choose the starting and finishing layers and specify a position for the new stack, choose a descriptive sub-stack root name and click Apply.

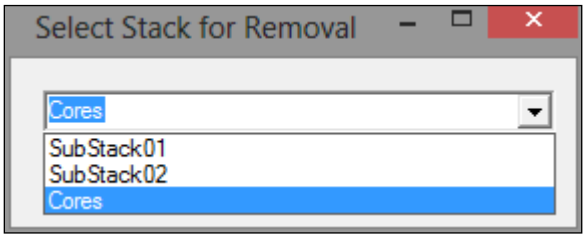
Copying and pasting stacks

To copy a stack in the Navigator select the stack, choose Copy and Paste Stack, then from the dialog below choose the position of the new stack



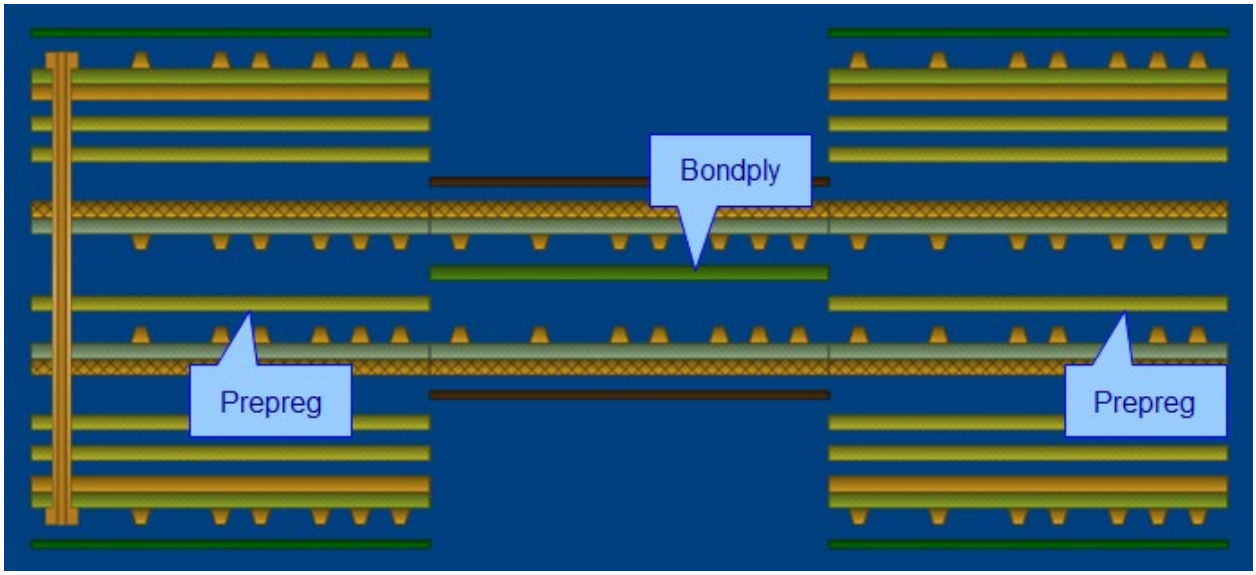
Removing stacks

To remove a stack right click the Navigator, choose Remove Stack and select the stack to be removed.



Aligning materials in the navigator

On occasions, adding a flexible stack results in misalignment between layer materials displayed in the navigator, for example, between the bondply and coverlay layers and the associated prepreg layers – see the graphic below.

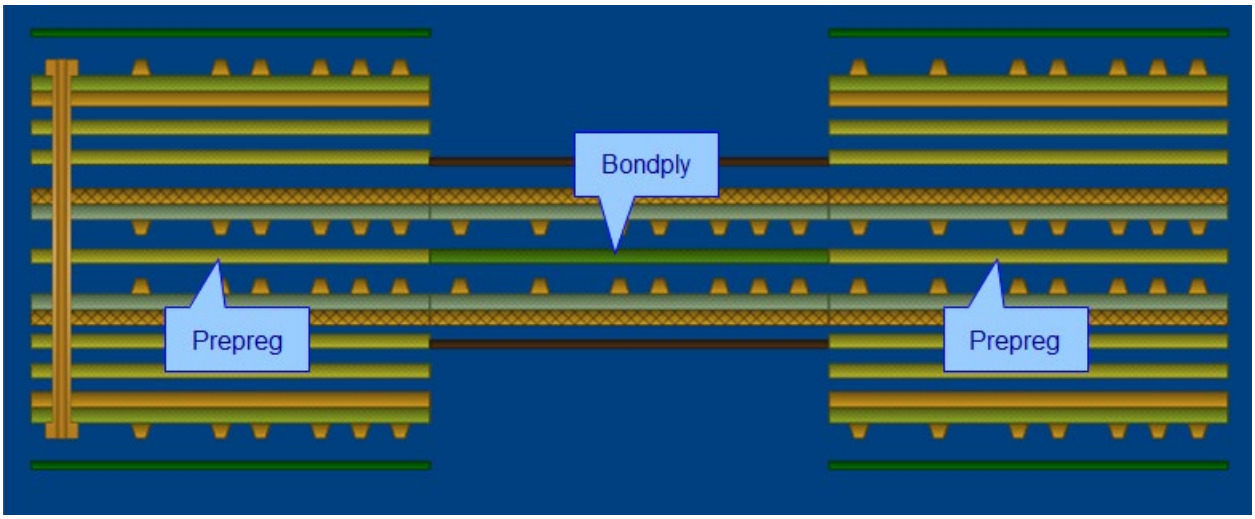


To move the layers into alignment, select the stack in the Stack Editor and use the FlexNav Move Up and FlexNav Move Down commands from the Edit menu.

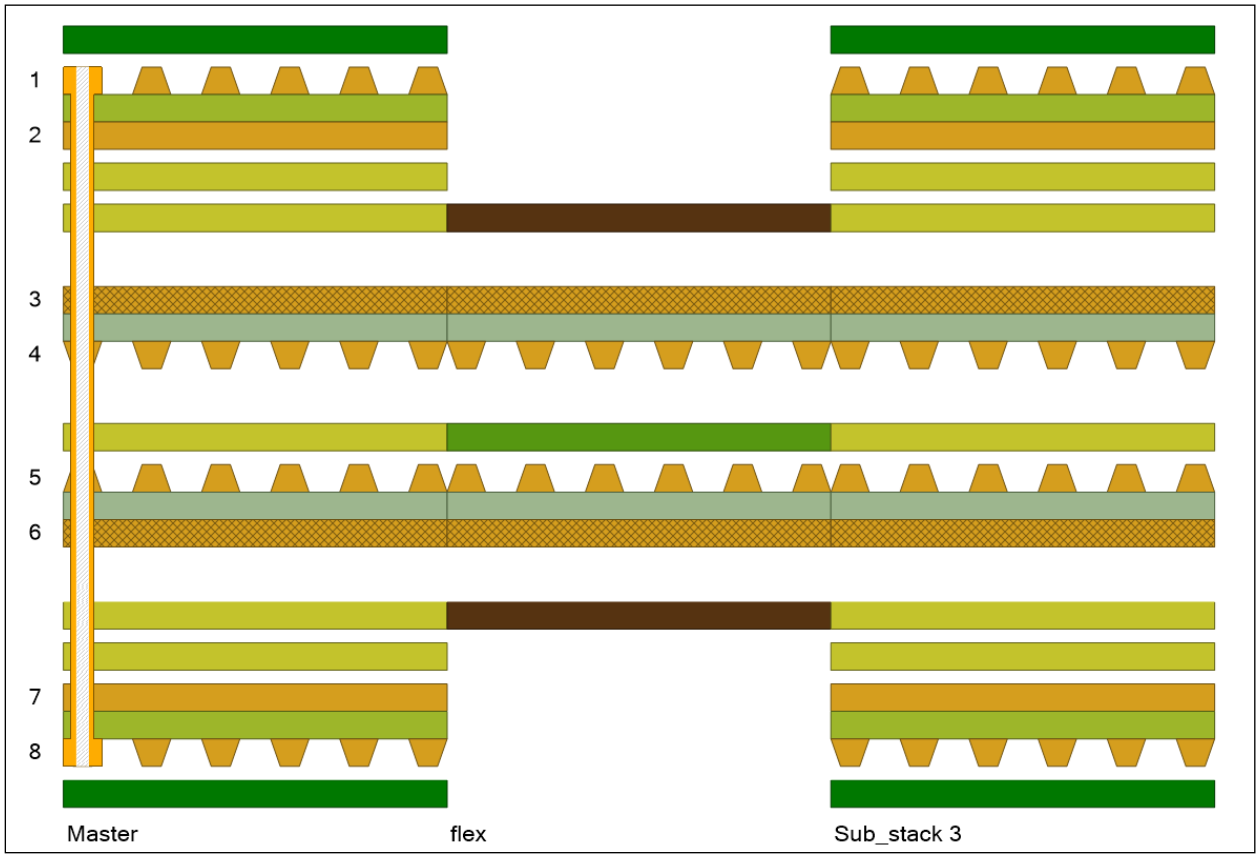
In the example above select the flexible stack in the Stack Editor, select the upper Coverlay layer and shift the layer up into alignment with the prepreg layer in the rigid stack (use the Ctrl + Shift + Up arrow keys)

Repeat the alignment for the bondply and lower coverlay materials (using the Ctrl + Shift + Down arrow keys.) The materials are displayed aligned in the navigator – below.

From the Edit menu Reset All NVDP (Navigator Visual Display Position) Attributes to return the stack to its original alignments.



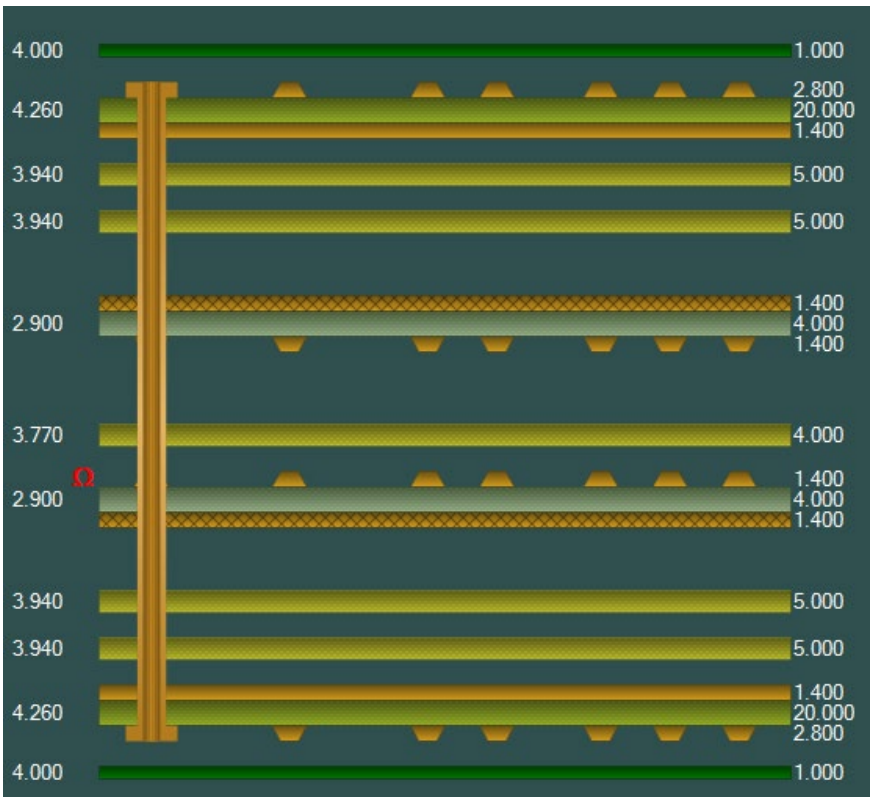
The navigator display is reproduced in the Technical Report



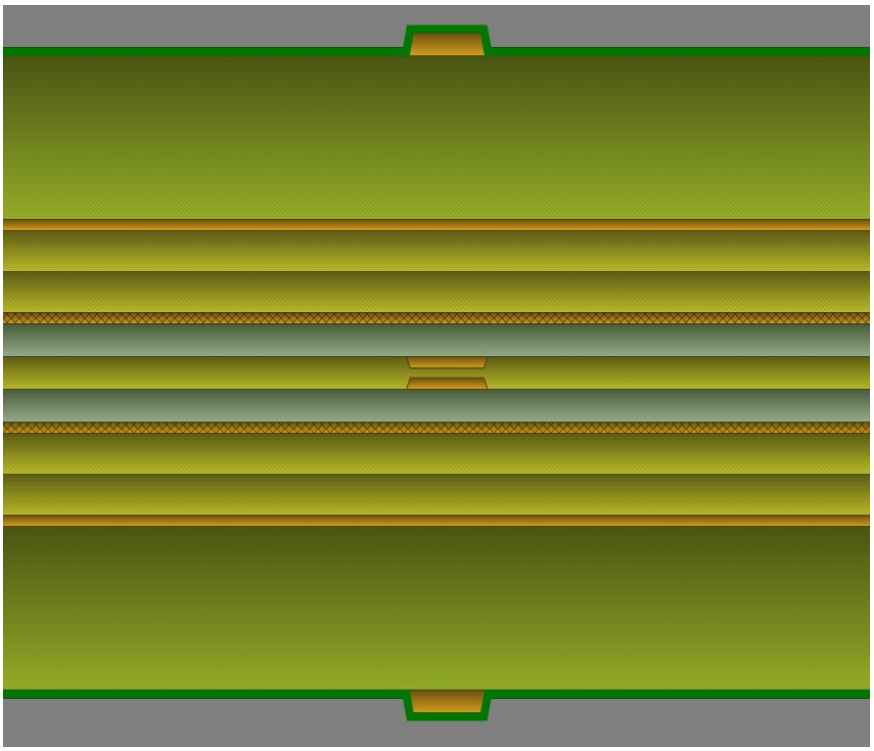
The technical report also supports different materials on the same dielectric layer, improving the clarity of documentation between the stackup designer and fabricator.

Displaying the stack in Proportional View

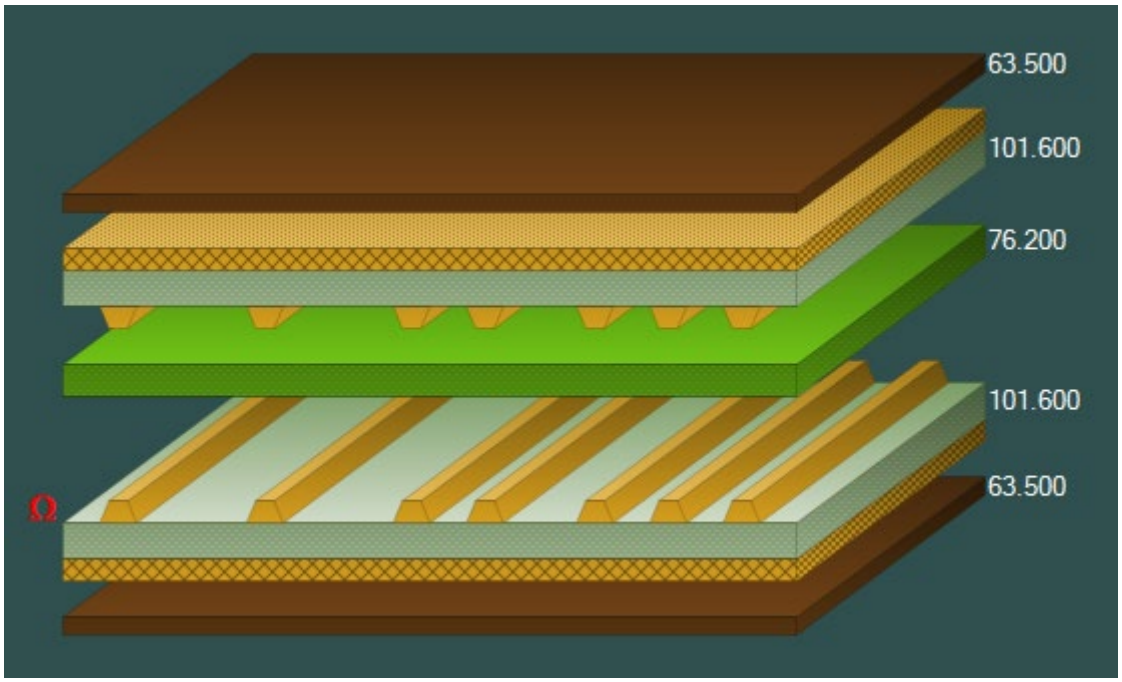
Speedstack can display the stackup so that the material thicknesses are shown proportional to each other. Select the stack in the Stackup Editor and from the View menu choose Proportional Stack Viewer.



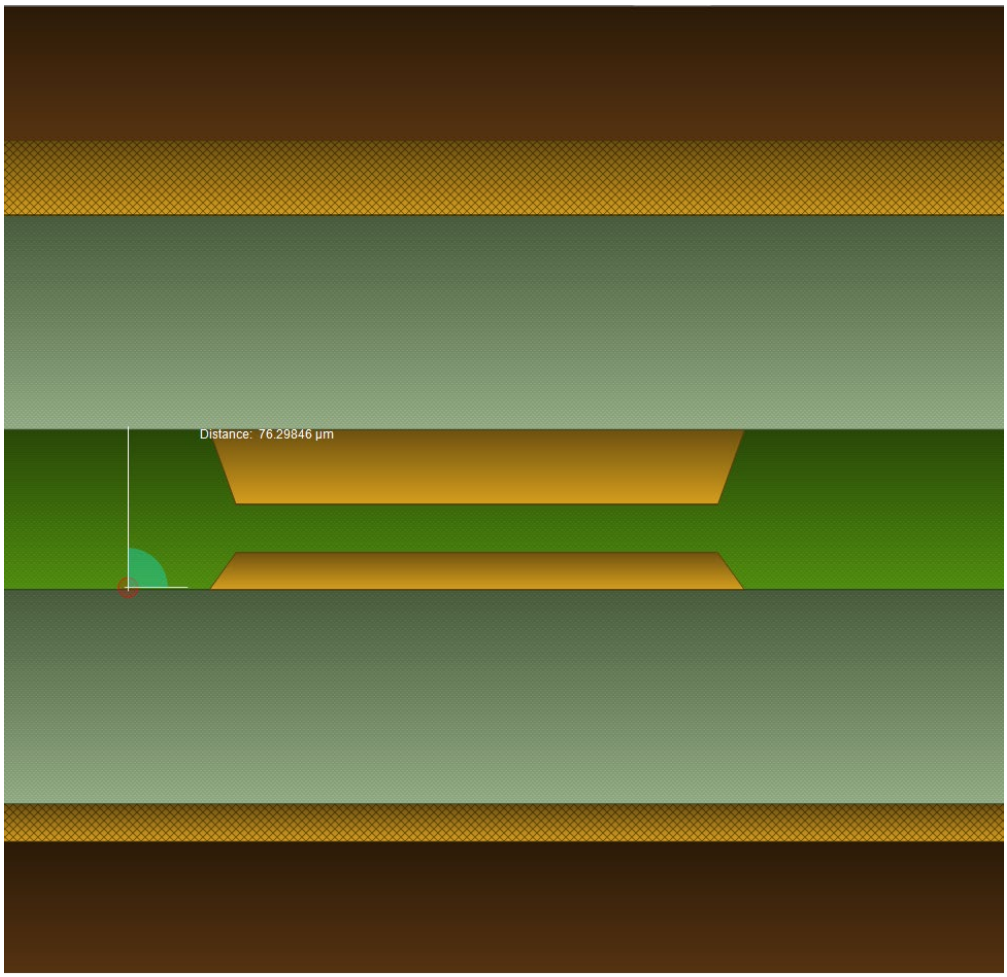
This visual aid will be found useful when considering the dielectric thicknesses between electrical layers.



Using the Ruler within Proportional view
Select the stack in the Stackup Editor



Switch to Proportional View and click the ruler on.



Zoom in as required and use the ruler to measure material dimensions, thicknesses, trace widths, etc.

Working with HDI builds

Speedstack HDI

For HDI PCB fabricators, Speedstack HDI provides the flexibility to quickly calculate the possible impact of substituting alternative materials to improve manufacturability and reduce cost while maintaining the specified parameters and performance of the board.

Easy graphical stackup display

The HDI navigator provides a rapid guide through the sequential sub-stack lamination sequence and presents the complete assembly in a parsed graphical display that shows each phase of the multi-step lamination sequence of an HDI PCB. User-definable settings within the navigator allow engineers to display layers in transparent, invisible or 3D mode.

Sub-stack reordering

Speedstack Navigator makes re-ordering and renaming sub-stacks quick and easy in HDI builds; sub-stacks can be simply moved left or right within the Navigator window.

HDI builds

Use the Speedstack Navigator to document HDI press/drill cycles. Speedstack can document press cycles based on foil locations or drill start and end layers.

Sequential plan

The Sequential plan command creates sub-stacks that represent each press cycle in a sequential lamination from the Master stack based on foil locations.

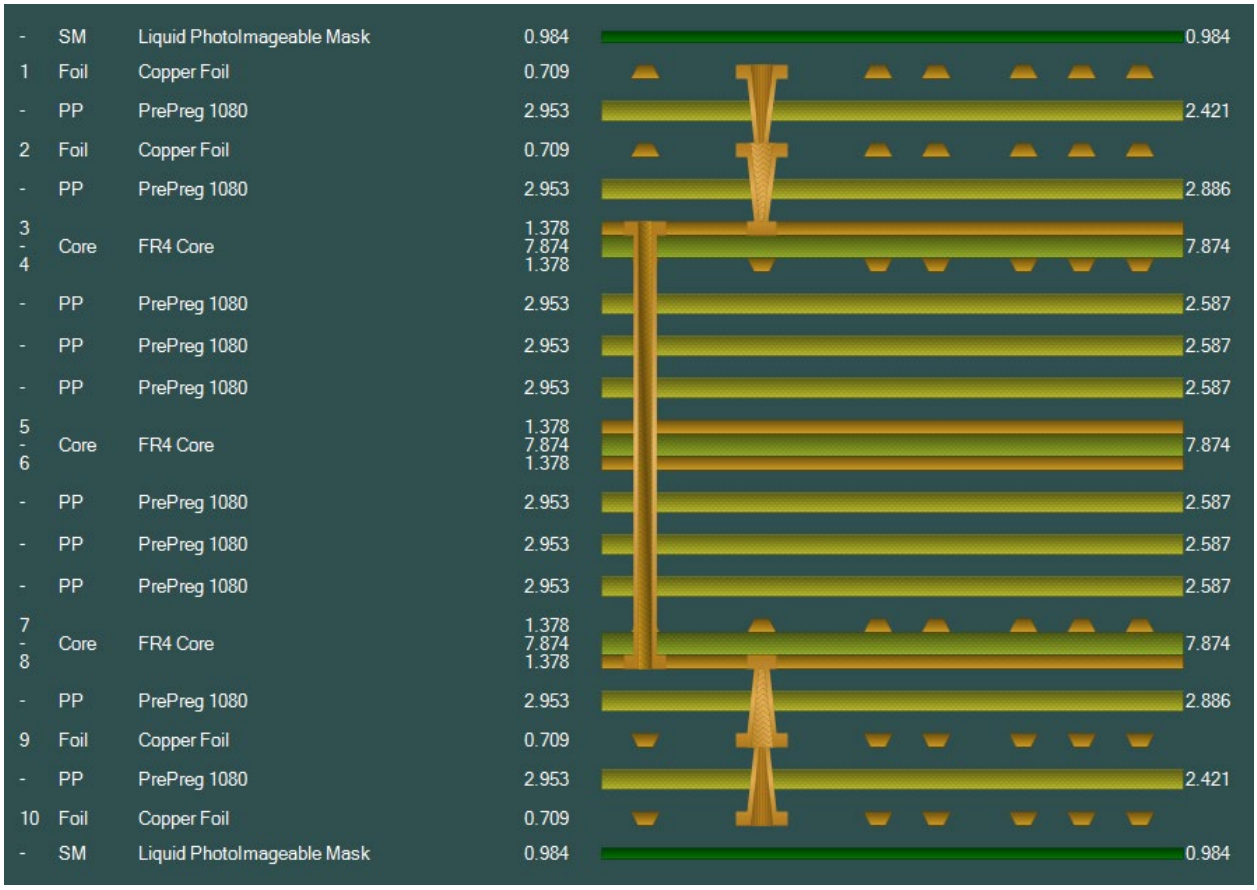
Drill plan

Using Drill Plan, Speedstack determines the sub-stacks by the start / end layers of the drills.

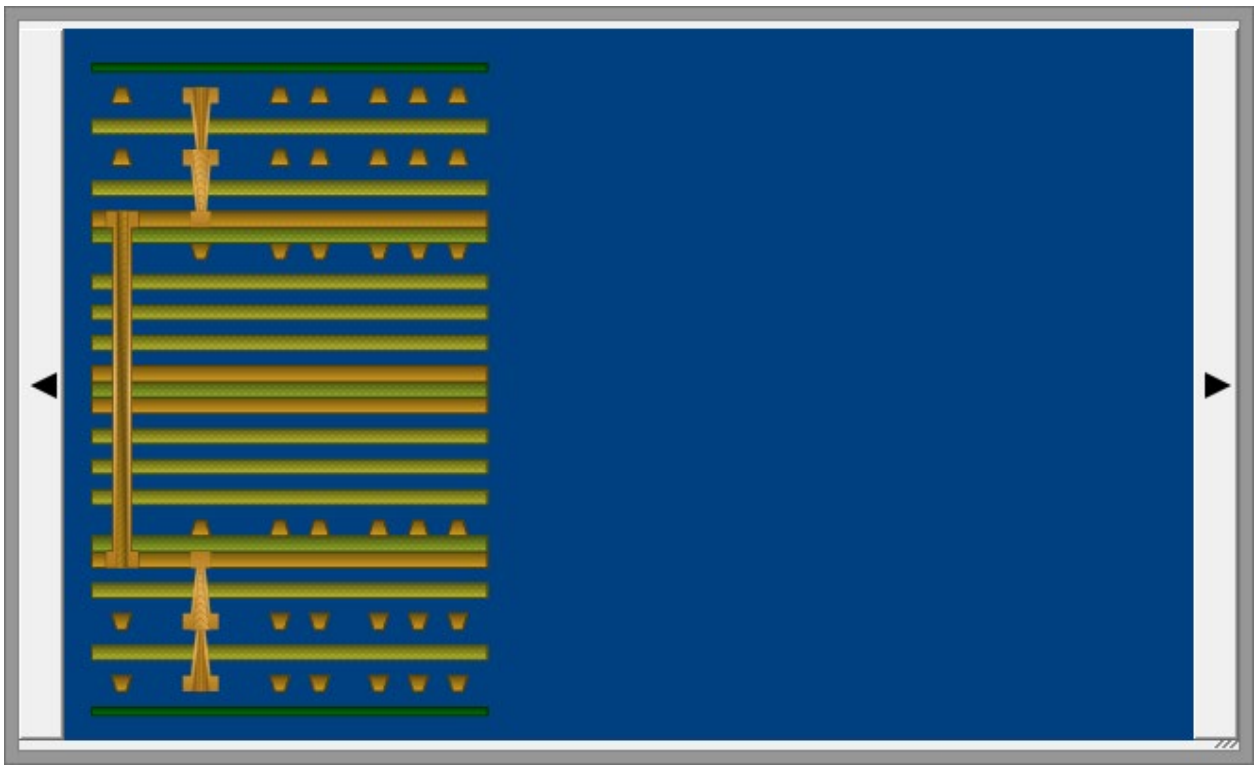
Creating the target stack with the Stack Editor

Consider the target stack below – it will require three press cycles. Build and document the stack in the Stack Editor.

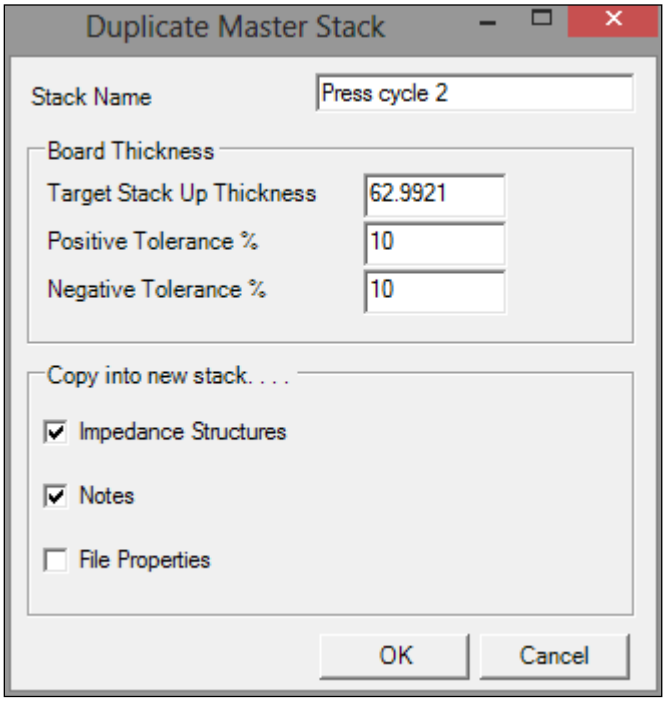
Switch to 2D View.

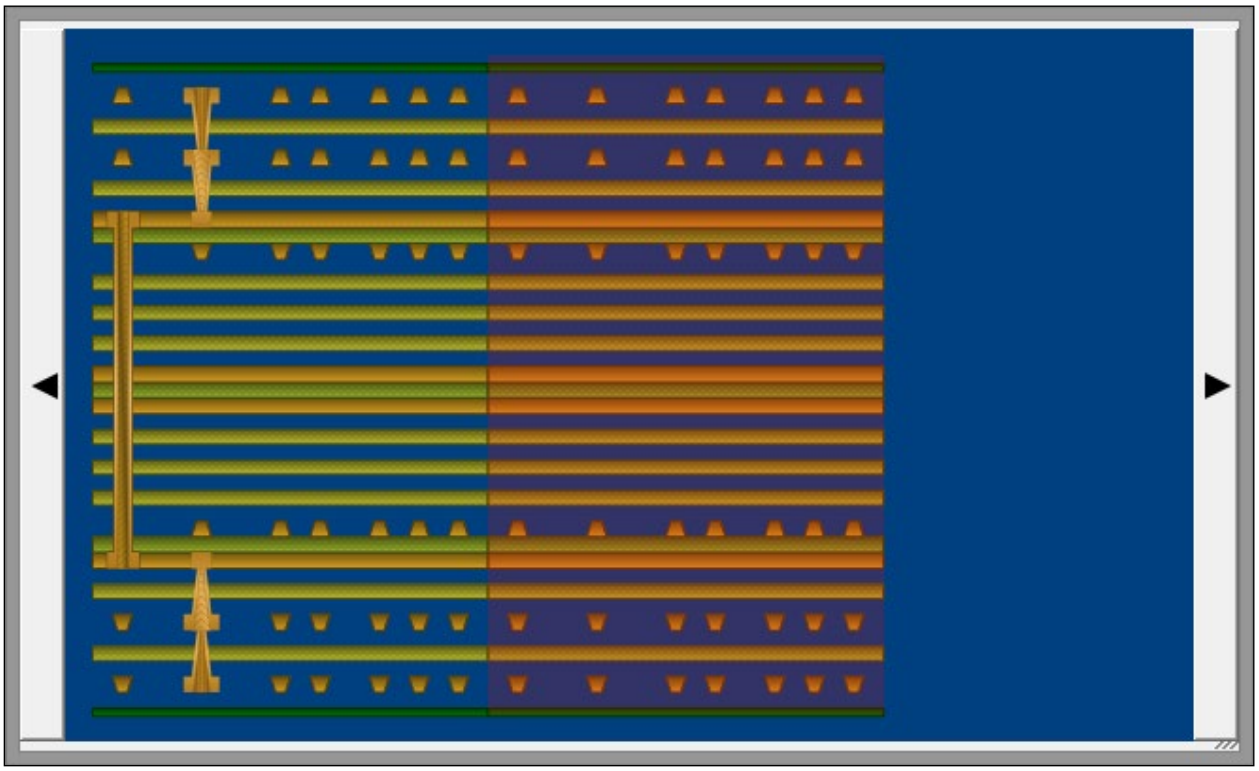


With the target stack completed use the Navigator's Add Stack to document each press cycle, building up the stack in the Navigator. Press F4 to start the Navigator and display the master stack.



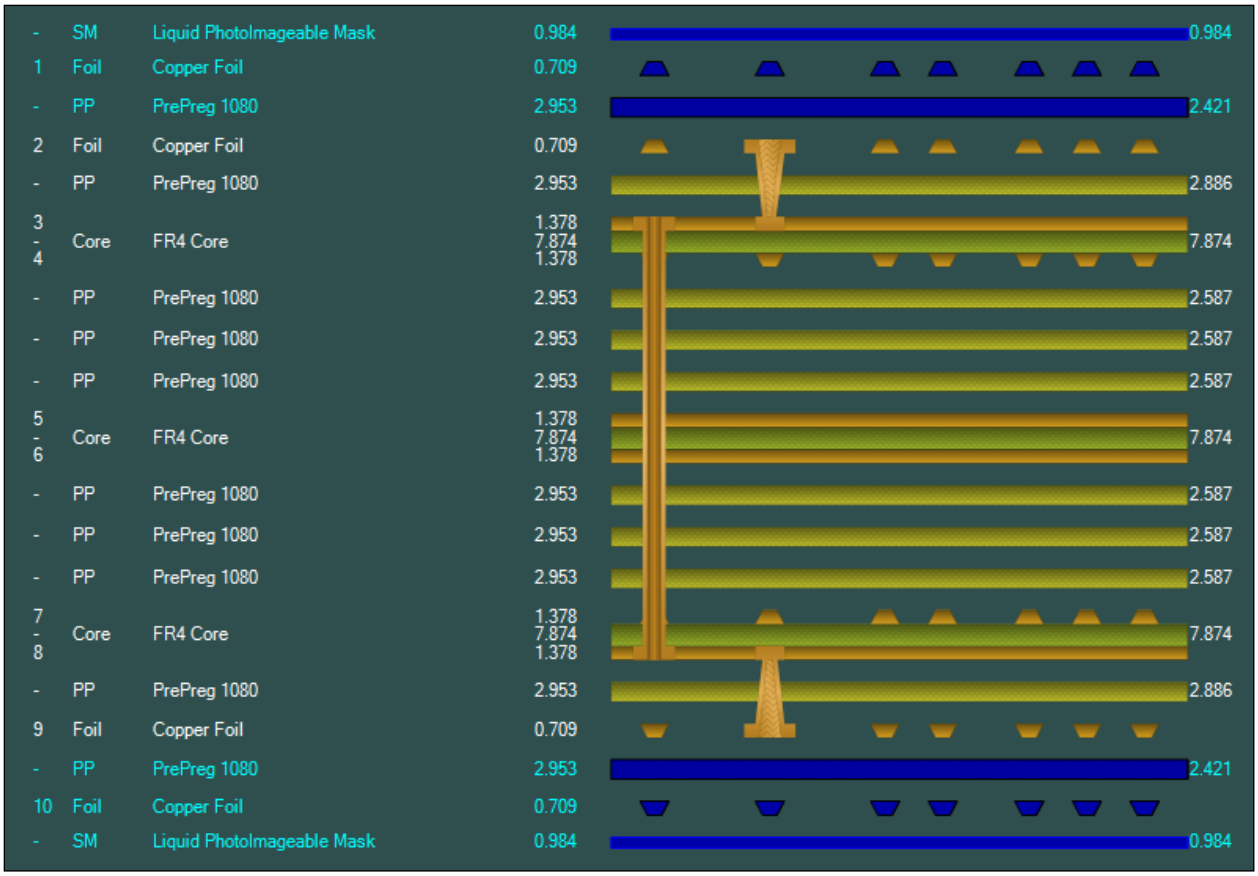
Click Add Stack to copy the stack and name the new sub-stack Press cycle 2.



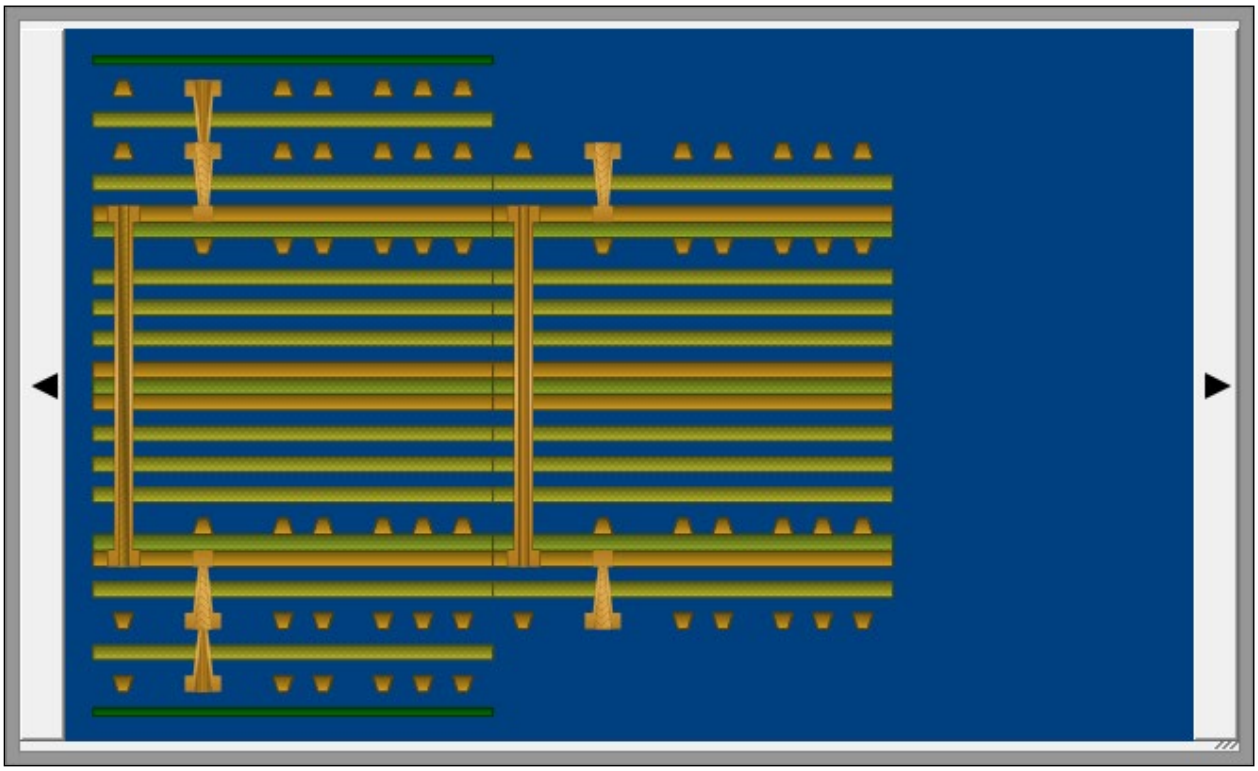


The new sub-stack is copied into the navigator window

Click the sub-stack to display it in the Stack Editor. In the Stack Editor add the drills and disable the materials that are added in the final press cycle.

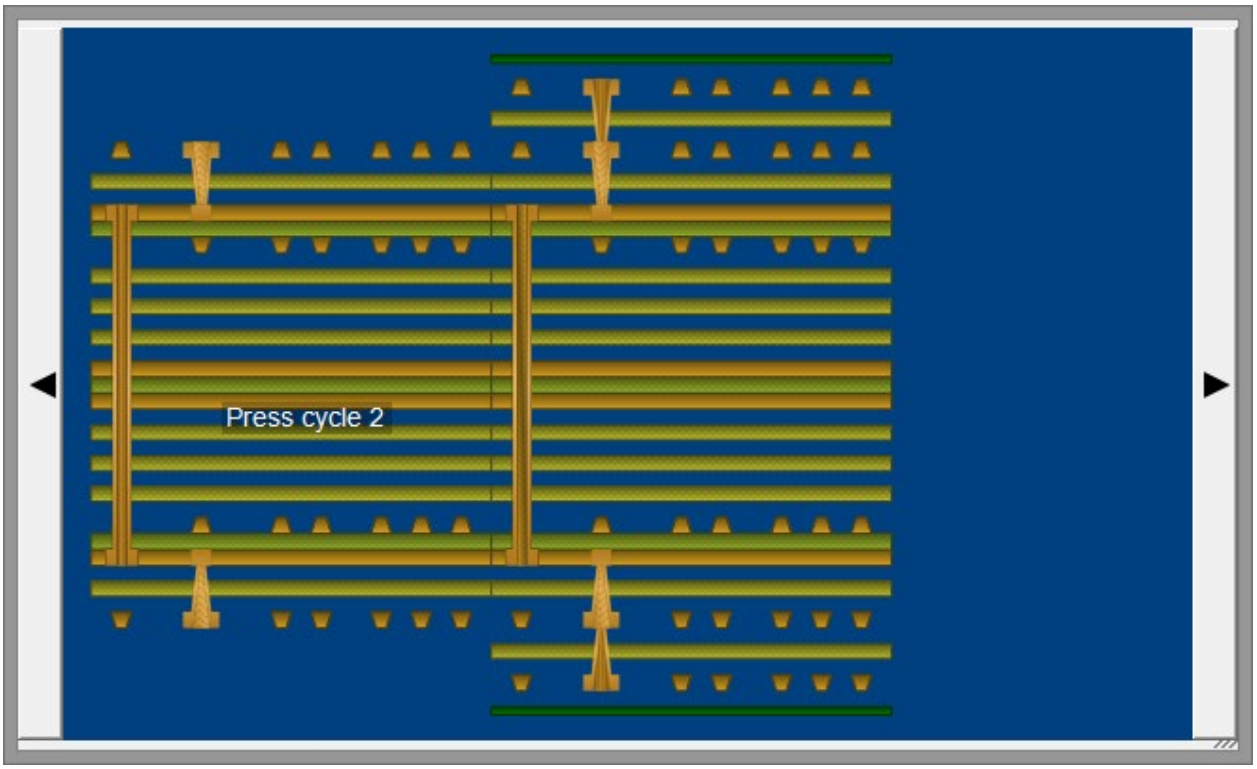


The Navigator displays the second press cycle alongside the master stack.

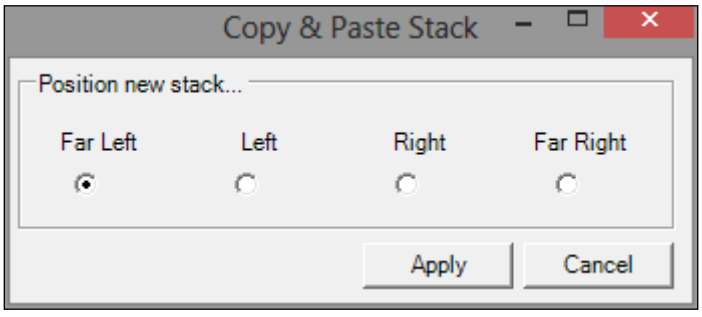


The sub-stack can be displayed either to the right or left of the master stack. Right click the sub-stack and from the context menu choose Move Left.

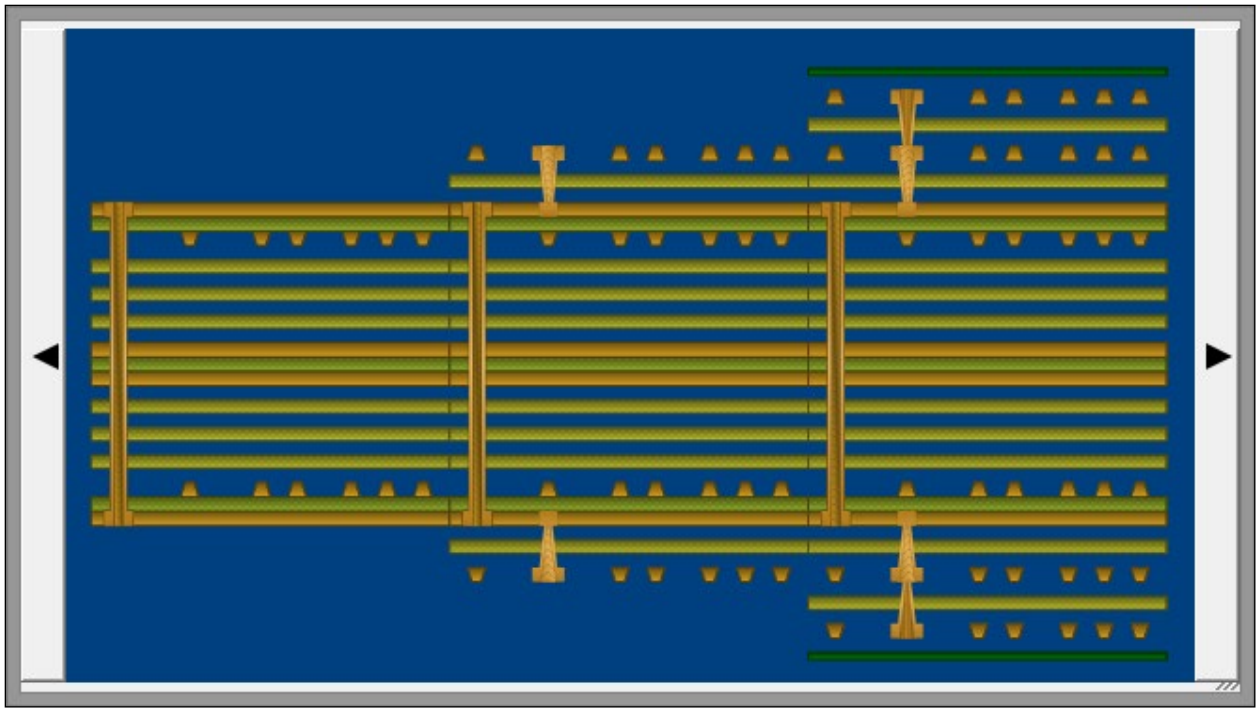
Sub-stack Press cycle 2 is shown to the left of the master.



To add the first press cycle right click the sub-stack and choose Copy and Paste Stack and position the new sub-stack to the far left.



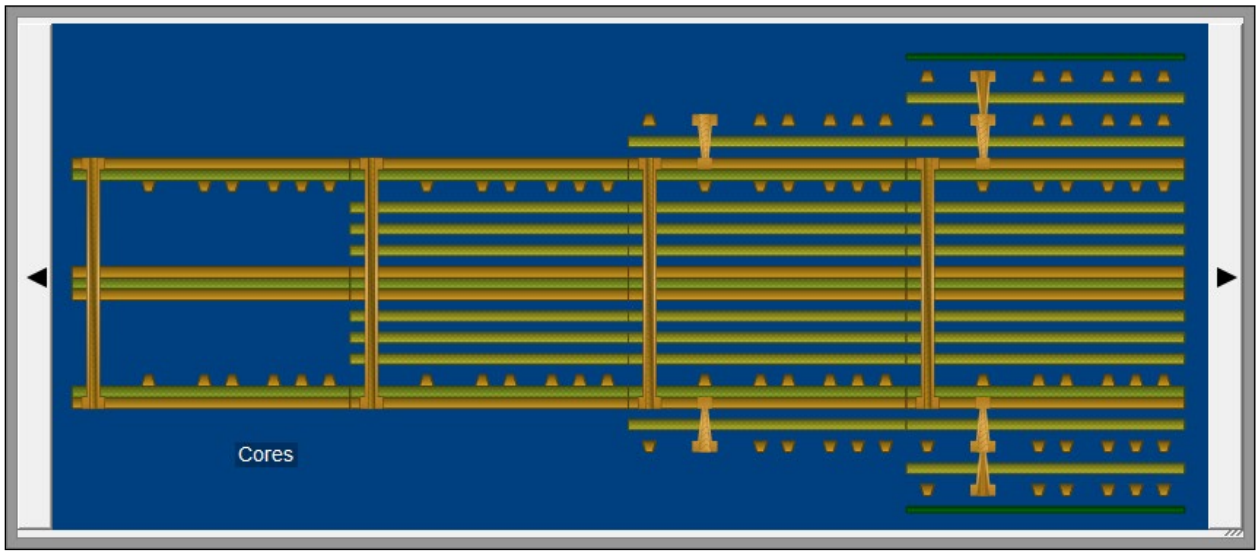
Modify the new sub-stack in the Stack Editor as previously described and display the completed stack in the Navigator.



Each press cycle appears as a separate stack in the Navigator.

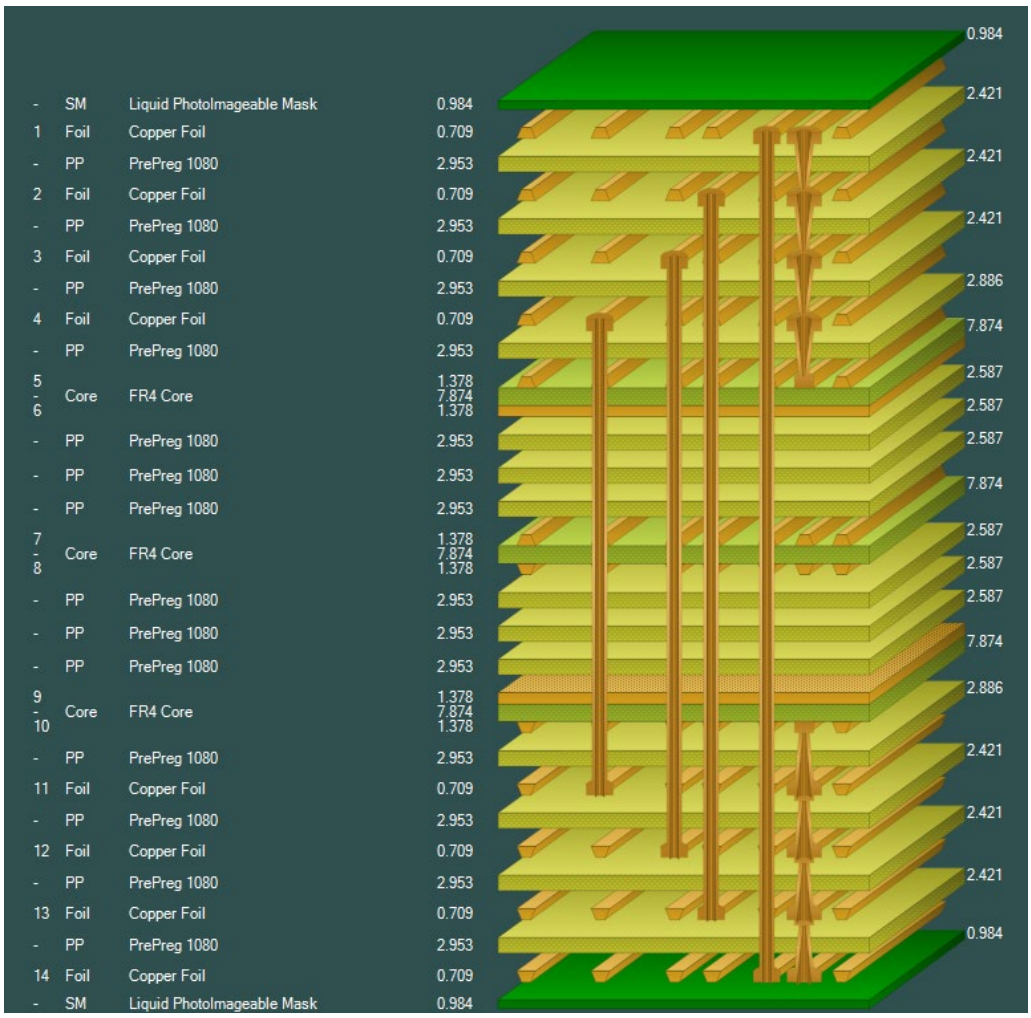
In the fabrication process the manufacturer will process all the core materials first, prior to bonding where each core is interleaved with prepreg materials. It is sometimes useful, therefore, to see all the core materials on a single sub-stack.

Right click the Navigator window and choose HDI Build|Expose Cores to display the core layers.



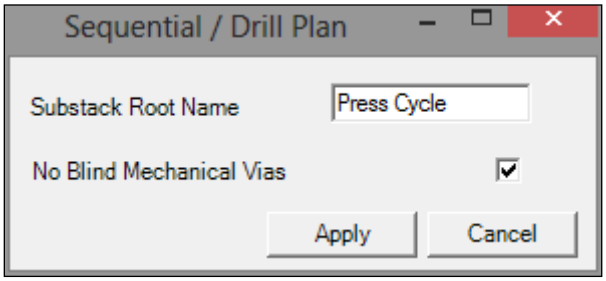
Using the Sequential Plan

Sequential Plan creates sub-stacks that represents each press cycle in a sequential lamination from Master stack based on foil locations. Consider the 14-layer stack below – this stack will need several press cycles to manufacture.

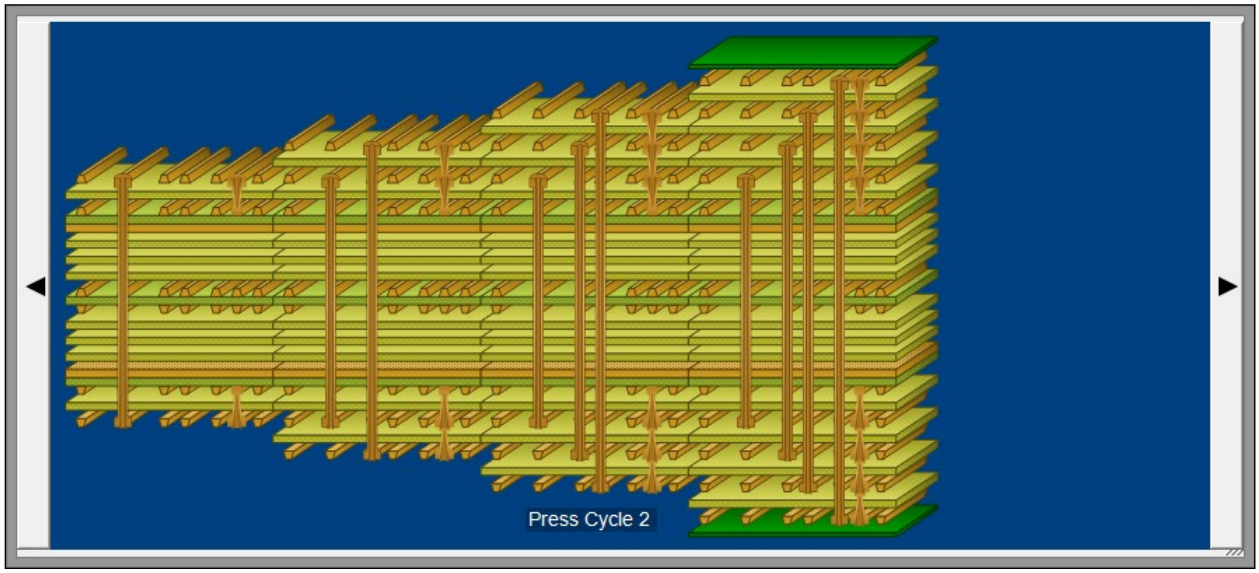


Opening the Navigator will display the completed master stack (shown below) in the Navigator window.

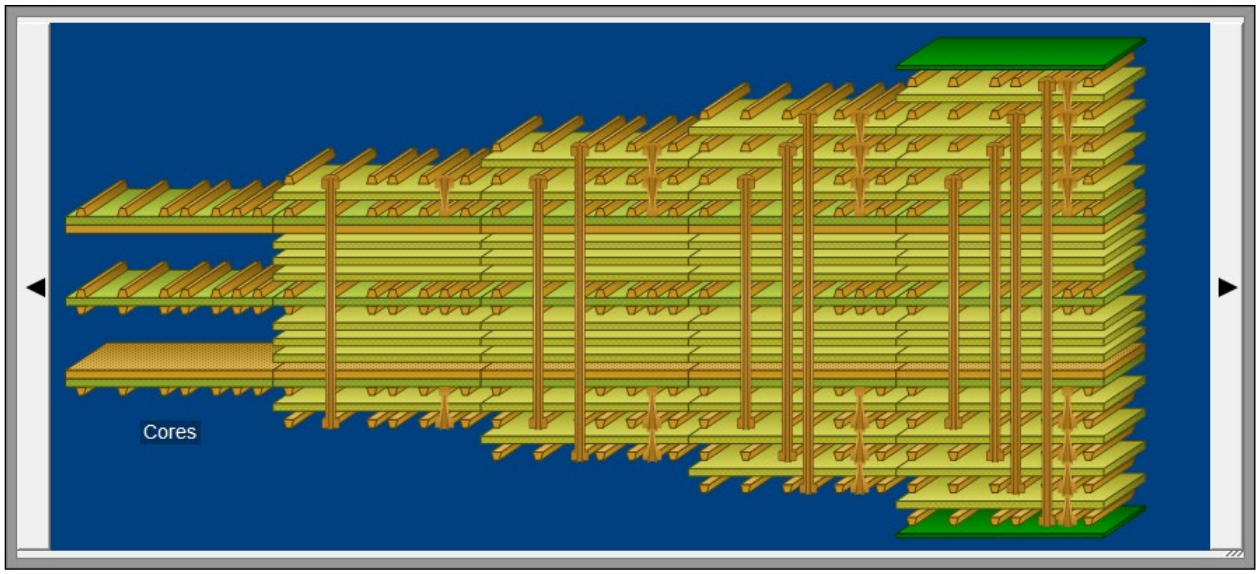
Right click the Navigator window and choose HDI Build |Sequential Plan and name the sub-stacks:



Click Apply – the Navigator displays the 4 press cycles

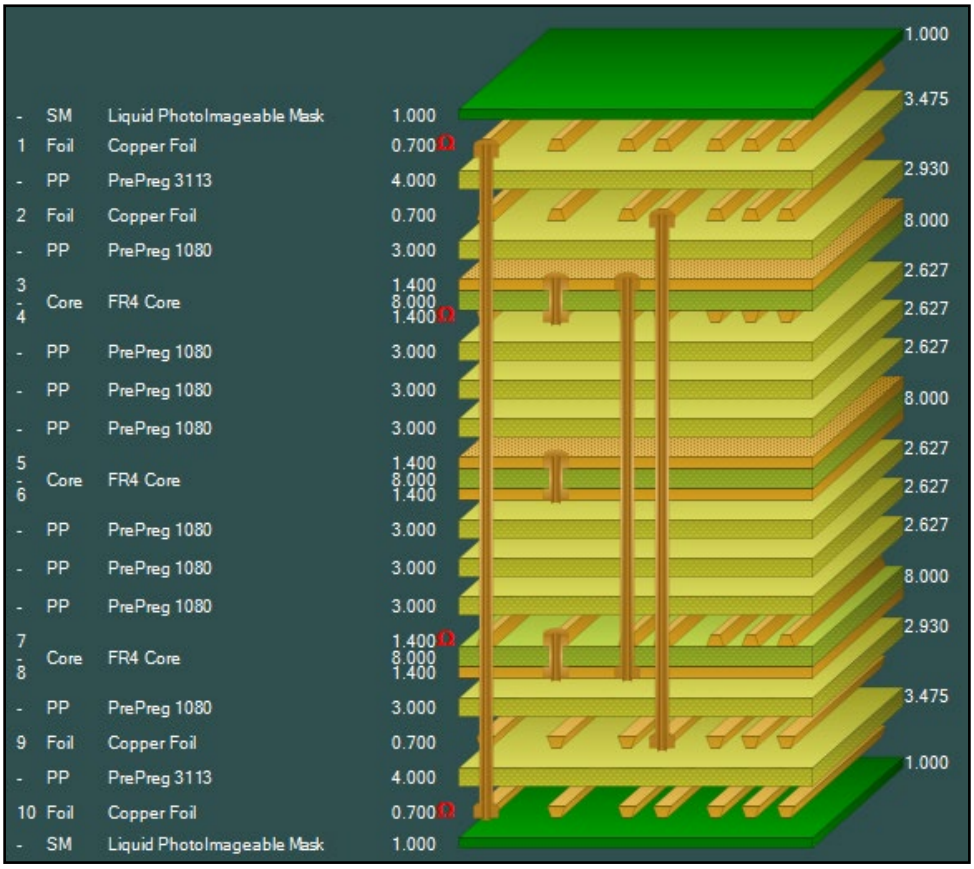


Choose HDI Build|Expose Cores – the cores are displayed in the Navigator window alongside the press cycles.

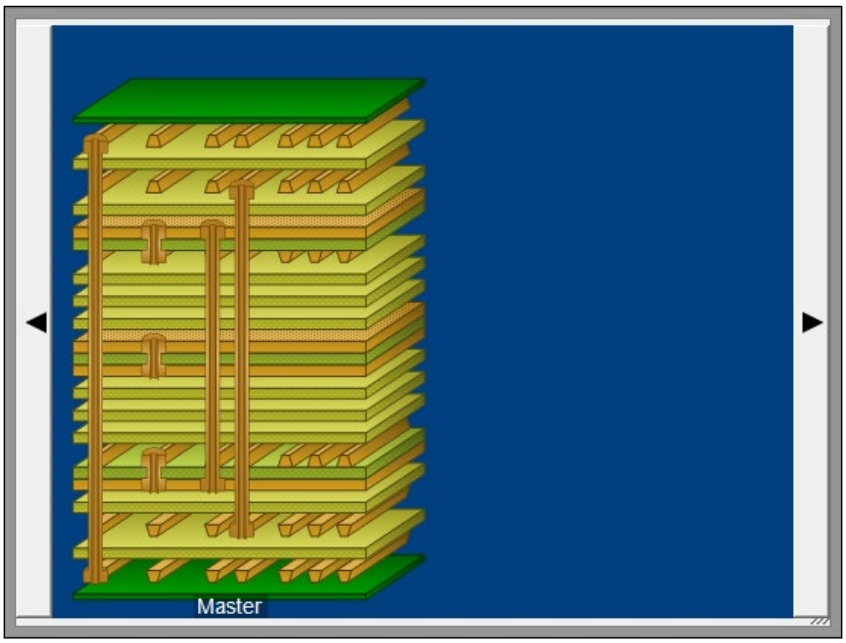


Using the Drill Plan

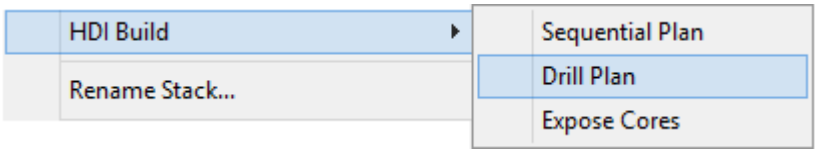
The HDI Build|Drill Plan creates sub-stacks that represents each press cycle from the Master stack based on drill start-end layers. Consider the stackup below – a 10 layer sequential lamination construction.



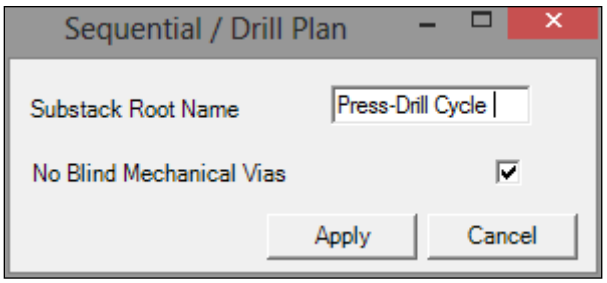
Press the F4 key to open the Navigator



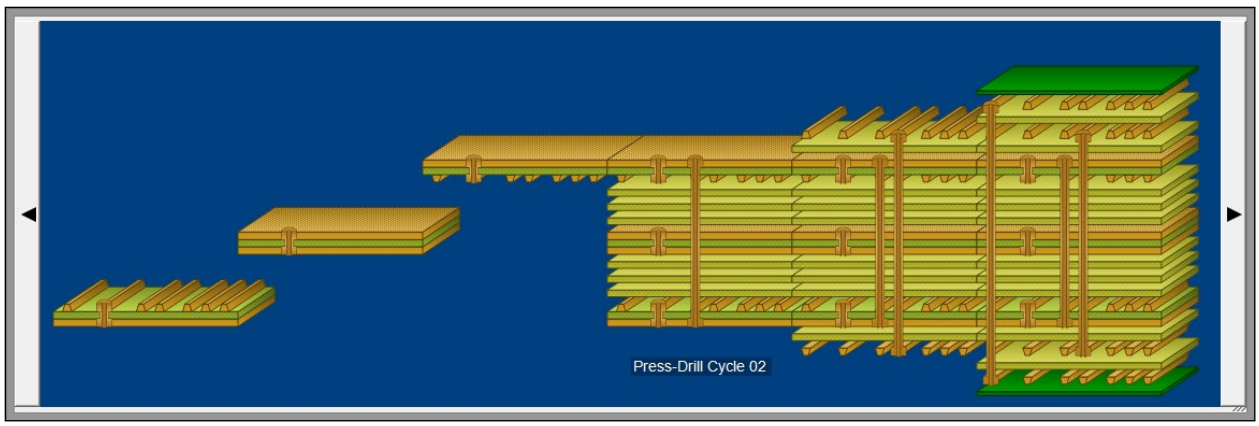
The completed Master stack is displayed. Right click the Navigator and choose HDI Build|Drill Plan.



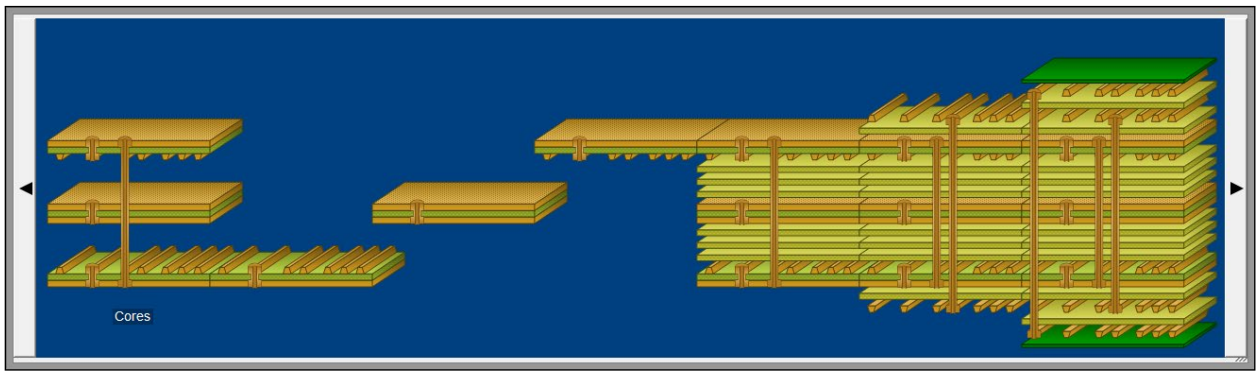
Supply the Sub-stack root name – the name willl be used when numbering the press-drill cycles.



Click Apply – Speedstack documents the build-up stages of the sequential lamination.



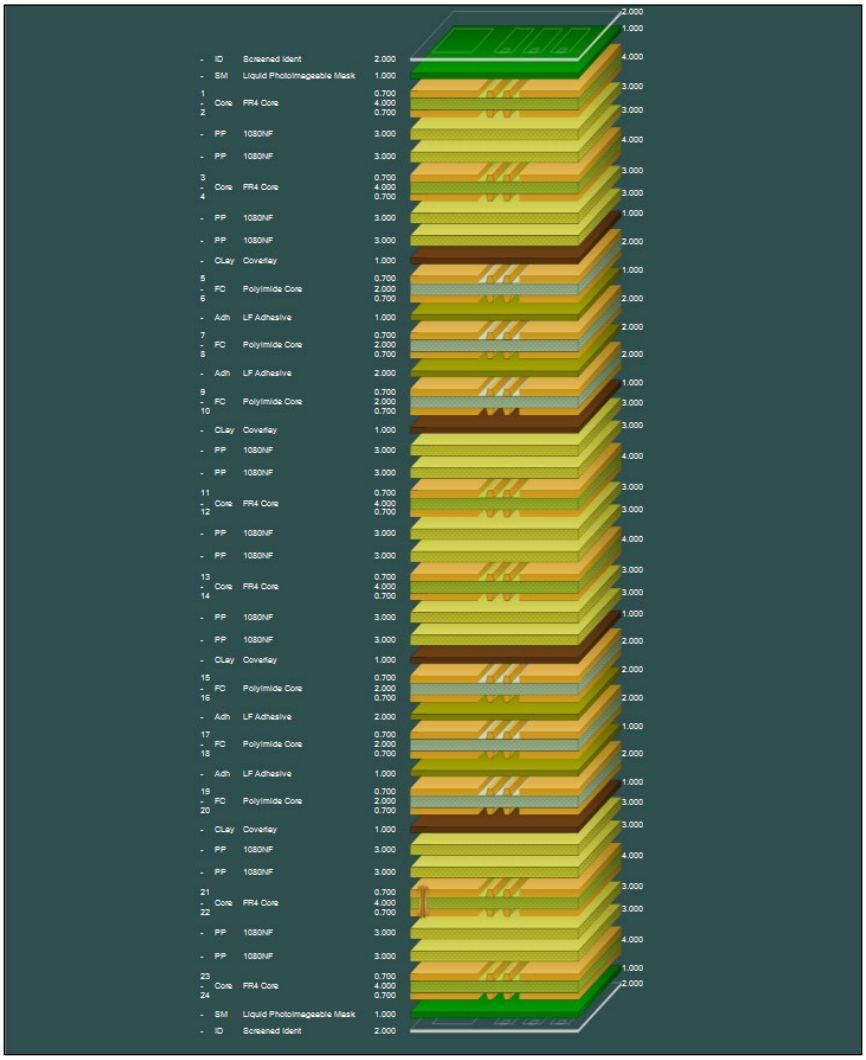
Exposing cores
Right click the Navigator and choose HDI Build|Expose Cores – the cores are shown alongside the press cycles.



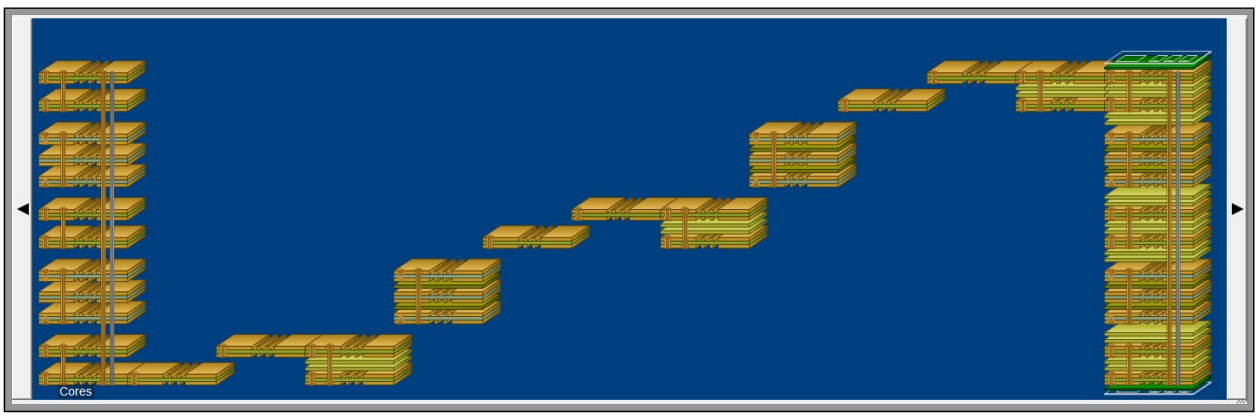
There are no limits to the number of press cycles that may be documented.

Working with multiple press cycles

The stack below is a 24 layer stack with multiple press-drill cycles. Open the Navigator, choose HDI Build|Drill Plan.



The Navigator displays the drill plan and cores below:



Printing the Navigator screen

From the File menu choose Print Technical Report – Speedstack prints the Navigator screen with its press cycles along with individual stack data, impedance data and drill data tables.

Using Speedstack materials libraries

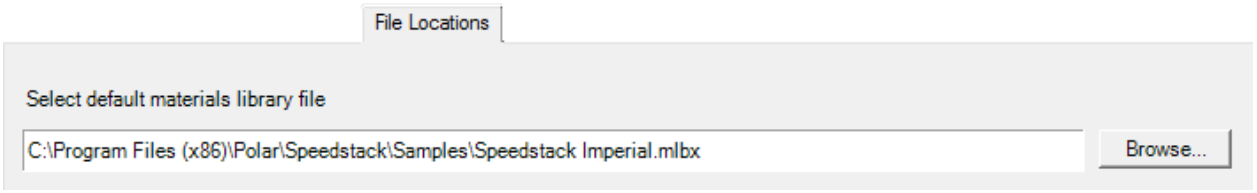
The materials libraries allow designers to manage their own libraries of board materials. Libraries may be created and materials added. Up to date libraries of materials may be downloaded from the Polar Online Material Library.

Materials Library

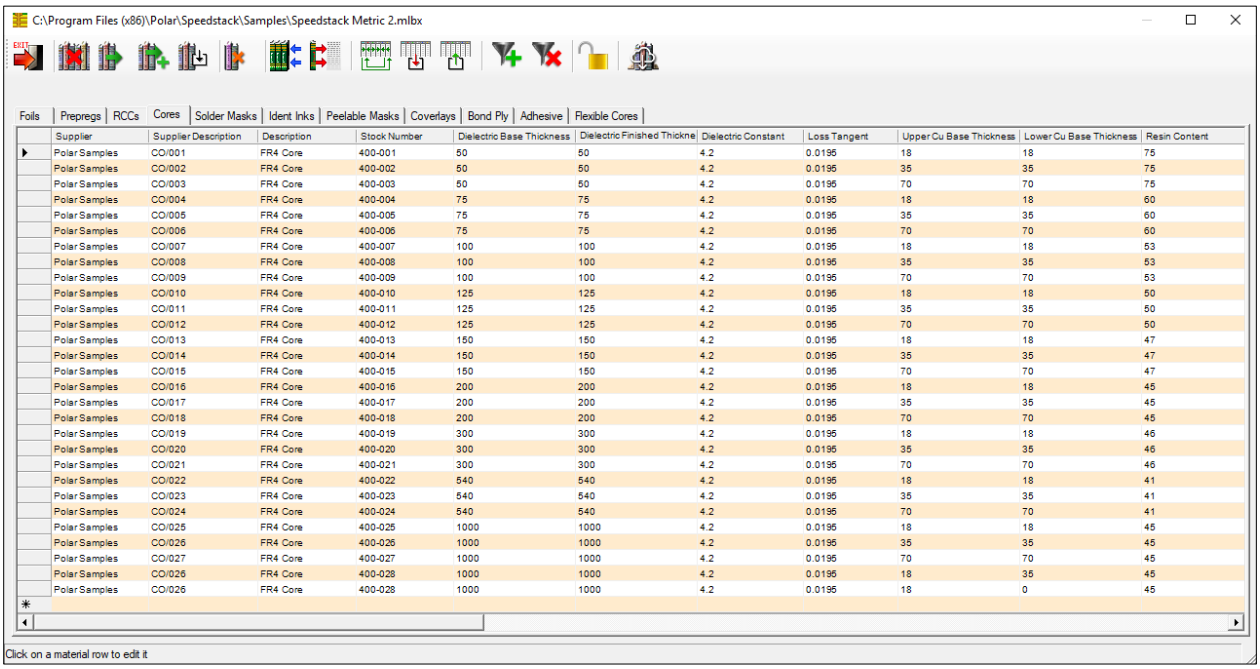
Click the Materials Library button to display the Materials Library window.

Working with the materials libraries

When Speedstack is started the materials library specified as the default materials library file (via Tools|Options|File Locations) is opened.



Each library component type is accessible via its associated tab. Click on the tab to view or edit the component type.



Materials library toolbar

Use the toolbar to load and save libraries, import or export libraries, arrange data columns and filter by data field or access the online or on-premise libraries. The Toolbar and button functions are shown below.

 Exit library

 Clear materials library

 Open materials library

 Open and Append

 Save materials library

 Clear current data table

 Import CSV library

 Export CSV library

 Select & arrange column fields

 Save column order

 Load column order

 Set filter

 Clear filter

 Library lock

 Online / on-premise library

Opening a library

Open Materials Library

To open, or load, a library click the Open Library icon and browse to the library; click Open – the currently loaded library will be replaced.

Opening and appending a library

Open and Append Library

To open a library and add the materials to an existing library click the Open and Append Library icon, browse to the library and click Open: the material will be added to the existing library table.

Creating a new library

Clear Materials Library

To create a new library, click Clear Materials Library; the library is removed from the library manager. Import materials as described below and save the library.

Save Materials Library

Click Save Materials Library and supply a name and destination folder to create the new library. To have the library load as Speedstack starts, specify it as the default materials library file via Tools|Configuration Options|File Locations

Importing material to the Speedstack materials library

Speedstack allows users to add existing material lists (usually supplied from the material manufacturer data sheets) to its library; material data must be arranged in the format and order used by the Speedstack library.

Library materials can be imported from the Polar Online / On-Premise Library or from local library files.

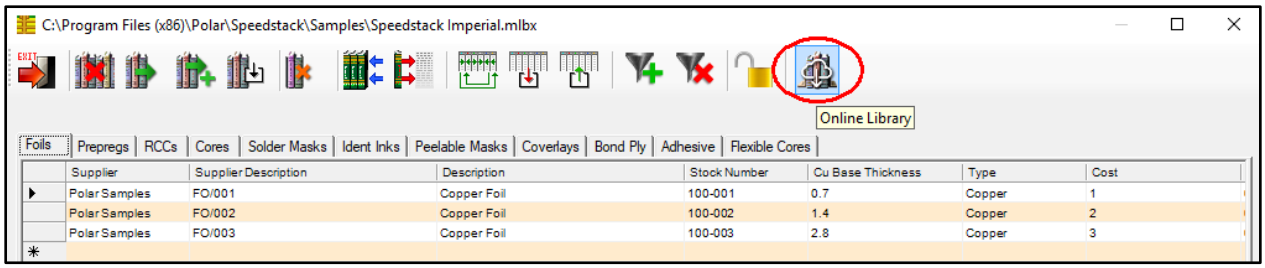
Using the Online Library

The Online Library comprises the most up to date copies of the material files supplied from materials manufacturers who are members of the Polar Speedstack Supplier Partner program. Each new version of Speedstack adds new materials to the Polar online library; utilisation of the online library requires access to the internet.

The On-Premise copy of the online library is available on request for Polarcare subscribers who may have restricted access to the internet (for example, as a result of IT security policies.). Contact polarcare@polarinstruments.com with your Polarcare Contract number and Speedstack version.

Importing from the Polar Online Library

Choose the material table tab (Foils, Prepregs, etc.) and click the Online Library icon.

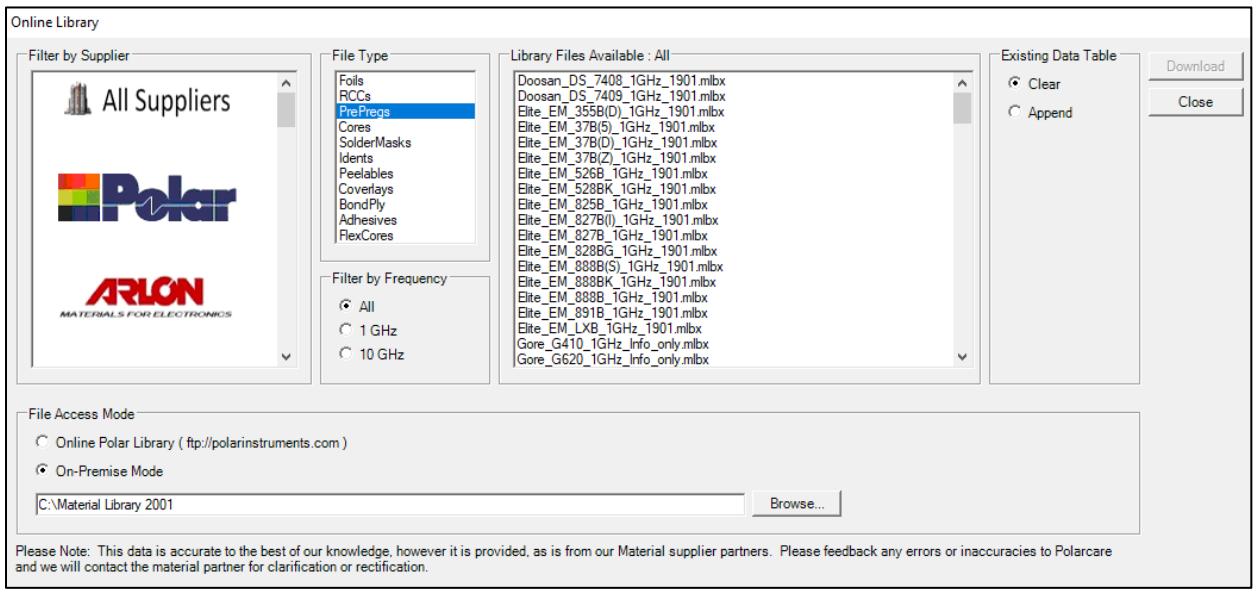


Speedstack connects to the Online Library and displays the materials available for each file type from all the suppliers in the Speedstack Supplier Partner program; click on a material supplier's name in the Filter by Supplier pane to view just the materials available from that supplier.

Filtering libraries by frequency

Material libraries contain values for dielectric constant (Dk) and loss tangent (Df) measured at frequencies specified by the supplier. The measurement frequency is indicated in the library file name.

Use the Filter by Frequency function to list all files or just the files with Dk and Df specified at 1GHz or 10GHz.



On-Premise libraries

Where access to the online library is unavailable or a local copy is required, a complete set of the online libraries is available on request to Polarcare subscribers; contact polarcare@polarinstruments.com with your Polarcare contract number and Speedstack version. The supplied libraries should be copied to a suitable local folder with the file/folder structure preserved. Choose On-Premise Mode and browse to the local copy: the library files should appear as a local online library; import materials as described above.

Downloadable mlbx files
Note that the Online Library only lists files with .mlbx extensions and that follow the file naming conversion:

<Supplier>_<MaterialFamily>_<freq>_<release>. mlbx

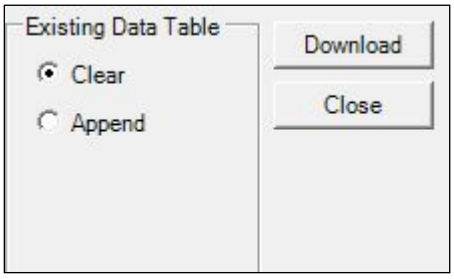
(No spaces are permitted in downloadable library file names.)

All .mlbx file names reflect the frequency at which dielectric constant and loss tangent is specified and the Speedstack release version.

Although the .mlbx file format will support multiple material types (Foils, Prepregs, Cores, etc.) in the same file *the downloadable .mlbx file only contains a single material type*.

Choosing material files
Browse through the list of available materials or scroll through the list of suppliers and choose a supplier to filter the materials by that supplier.

Choose the File Type and material. From the Existing Data Table dialog select Clear to replace the contents of the selected table type or Append to add the new materials to the table.

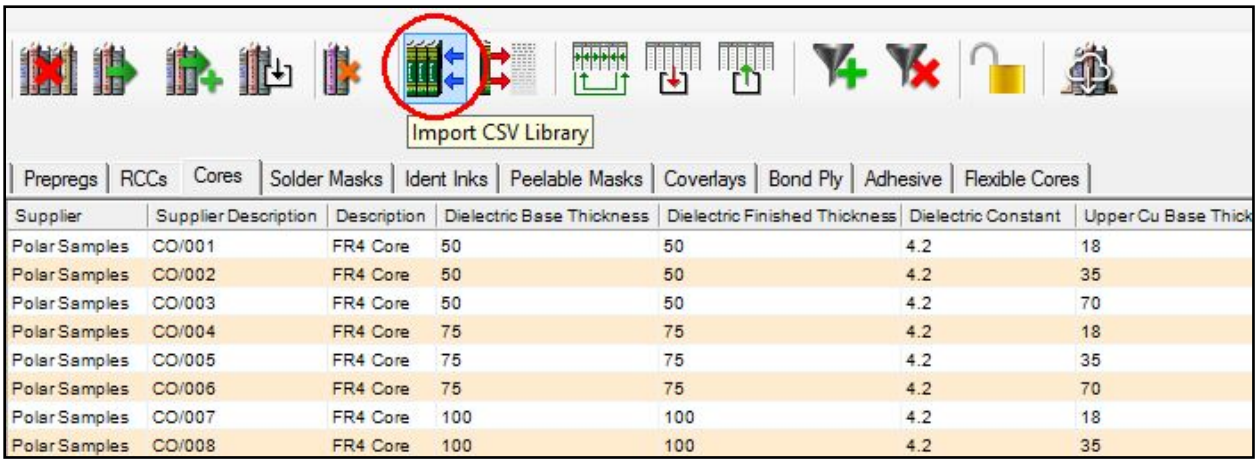


Click Download; repeat for each material to be added to the library then click Close.

Note: Many organisations connect to the Internet via proxy servers to provide caching and controlled access. In some cases, a proxy server may return library content in a format that prevents successful download into Speedstack. If your organisation connects to the internet via a proxy server, you may need to request the MIS department to grant address ftp://polarinstruments.com permission to bypass the proxy server – if this is not possible the libraries can be supplied for local (on-premise) access (see above.)

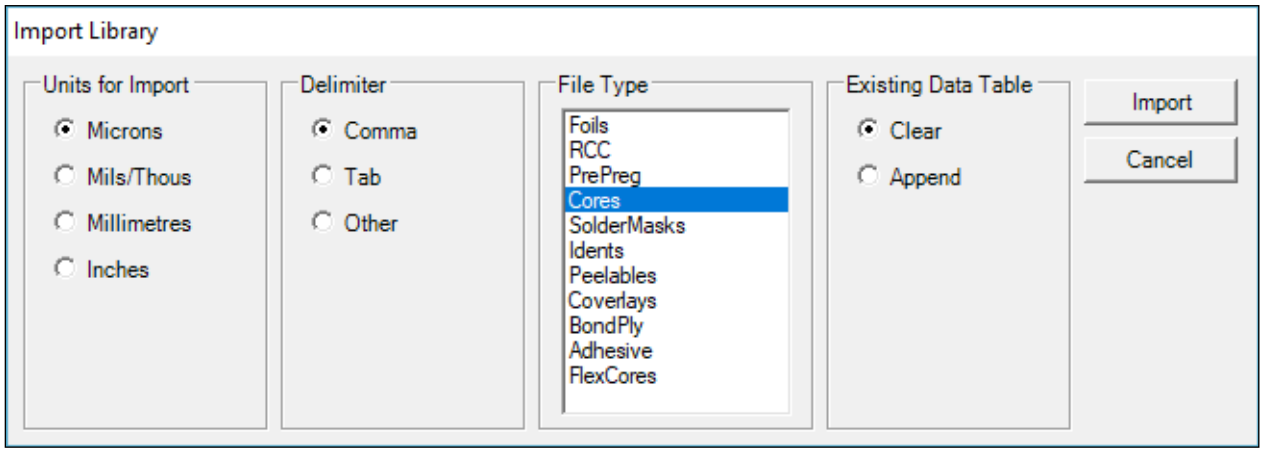
Importing from local material files
Prior to importing the material data file ensure the file is not open in another process (e.g. Microsoft® Excel®.)

Click the Speedstack Materials Library button to open the Library, and then click Import CSV Library to open the Import dialog.



Supplier	Supplier Description	Description	Dielectric Base Thickness	Dielectric Finished Thickness	Dielectric Constant	Upper Cu Base Thick
Polar Samples	CO/001	FR4 Core	50	50	4.2	18
Polar Samples	CO/002	FR4 Core	50	50	4.2	35
Polar Samples	CO/003	FR4 Core	50	50	4.2	70
Polar Samples	CO/004	FR4 Core	75	75	4.2	18
Polar Samples	CO/005	FR4 Core	75	75	4.2	35
Polar Samples	CO/006	FR4 Core	75	75	4.2	70
Polar Samples	CO/007	FR4 Core	100	100	4.2	18
Polar Samples	CO/008	FR4 Core	100	100	4.2	35

When importing materials set the Import options in the Import Library dialog: specify the units, delimiter and material type and specify whether the material will be used to clear the current data table or append to the existing library.



Replacing existing material tables

Choose the Clear Existing Data Table option and choose the field delimiter type. The library import function can accept files in a variety of formats, tab delimited, comma separated and Excel worksheet and template formats but must be in the format of the supplied sample files with columns in the correct order.

Specify the units for import, file delimiter and choose the file type (Foil, RCC, Prepreg, etc.) and click Import. Navigate to the file via the Open dialog and click Open.

Repeat the procedure for every file type to be imported. Save the file as a .mlbx library file.

Adding material data to an existing library

To add material data to an existing library table, open the library, click Import CSV Library, click the Append to Existing Data Table and click Import.

Navigate to the .csv or .txt file and click Open. Save the modified library file as a .mlbx file.

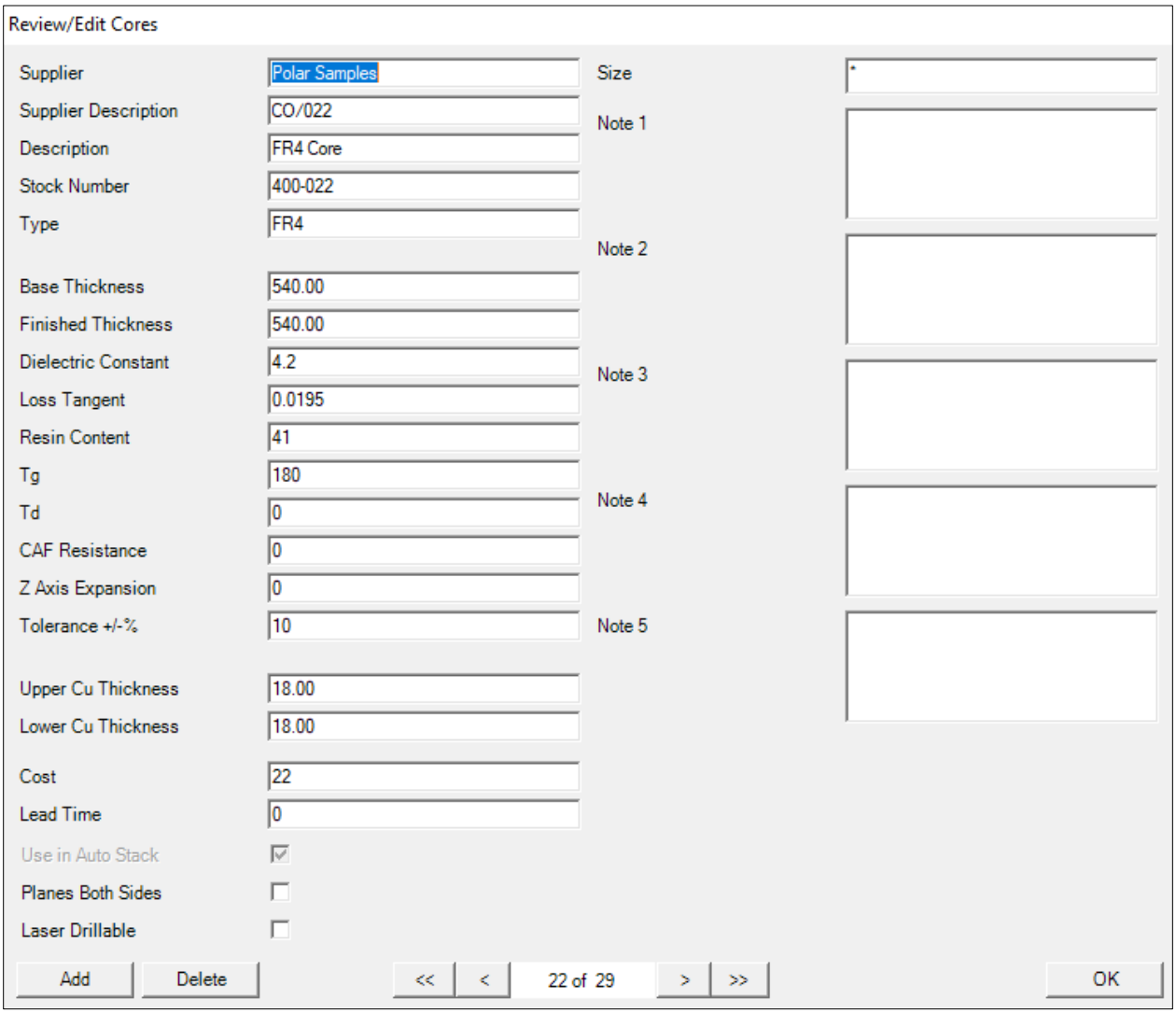
Exit the library when all file types have been imported.

Adding new material to the data tables

Caution: ensure consistency of units

When defining dimensions, e.g. layer thicknesses, for a stackup ensure that all measurements are defined using the same units (mils, mm, etc.) throughout the structure and its associated libraries.

Open the library to be modified. To add individual materials to a library click the associated component type tab; click onto a material, or empty line. An editing box will open which will contain the material clicked on, or the last material in that type library.



The material can be edited or deleted, or a new material can be added. To speed up the process of adding families of materials, when a material is added the properties of the last

material are copied to the new material. The details can then be edited. Clicking OK will add any new materials to the end of the list.

Importing material to the data tables

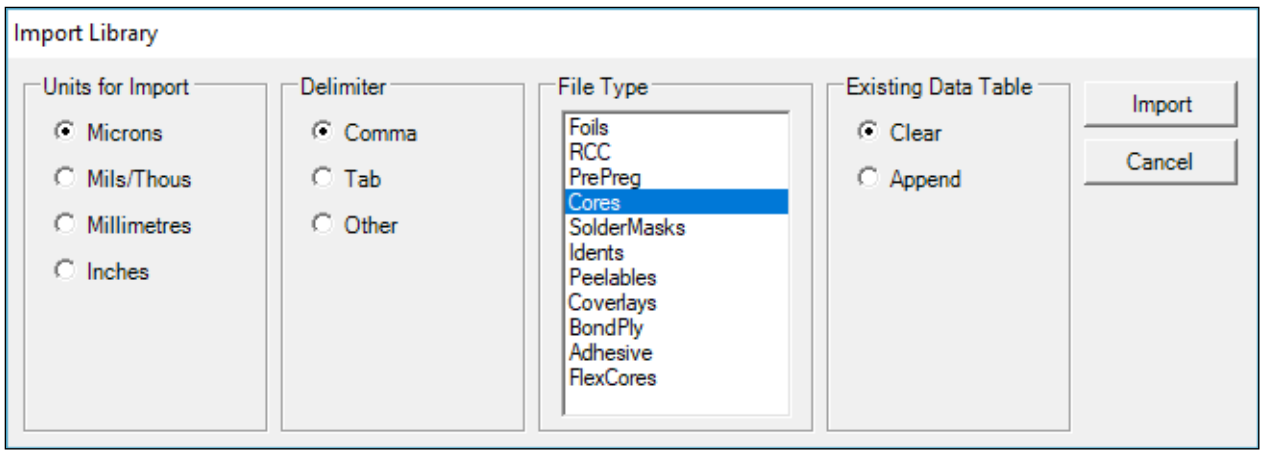
Speedstack allows users to add existing material lists to its library; material data must be arranged in the format and order used by the Speedstack library.

Library sample files

Sample files for all material types in comma separated value format and Microsoft Excel spreadsheet and template formats suitable for importing to the Speedstack are available on request from Polar Instruments.

Import CSV Library

Click the Materials Library button to open the Library, and then click Import CSV Library to open the Import dialog.

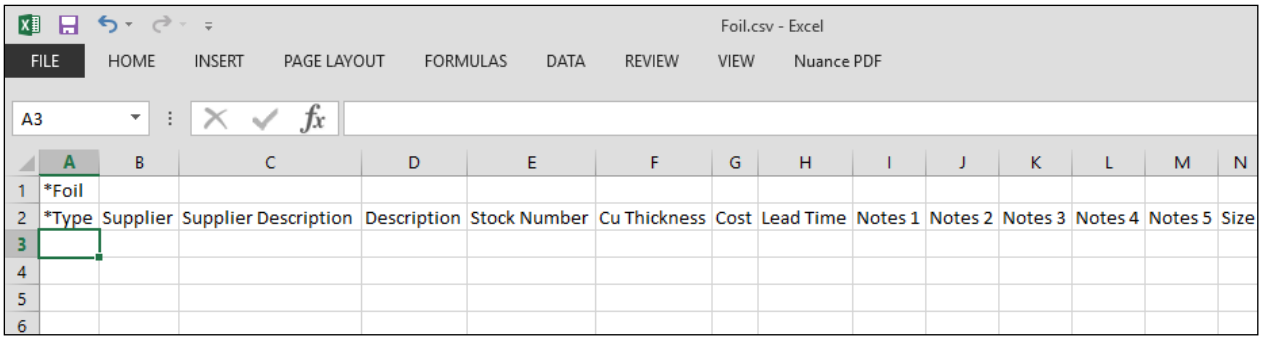


Choose Clear or Append to Existing Data Table as appropriate.

Creating a new materials library table

Choose Clear Existing Data Table, click Export Library as CSV and choose microns as units and the field delimiter type and click Export. The data table is exported as a “template”.

Open the file in a suitable text file editor – the file below is opened in Microsoft Excel and shows the file header rows with the column headers in the order and format expected by the Speedstack library manager. Add the material data to the associated columns and save in text format. As noted above, templates for all materials are available on request from Polar Instruments.



	A	B	C	D	E	F	G	H	I	J	K	L	M	N
1	*Foil													
2	*Type	Supplier	Supplier Description	Description	Stock Number	Cu Thickness	Cost	Lead Time	Notes 1	Notes 2	Notes 3	Notes 4	Notes 5	Size
3														
4														
5														
6														

Empty Foils library table

The library import function can accept files in a variety of formats, tab delimited, comma separated and Excel worksheet and template formats.

Sections of the sample files suitable for Speedstack are shown below.

	A	B	C	D	E	F	G	H	I
1	* Cores								
2	*							Dielectric	Dielectric
3	*Type	Supplier	Supplier Description	Description	Stock Number	Upper Cu Thickness	Lower Cu Thickness	Base Thickness	Finished Thickness
4	FR4	Polar Samples	CO/001	FR4 Core	400-001	0.018	0.018	0.05	0.05
5	FR4	Polar Samples	CO/002	FR4 Core	400-002	0.035	0.035	0.05	0.05
6	FR4	Polar Samples	CO/003	FR4 Core	400-003	0.07	0.07	0.05	0.05
7	FR4	Polar Samples	CO/004	FR4 Core	400-004	0.018	0.018	0.075	0.075
8	FR4	Polar Samples	CO/005	FR4 Core	400-005	0.035	0.035	0.075	0.075
9	FR4	Polar Samples	CO/006	FR4 Core	400-006	0.07	0.07	0.075	0.075
10	FR4	Polar Samples	CO/007	FR4 Core	400-007	0.018	0.018	0.1	0.1
11	FR4	Polar Samples	CO/008	FR4 Core	400-008	0.035	0.035	0.1	0.1

Sample Cores library file in Microsoft Excel format

```
* Cores,,,,,,,,,,,,,,,,,,,,,,,,
*,,,,,,,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,,,,,,,
*Type,Supplier,Supplier Description,Description,Stock Number,Upper Cu Thickness,Lower Cu Thickness,Base Thickness,Finished Thickness,
Content,Tg,Td,CAF Resistance,ZAxisExpansion,ExcessResin,Tolerance,Cost,Lead Time,Notes 1,Notes 2,Notes 3,Notes 4,Notes 5,Size
FR4,Polar Samples,CO/001,FR4 Core,400-001,0.018,0.018,0.05,0.05,4.2,75,180,0,0,0,0,10,0,0,,,,,,*
FR4,Polar Samples,CO/002,FR4 Core,400-002,0.035,0.035,0.05,0.05,4.2,75,180,0,0,0,0,10,0,0,,,,,,*
FR4,Polar Samples,CO/003,FR4 Core,400-003,0.07,0.07,0.05,0.05,4.2,75,180,0,0,0,0,10,0,0,,,,,,*
FR4,Polar Samples,CO/004,FR4 Core,400-004,0.018,0.018,0.075,0.075,4.2,60,180,0,0,0,0,10,0,0,,,,,,*
```

Sample library file in comma separated format

Files for importing into the library must be in the above format, *with columns in the correct order*.

Specify the delimiter if necessary and choose the file type (Foil, RCC, Prepreg, etc.) and units for import and click Import and Clear or Append as required.

Choose the file from the list displayed in the Open dialog and click Open. Repeat the procedure for every file type. Save the file as a .mlbx library file.

Exit the library manager when all file types have been imported.

Adding material data to an existing library

To add material data to an existing library, open the library click Import CSV Library, click the Append to Existing Data Table and click Import.

Choose the .csv or .txt file and click Open. Save the modified Library file as a .mlbx file.

Selecting Materials from the Library

Column Order (Materials Library)

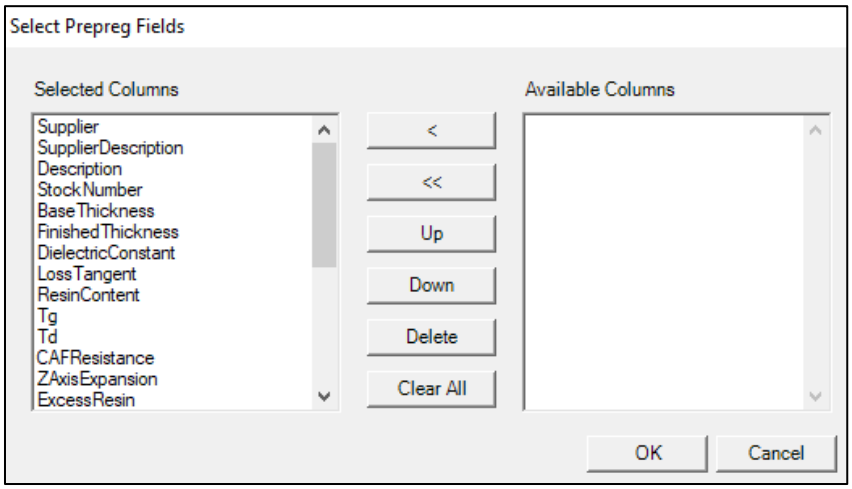
The default setting displays all columns. The columns displayed and the order they are displayed can be set in the materials Library form.

Arranging Columns in Library Forms

The Library windows can be customised in respect of which columns to display and in which order.

Arrange Columns

Click the Go to Materials Library button and select Arrange Columns; the dialog associated with the selected material tab (Foils, Prepregs, etc.) is opened.



The Left box of the dialog shows the columns that will be displayed and the order top to bottom is the order they will be displayed left to right in the library window.

Click OK to return to the Materials Library, which will show the columns as set.

Save Column Order

Until the column order is saved the column order is only available during the current session. Click Save Column Order to define the selected column order as the default order whenever the program is run.

Load Column Order

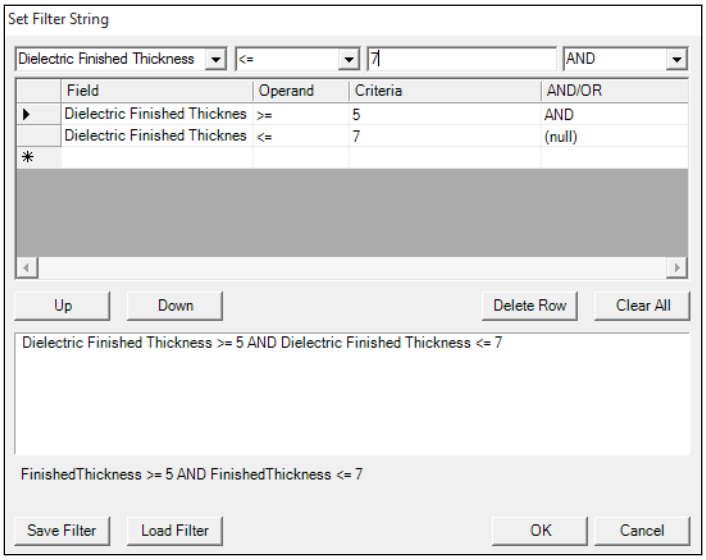
Click Load column Order to apply a saved column arrangement.

Filtering Materials

When adding or swapping materials, available materials (Foils, Prepregs, etc.) are listed in the associated material library dialog. Lists can be filtered for materials matching desired parameters (dielectric thickness, Er, etc.)


.Set Filter

In the library window click the Set Filter to display the Set Filter String dialog.



Filter strings can be created and saved for future use. To save click Save Filter, to recall an existing filter click the Load Filter button, choose the filter (.mlf) file and click OK.

Building the filter string

Build the filter string by selecting parameters, operands and criteria from the drop-down boxes. If the AND/OR box is selected another row is automatically added to the grid. The filter language is a sub-set of common database commands.

Use the Up/Down buttons to select a row for deletion. The arrowhead at the side of the grid indicates the selected row.

Click OK to apply the filter immediately to the selected library. If desired, save the filter string for future use. (The Speedstack provides for interaction between the library dialog and filter form. This allows complex strings to be built line-by-line and tested without saving until the string is completed.)

When saving the filter choose a descriptive name for the file that reflects the purpose of the filter. The Speedstack automatically names the files for the material type.

Using the Like operator

Use the Like operand to filter results via wild card characters. The characters * and % can be used to represent groups of starting or ending characters.

For example, specifying Like ‘Po%’ or ‘Po*’ as the criterion for the Suppliers field will show all suppliers beginning with ‘Po’.

Similarly, specifying Like ‘%es’ or ‘*es’ as the criterion for the Suppliers field will show all suppliers ending with ‘es’.


Clear Filter

Click the Clear Filter to remove the filter and display all materials of the selected type.

Locking the library

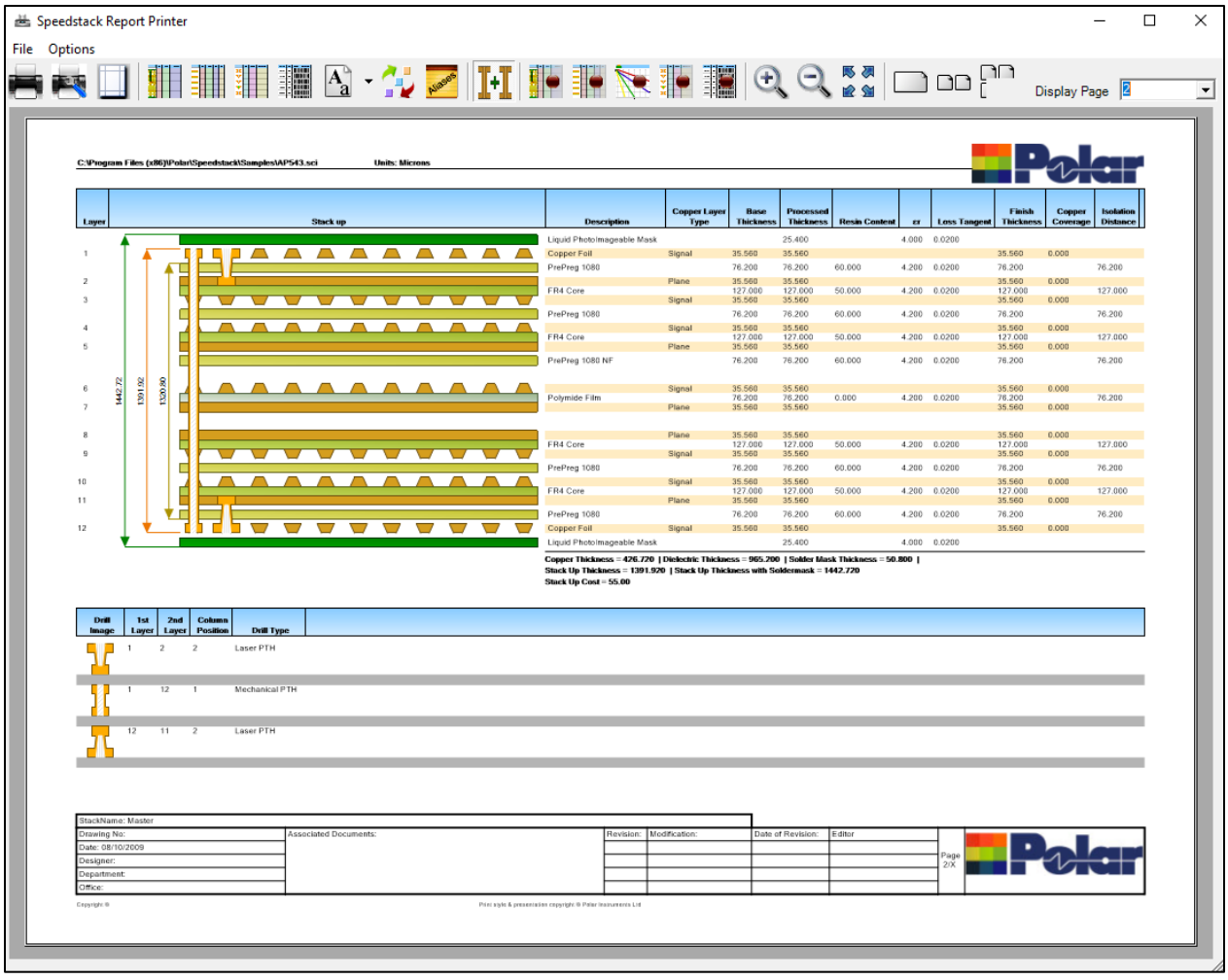

Library Lock

The materials library can be locked and password protected to prevent unauthorised or accidental editing. If no password has been set the Material Library remains open for any changes and modifications.

To lock the library, click the Library Lock button and supply a password; the library is then locked and any editing requires the password to be entered (via clicking on the padlock). Once unlocked it will remain unlocked until Speedstack is closed or the padlock is clicked again.

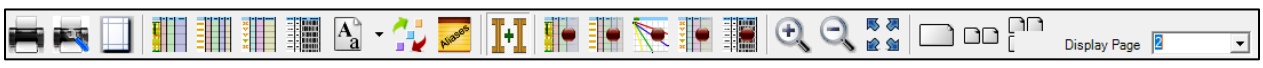
Printing stackup information

To print the stackup information, choose the Print command. Print Technical Report includes stack details, controlled impedance structures – with optional loss frequency graphs for each structure, drill specifications, bill of materials information, frequency dependent properties and information entered into the Stack File Properties.



Speedstack Report Printer toolbar

The Speedstack Report Printer toolbar provides shortcut access to the most commonly used printing commands.



Use these commands to set up the printer, page orientation and margins, font size and printing order, select data columns for display, display or suppress data tables and choose the on-screen zoom levels. Button functions are described below.

 Send report to printer

 Print set up – choose printer, print range, copies

 Page set up – orientation and margins

 Select stack data columns

 Select impedance data columns

 Select drill data columns

 Select BOM data columns

 Change font size

 Select stack/drills/impedance/notes print order

Set note field aliases

  Show expanded drills – toggle wide stack and narrow stack image

 Toggle suppress stack data table

 Toggle suppress controlled impedance data table

 Toggle suppress frequency dependent loss graphs

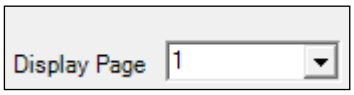
 Toggle suppress drill data table

 Toggle suppress BOM data table

  Zoom in / Zoom out

 Fit page to viewer

 Preview one / two / four pages

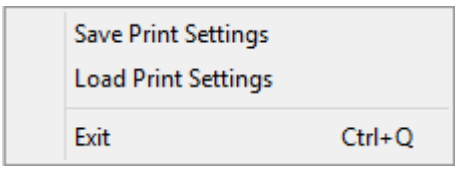


Display Page select

Speedstack Report Printer menu system

File menu

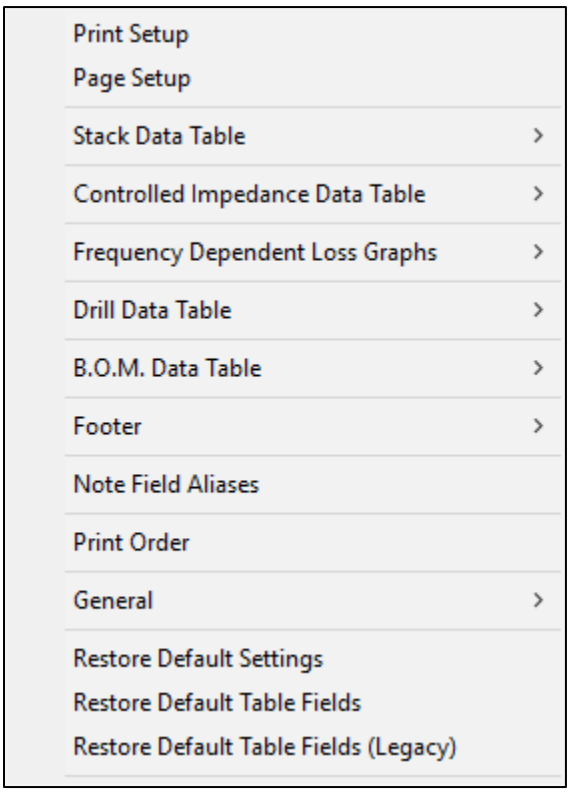
Use the File menu under the Printing window to save and load print settings.



Whichever settings were last used in a session will become the default when the Printing window is next loaded.

Options menu

The Speedstack Report Printer Options menu contains all the settings for printing.



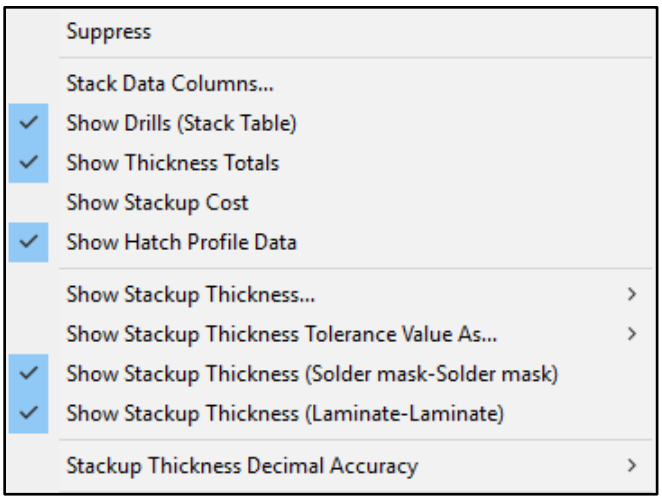
Print Setup

Use the Print Setup command to choose the target printer, along with its properties, the range of pages to print and

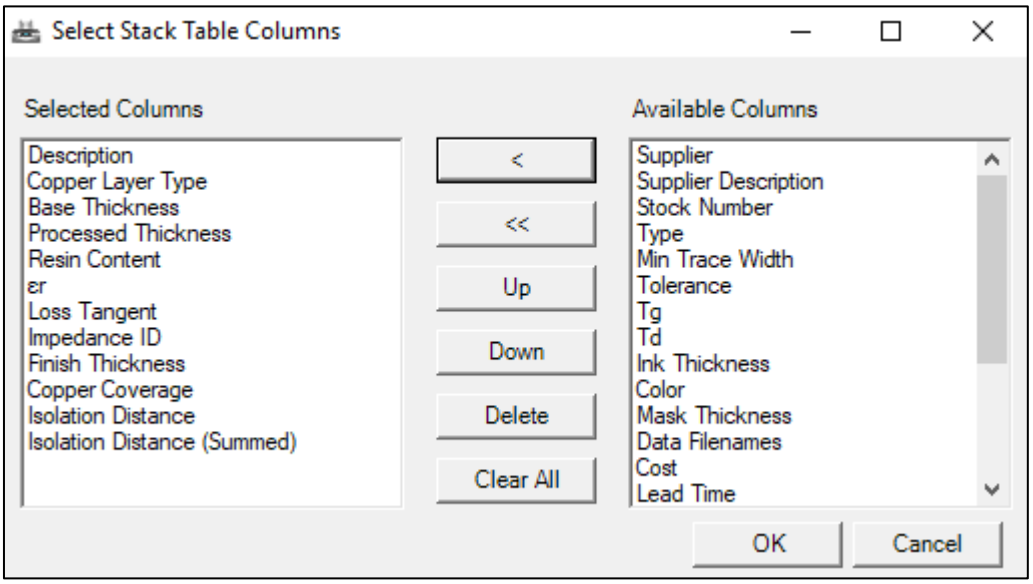
number of copies. Optionally, click the Print to file check box to save the output to a file (e.g. to save the file as a document in PDF format) when printed.

Page Setup
Page Setup displays the Page Setup dialog to change the size and orientation, paper source and margins.

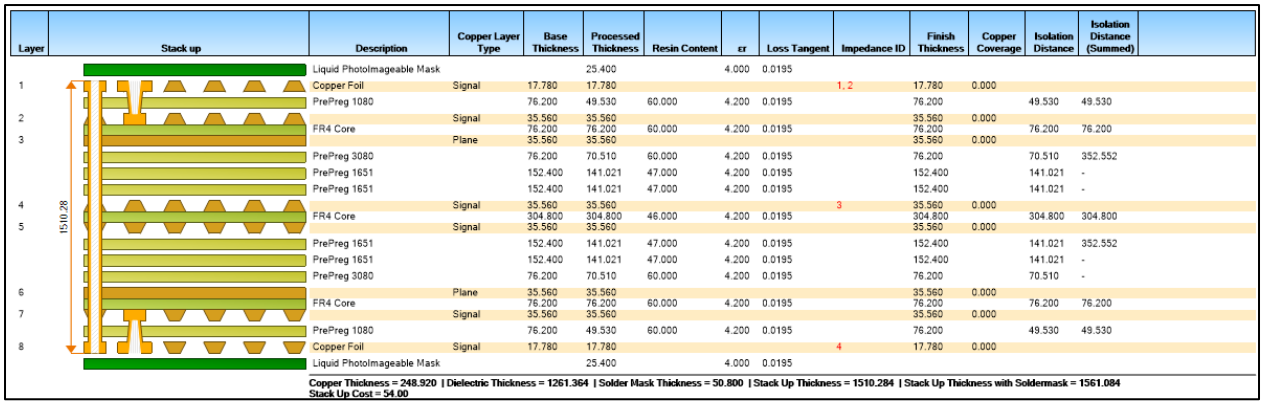
Stack Data Table
The Stack Data Table commands allow for optional display of stack parameters, drills, thickness totals and tolerances.



Stack Data Columns: select, combine and order the data columns available for the stack as desired.



The stack data table is displayed in selected column order:



Layer	Stack up	Description	Copper Layer Type	Base Thickness	Processed Thickness	Resin Content	er	Loss Tangent	Impedance ID	Finish Thickness	Copper Coverage	Isolation Distance	Isolation Distance (Summed)
		Liquid Photoimageable Mask			25.400		4.000	0.0195					
1		Copper Foil	Signal	17.780	17.780				1, 2	17.780	0.000		
		PrePreg 1080		76.200	49.530	60.000	4.200	0.0195		76.200		49.530	49.530
2			Signal	35.560	35.560					35.560	0.000		
3		FR4 Core		76.200	76.200	60.000	4.200	0.0195		76.200		76.200	76.200
			Plane	35.560	35.560					35.560	0.000		
		PrePreg 3080		76.200	70.510	60.000	4.200	0.0195		76.200		70.510	352.552
		PrePreg 1651		152.400	141.021	47.000	4.200	0.0195		152.400		141.021	-
		PrePreg 1651		152.400	141.021	47.000	4.200	0.0195		152.400		141.021	-
4			Signal	35.560	35.560				3	35.560	0.000		
5		FR4 Core		304.800	304.800	46.000	4.200	0.0195		304.800		304.800	304.800
			Signal	35.560	35.560					35.560	0.000		
		PrePreg 1651		152.400	141.021	47.000	4.200	0.0195		152.400		141.021	352.552
		PrePreg 1651		152.400	141.021	47.000	4.200	0.0195		152.400		141.021	-
		PrePreg 3080		76.200	70.510	60.000	4.200	0.0195		76.200		70.510	-
6			Plane	35.560	35.560					35.560	0.000		
7		FR4 Core		76.200	76.200	60.000	4.200	0.0195		76.200		76.200	76.200
			Signal	35.560	35.560					35.560	0.000		
		PrePreg 1080		76.200	49.530	60.000	4.200	0.0195		76.200		49.530	49.530
8		Copper Foil	Signal	17.780	17.780				4	17.780	0.000		
		Liquid Photoimageable Mask			25.400		4.000	0.0195					

Copper Thickness = 248.920 | Dielectric Thickness = 1261.364 | Solder Mask Thickness = 50.800 | Stack Up Thickness = 1510.284 | Stack Up Thickness with Soldermask = 1561.084
Stack Up Cost = 54.00

Use the Drills (Stack Table) command to show or hide the drills in the stackup graphic in the Stack Table.

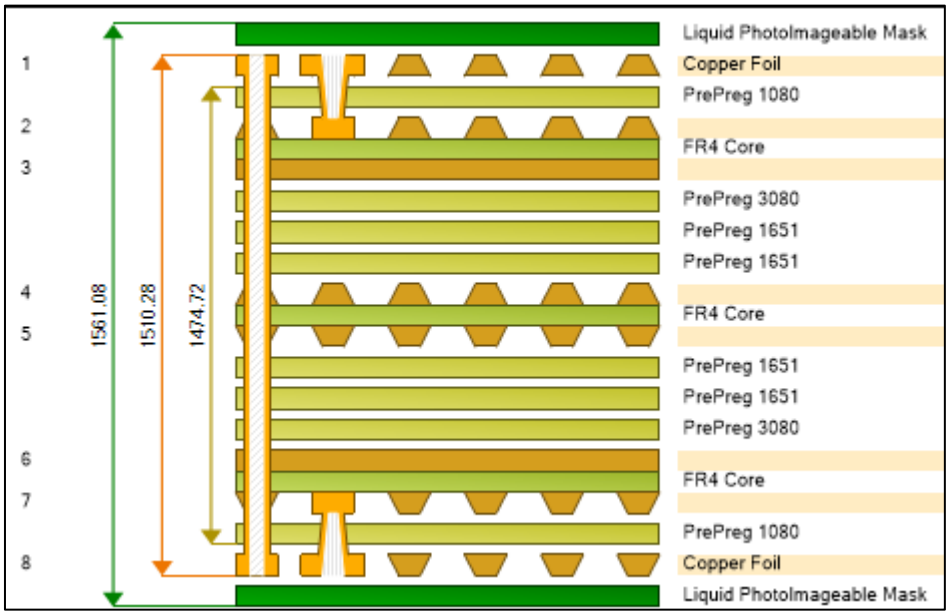
The Thickness Totals provides optional display of the sum of materials thicknesses, copper, dielectric, solder mask and the stackup – with and without the solder mask thickness.

Use the Show Stackup Cost option to display the cost in the stack summary.

Select Show Hatch Profile Data to include the hatch pitch and width and copper area percentage in the stack summary.

Use the Show Stackup Thickness commands to display or hide the target or calculated values of total stack thickness.

Values can optionally include solder mask and laminate thicknesses.

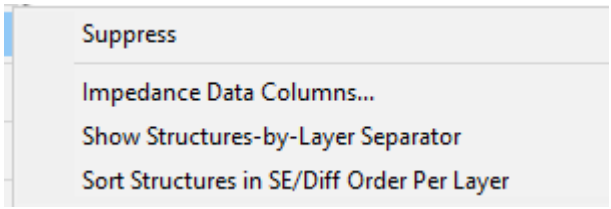


When the target value of the Stackup thickness is chosen the Stackup Thickness Tolerance values can be displayed as percentages of the target stack thickness or as actual values.

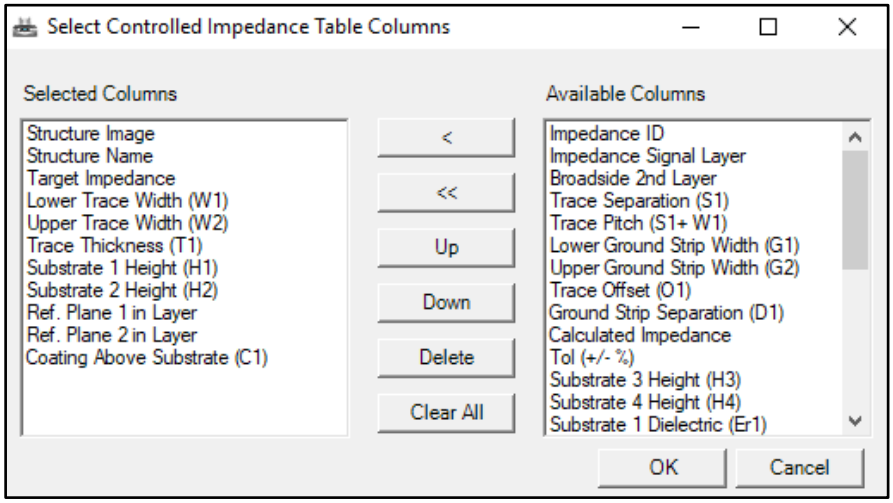
Choose Stackup Thickness Accuracy to display accuracy by number of decimal places.

Controlled Impedance Data Table

Use the Controlled Impedance Data Table options to show or hide the controlled impedance structures and parameters.



Impedance Data columns can be selected for display and ordered as required. Choose the parameters for display from the Available Columns pane and change the order of display using the Up and Down buttons.



Grouping structures by layer

Within the Impedance Data Table structures can be grouped by layer; choose Show Structures-By-Layer Separator. The Separator will add a black structure separator bar on the print out between structure groups, allowing the structures to be sorted by layer number rather than the order that the structures are added to the stack.

Structure Image	Structure Name	Target Impedance	Calculated Impedance	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Thickness (T1)	Substrate 1 Height (H1)	Substrate 2 Height (H2)	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Coating Above Substrate (C1)
	Coated Microstrip 1B	75.000	75.870	114.300	88.900	17.780	161.290	0.000	3	0	25.400
	Edge Coupled Coated Microstrip 1B	100.000	100.350	215.900	190.500	17.780	161.290	0.000	3	0	25.400
	Edge Coupled Offset Stripline 1B1A	100.000	101.280	184.150	158.750	35.560	692.912	388.112	3	6	0.000
	Coated Microstrip 1B	75.000	75.870	114.300	88.900	17.780	161.290	0.000	6	0	25.400

Sorting impedance structures by type

The technical report, by default, prints the structures within a layer in the order in which they were added to the stack.

In the example stack below the structures were added to the stack in the order shown.

Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Target Impedance	Tol (+/- %)	Calculated Impedance
1		Edge Coupled Coated Microstrip 1B	1	3	0	8.500	7.500	8.115	100.000	10.000	100.350
2		Coated Microstrip 1B	1	3	0	4.500	3.500	0.000	75.000	10.000	75.870
3		Coated Microstrip 1B	1	3	0	11.476	10.476	0.000	50.000	10.000	49.520
4		Edge Coupled Coated Microstrip 1B	1	3	0	12.542	11.542	10.000	85.000	10.000	85.220

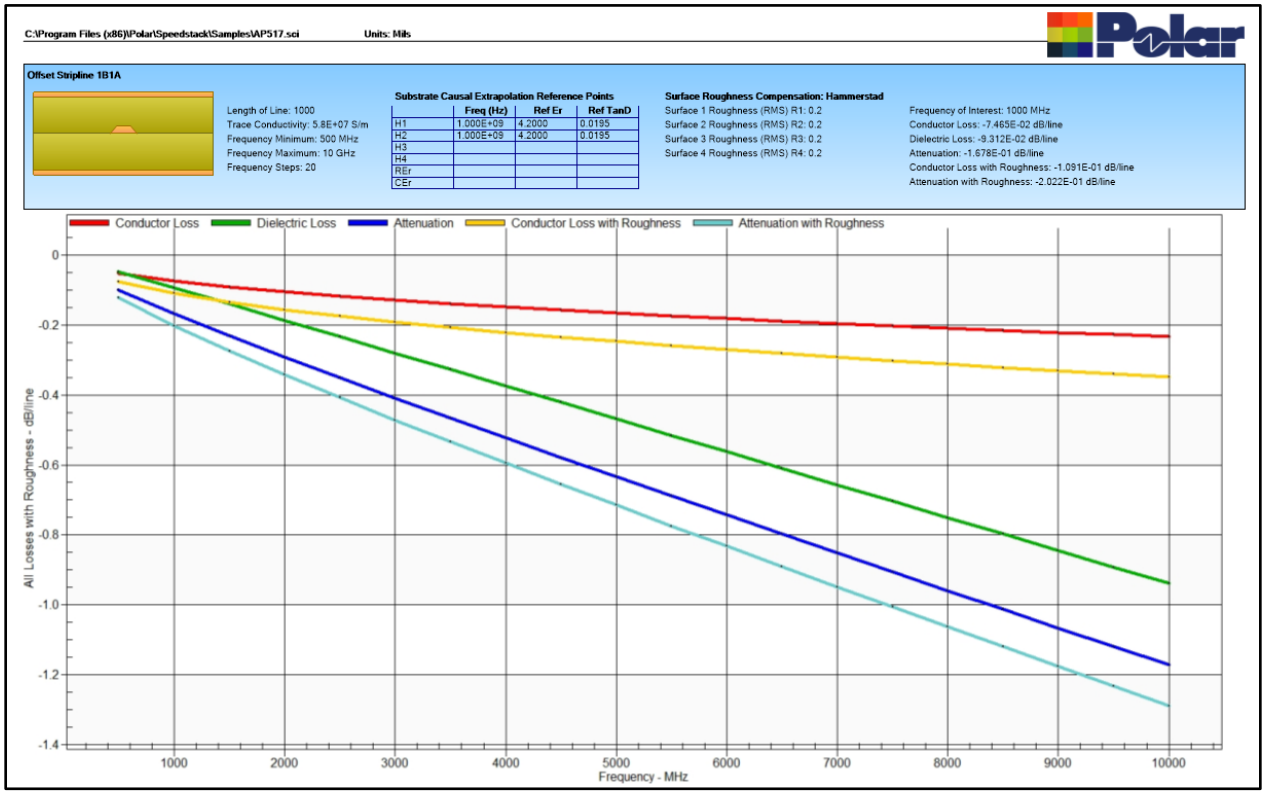
Structures within each layer can be grouped by type, single ended and differential.

To sort the structures by type choose the Sort Structures by SE/Diff Order per Layer; the structures within each layer will be ordered in single ended then differential order as shown in the graphic below.

Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Target Impedance	Tol (+/- %)	Calculated Impedance
2		Coated Microstrip 1B	1	3	0	4.500	3.500	0.000	75.000	10.000	75.870
3		Coated Microstrip 1B	1	3	0	11.476	10.476	0.000	50.000	10.000	49.520
1		Edge Coupled Coated Microstrip 1B	1	3	0	8.500	7.500	8.115	100.000	10.000	100.350
4		Edge Coupled Coated Microstrip 1B	1	3	0	12.542	11.542	10.000	85.000	10.000	85.220

Frequency dependent loss graphs

Speedstack Si provides graphing and tabular display of the frequency dependent properties of each controlled impedance structure in the stackup. The technical report includes the option of displaying the loss v frequency graph of every structure in the stackup – see below.



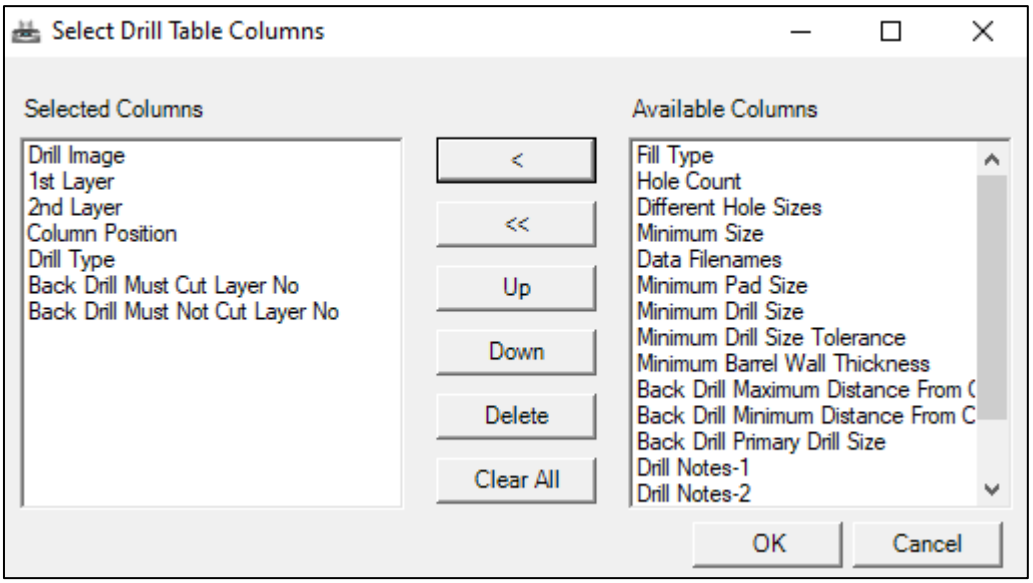
When the technical report is selected for print Speedstack recalculates and displays the loss v frequency for the frequency dependent properties of each structure in the stackup.

The display for each structure includes the structure graphic and the associated frequency dependent parameters, the substrate causal extrapolation reference points, the surface roughness method and settings and the losses and attenuation at the user defined frequency of interest.

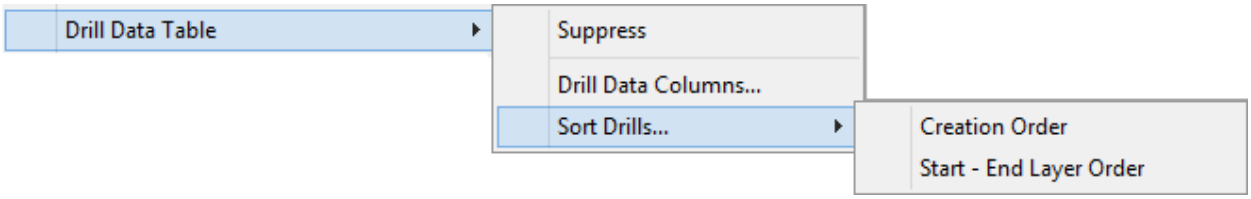
From the Options menu, choose Frequency Dependent Loss Graphs|Suppress to toggle display of frequency dependent loss graphs and tables.

Drill DataTable

Use the Drill Data Table command to show or hide the table of drill parameters and to select and order parameter values for display.

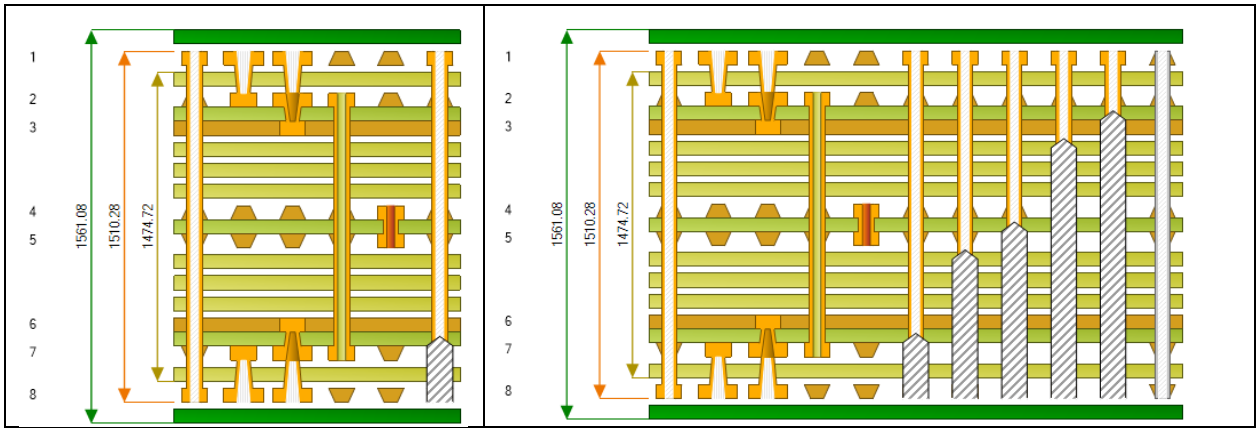


Use the Sort Drills… command to order the drill table – drills can be sorted by start-end layer order or creation order.



Showing expanded drills

Speedstack can display up to eleven drill columns in a stack. but many users won't ever need more than six columns. I to allow the user to toggle between wide stack and narrow stack image mode. f they would prefer to use the horizontal space for data columns they can select the narrow stack up image. If drills exist beyond column six and narrow stack mode is selected we display a warning.



Bill of Materials Table

Speedstack's Technical Report incorporates the Bill of Material (BOM) table with the stock-number displayed optionally as a barcode. The table contains fields for Total Quantity (No. Panels * Stack Quantity) and Total Cost (Unit Cost * Total Quantity.)

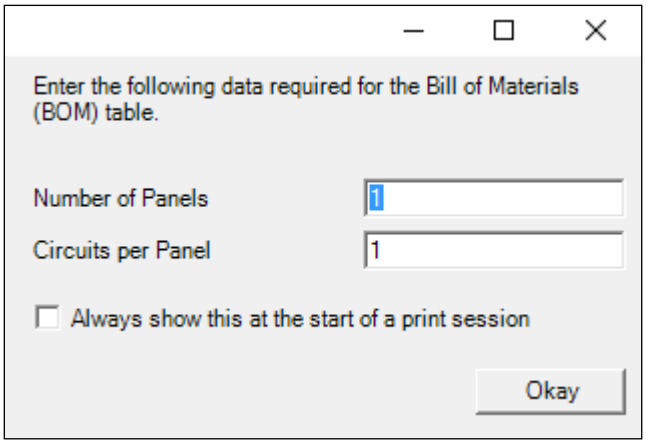
Supplier	Supplier Description	Description	Type	Stock Number	Stack Quantity	Unit Cost	Stack Cost	Total Quantity	Total Cost
Polar Samples	SM/001	Liquid PhotoImageable Mask	SolderMask		2	0.00	0.00	2	0.00
Polar Samples	FO/001	Copper Foil	Copper		2	1.00	2.00	2	2.00
Polar Samples	PP/001	PrePreg 1080	Dielectric		2	1.00	2.00	2	2.00
Polar Samples	CO/005	FR4 Core	FR4		2	5.00	10.00	2	10.00
Polar Samples	PP/002	PrePreg 3080	Dielectric		2	2.00	4.00	2	4.00
Polar Samples	PP/004	PrePreg 1651	Dielectric		4	4.00	16.00	4	16.00
Polar Samples	CO/020	FR4 Core	FR4		1	20.00	20.00	1	20.00
							54.00		54.00

No. of Panels = 1 | Circuits Per Panel = 1 | Price Per Circuit = 54.00 |

The table includes totals for the Stack Cost and the Total Cost columns.

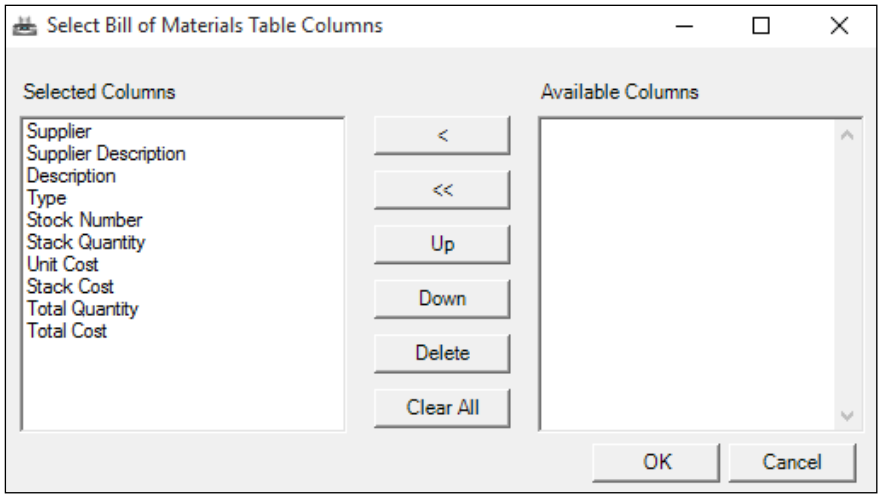
A summary section presents 3 values: No. of Panels, Circuits Per Panel and Price Per Circuit. The No. of Panels and Circuits Per Panel can be entered by the user at any time or optionally at the start of each print session.

From the Options menu choose B.O.M. Data Table | Panels / Circuits per Panel…

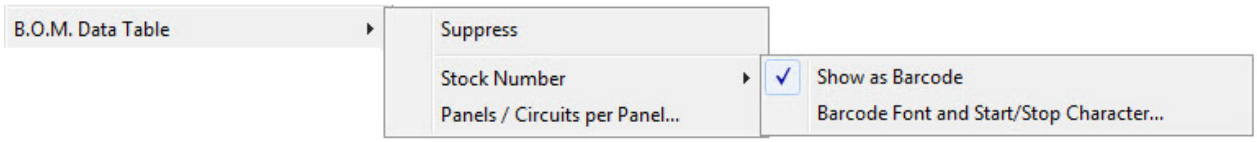


Price Per Circuit is a calculated value (Total Stack Cost / Circuits Per Panel).

Bill of Materials Table columns can be selected for display and ordered as required. Choose the parameters for display from the Available Columns pane and change the order of display using the Up and Down buttons.



From the Options menu choose B.O.M. Data Table to display or suppress the table. The Suppress command toggles the B.O.M. table on and off in the report.

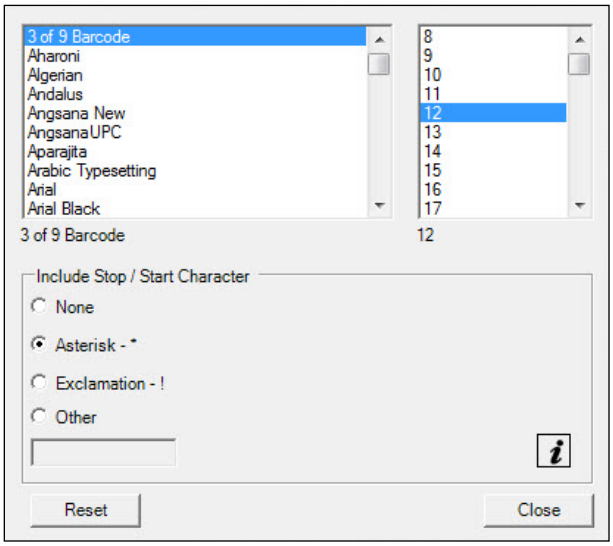


Stock numbers can be displayed in alpha-numeric form or as barcodes. Choose Stock Number|Show as Barcode to toggle the Stock Number display between barcodes or alpha-numeric text.

Description	Type	Stock Number	Stack Quantity	Unit Cost
Liquid PhotoImageable Mask	SolderMask		2	0.00
Copper Foil	Copper		2	1.00
PrePreg 1080	Dielectric		2	1.00
FR4 Core	FR4		2	5.00
PrePreg 3080	Dielectric		2	2.00
PrePreg 1651	Dielectric		4	4.00
FR4 Core	FR4		1	20.00

Choosing the bar code font

From the Stock Number command choose Barcode Font and Start/Stop Character. The Select Barcode font and Start/Stop Marker Characters dialog is displayed.



Choose the font and font size and the start / stop character as appropriate. (The barcode font must already installed on the host computer.)

Choosing the start/stop character

The Start/Stop character is a requirement for certain barcode types such as Code 39 (also referred to as Code 3 of 9, Code 3/9, Type 39, etc.) The Code 39 asterisk character is normally reserved as a start/stop character rendering the data a valid barcode.

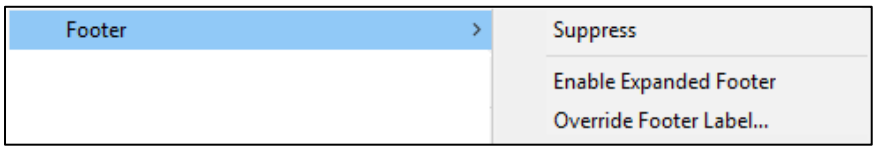
As an example, if the Stock-Number is 123-456, selecting the Asterisk option will add enclosing asterisks to the Stock-Number so that the barcode is valid.

(In some instances asterisks may already be included in the Stock-Number in which case choose the None option.)

There are other situations where another character may be used. Exercise caution when determining the appropriate font choice and start/stop character to use. In the event that an inappropriate font is chosen, the results may be unpredictable.

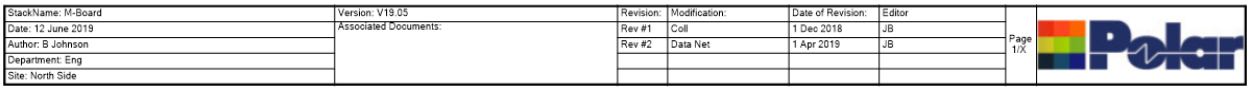
Footer

The report footer section is an optional item and may be displayed or suppressed (hidden).



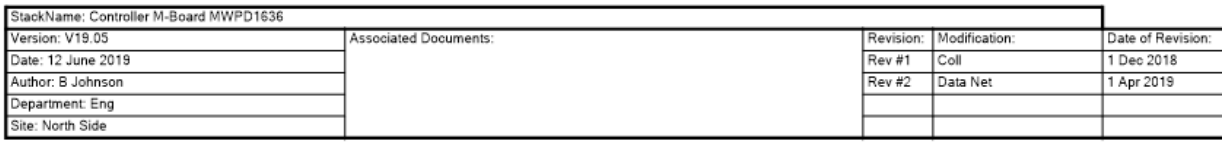
Suppressing the footer

When the Footer section is suppressed the space is used for other data, often reducing the number of pages required for the technical report.



Using the expanded footer

Use the Expanded Footer option to allow longer and more descriptive stack names to be displayed.

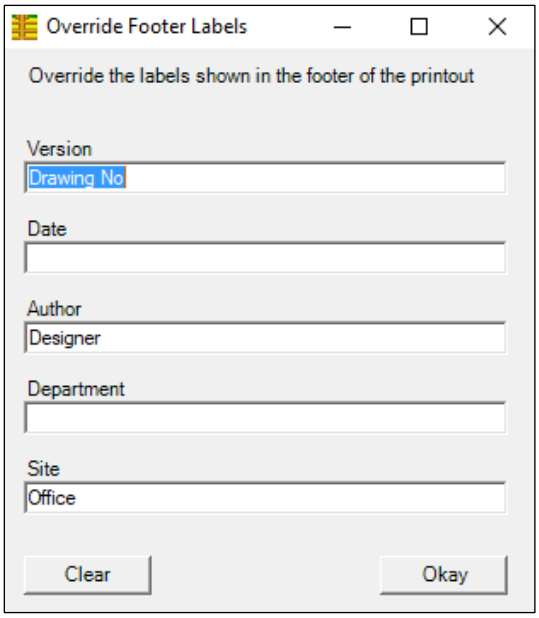


Overriding the footer labels

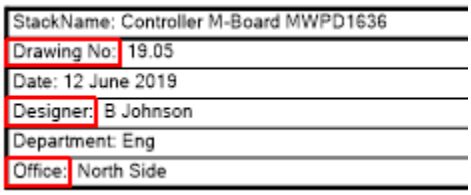
The labels in the footer may be changed to reflect the stackup design workflow and organisational structure.

Choose Footer | Override Footer Label…

The Override Footer Labels dialog is displayed:



The new labels will be reflected in the footer:

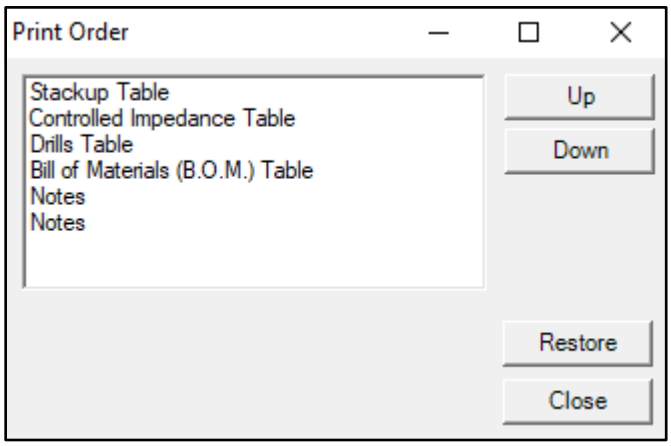


Note Field Aliases

Note Field Aliases allows for the free-text note fields (for the Stack and Controlled impedance tables) to be given descriptive names.

Print Order

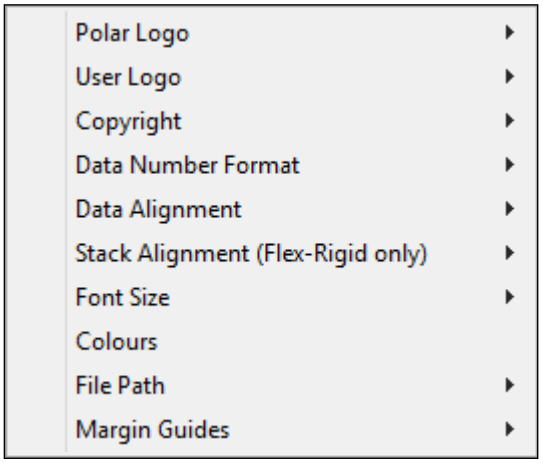
Use the Print Order dialog to move the Controlled Impedance Table, Drill Tables and Notes sections up or down within the report.



Note: the Stack/Materials data Table cannot be reordered and must remain the first item in the print order.

General options

Use the General Options to specify



Polar Logo: toggles on and off the Polar Instruments logo.

User Logo: toggles on and off the user-defined logo (as set in the application configuration).

Copyright: toggles on and off the copyright information and allows copyright test to be edited.

Data Number Format: sets the precision of numeric data in the printout.

Data Alignment: specifies alignment (left, centre, etc.) for stack, impedance and drill data.

Stack Alignment (Flex-Rigid only): – Align to Master Stack allows the vertical position of sub-stacks (printed on separate pages within the report) to be preserved with respect to the master stack; Align to Page Top presents each sub-stack at the top of each page.

Colours: allows for the colours of items within the report to be customised. Click Override Default Colours and Change to specify the new colour. Click Reset All to return to the default colours.

File Path: toggles on and off the file path/file name

Margin Guides: toggles on and off boundary markings (in the user selected units.) These match the Speedstack units selected within the Stackup Editor | Units menu.

The margin guides allow for display of the printable area of the page – which can vary depending upon the device – even though the page size remains the same. (With some devices the report cannot use the full extents of the page.)