Automated PCB Stackup Design System

User Guide

Speedstack 2008

Polar Instruments Ltd

Polar Instruments Ltd.
Garenne Park
St. Sampson
Guernsey
Channel Islands
GY2 4AF
ENGLAND

Fax: +44 (0)1481 252476

email: mail@polarinstruments.com
http://www.polarinstruments.com

MAN 199–0802

Speedstack 2008 User Guide

POLAR INSTRUMENTS LTD

Speedstack Specifications

Maximum layer count	64+
Via rules	Conventional, blind and buried
Materials library	Foils RCC foils Cores Prepreg Solder mask Ident Peelable mask Coverlay
Post press compensation	Yes (user defined)
Finished thickness compensation	Yes
Cu thickness calculation	Yes
Board thickness calculation	Yes
User library	Yes
Save builds	Yes

Personal Computer Requirements

Computer	IBM PC AT or compatible
Processor	Pentium 1GHz or better
Operating system	Windows 2000 SP4, Windows 2003 SP1, Windows XP SP1 or later
Environment	Requires .NET Framework v1.1
System memory required	512MB recommended
Hard disk space required	200MB (min.)
Video standard	XGA (1024 x 768) or higher Hi color 16 bit or higher
CDROM drive	
Mouse	Microsoft compatible
Licensing	Fixed: Parallel/USB key
	Floating FlexLM licence (Windows servers only)

Guide To The Manual

Introduction	Introduces the Polar Instruments Speedstack.
Getting started with Speedstack – Autostack	Steps through the process of using Autostack to create a simple stack from a set of manufacturer's data.
Using the Speedstack	Discussion of the Speedstack user interface; creating and editing stackups.
Adding controlled impedance structures	Working with the Si8000/Si9000 field solver to add controlled impedance structures to the stackup model. Using the goal seeking facilities of the field solver to obtain the correct impedance for a structure.
The Speedstack Materials libraries	Using the Speedstack materials libraries, creating new libraries, adding material to the library.
Design rule checking	Using the Speedstack Design Rule Checker to correct stackup design errors.

Contents

Introduction to Speedstack

The Speedstack Stackup Design System

With its Autostack VSR (Virtual Stack Realization) engine the Polar Speedstack PCB Stackup Design System is designed to automate the PCB stack design process and deliver significant reductions in the amount of time consumed in PCB stackup documentation and control. Given designer specifications the PCB fabricator can use the Speedstack Stack Builder to create in just a few steps the most cost effective stack for the range of available materials. The Speedstack offers interconnect designers (PCB layout engineers), PCB front-end engineers and fabricators a fast and professional solution to layer stackup creation. The Speedstack software provides formal documentation for everyone involved in ensuring the correct materials are used in the build process. Each potential stack is built by the Speedstack Autostack Virtual Stack Realization engine over 10000 times in order to predict the finished thickness yield, providing confidence that production yields will be achieved.

Speedstack PCB

Speedstack is a powerful PCB layer stackup design tool featuring both automatic layer stackup generation and powerful stackup editing capabilities. For PCB fabricators Speedstack PCB interfaces with the industry standard Polar Si8000m Controlled Impedance Design System. It includes a link and license for Polar's Si8000m controlled impedance design system, using the proven Polar Si8000m multiple dielectric boundary element field solver to provide the impedance data for the stack. In addition, Speedstack PCB licence holders have full access to the stand alone Si8000m Quick Solver licence.

Speedstack PCB is especially tailored for PCB fabricators and PCB brokers – any one with a requirement to design or communicate controlled impedance PCB stackups. Speedstack PCB customers are able to share stackups and read impedance requirements from designers who are using Speedstack Si.

Speedstack Si

For electronic engineers involved in stackup design Speedstack Si interfaces with the Polar Si9000e Transmission Line Design System.

Both Speedstack Si and Speedstack PCB are able to directly output controlled impedance test files associated with each stackup. For the fabricator this is an ideal way to link the impedance test requirements to a particular job. For the OEM this offers a clear method of sending impedance test specifications out to suppliers or brokers. Designers and fabricators can work together and select the best material combinations for minimising build costs. Fabricators can share their in house material libraries with OEMs and ensure the most effective material choice is employed in the build.

3 routes to stackup creation

Polar's Speedstack can provide automatically built stacks with its Autostack facility but users who require more control over the stack creation process may specify the stackup semi-automatically with the powerful Stackup Wizard or alternatively build the stack manually, layer by layer. Speedstack is flexible and allows full manual editing of stacks created under the Autostack VSR (Virtual Stack Realization) engine or the Stackup Wizard.

Easy stackup editing

The Speedstack allows the user to view stackup in 2D or 3D format. Layer and material annotation is clear and easy to read and each layer may be selected and queried to display the associated material type and properties, including the associated data file. Visible drill information ensures that designers instantly know which layers support conventional, blind and buried vias.

Speedstack allows you rapidly to build and share stacks and verify via aspect ratios and track spacing rules. The stack file contains base material information combined with layer description and a complete listing of transmission line structures deployed in the stack. Keeping all stack information in one file ensures that manufacturing data is accurately shared between original designer and fabricator.

Integration with the Si8000/Si9000

The Speedstack is fully integrated with the Polar Si8000 Controlled Impedance Quick Solver and the Si9000 PCB Transmission Line Field Solver so the user can quickly add controlled impedance structures to layers in the stackup. The designer or board fabricator can use the Goal Seek facility of the Si8000/Si9000 to arrive rapidly at the controlled

impedance structure parameters to produce the target impedance.

Materials library

The Speedstack supports a flexible materials library. This allows the designer to use standard materials data and also provides the facility to create new material libraries. PCB fabricators can also build libraries of commonly stocked materials to give interconnect designers visibility of the materials held in stock. Speedstack thus supports three types of library – custom user libraries of materials, generic designer libraries of materials of given dielectric characteristics (for example, thicknesses) along with a comprehensive set of materials libraries from PCB base material suppliers who are members of the Polar Speedstack Material Partner program.

Preferred builds

PCB fabricators are able to create and share preferred builds and exchange the associated information with designers. Build information also includes blind and buried via information. This simplifies the task of sharing stackup and drilling information between board shops and the design community.

Dimensional information

Finished board thickness is a critical dimension in many applications; the Speedstack keeps track of the finished PCB thickness and tolerance, and allows fabricators the flexibility of adding in-house post-press thickness for prepreg layers. Additionally, Speedstack takes into account plating thickness where appropriate.

High layer count boards

On boards with high layer counts it can be very easy to make a change that would produce a non-symmetrical stack. The Speedstack Design Rules Check monitors symmetry across the stack, and ensures that material symmetry is maintained. Speedstack also makes it easy to set the symmetrical build mode to ensure that any changes you make are applied equally across the stack.

Documentation and file format

In addition to saving the stack in efficient electronic format, Speedstack outputs stack graphics in a variety of formats to suit your requirements. Stack data may be output in GERBER, DXF, bitmap, JPEG and XML. In addition, the stack data can be exported in comma-separated form for inclusion in other systems. Speedstack's customisable

printouts make it easy to discuss alternate builds and pricing impacts with fabricators.

Applications engineers, front end and production engineers benefit from receiving stack information in an intuitive, easy to understand format. The Speedstack .sci file contains full details of the layer stackup of a particular job. If changes are necessary or preferred stacks are to be shared with customers, Speedstack can cut the time for documentation and information sharing to a fraction of the time taken when employing traditional methods such as spreadsheet, word processor or presentation software.

Supplier management

When multiple-sourcing PCBs or when moving from prototype to volume production, the stack and fabrication design rule checks ensure that the manufacturing capabilities of your chosen suppliers are not overlooked. In addition the professional documentation output from the SB8000/SB9000 ensures that layer stack information is accurately conveyed to PCB suppliers.

Graphical interface

The Speedstack offers an easy to interpret graphical interface. Clearly showing the layers supporting blind and buried vias, the Speedstack also records the data file for each layer (including ident and peelable mask layers). The graphical interface is especially designed to simplify the process of communication between interconnect designer and fabricator. OEMs who need to manage boards sourced from multiple suppliers will also find this facility invaluable. In addition to physical layers Speedstack adds mask and notation for electrical layers.

Installing Speedstack

Installing and activating Speedstack

It will be necessary to install and activate the product license and set operating options prior to building stacks or performing calculations with Speedstack. Consult your Polar representative for installation/activation directions.

Uninstalling the software

Caution Prior to uninstalling, make a copy of the Speedstack folder structure and store in a safe place.

To uninstall the Speedstack software, click the Windows Start button and choose Settings and Control Panel.

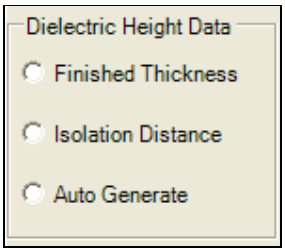
Double-click Add/Remove Programs and choose Speedstack from the list. Click Remove.

Getting started with Speedstack – Autostack

Creating a stack with Autostack

The Polar Instruments Speedstack PCB Stackup Builder allows users to create and modify stacks manually via the Stack Editor or automatically using Autostack. This section steps through the process of using Autostack to create a simple stack from a set of manufacturer's data. When completed the stack will be transferred to the Stack Editor for manual editing.

Autostack offers three methods of specifying dielectric height, Finished thickness, Isolation distance and Auto Generate.



In this example we assume the values of dielectric height are unknown and select the Auto Generate method. For a discussion of calculating dielectric height with Speedstack refer to Polar Instruments Application Note AP507.

When using Auto Generate the dielectric heights are calculated automatically so only the following information is required (the manufacturer's sample data values chosen for this example are typical for a standard PCI card):

- The overall board thickness – in this example we specify 64 mil (1.6mm) ± 10%.
- Build type (foil or core)
- A reference dielectric constant – in this example, 4.2.
- The controlled impedance requirements:

  – 50 ohm (±10%) single-ended on Layer 1 referenced to Layer 2. Trace width (W1) 22 mil ~ 0.56mm.

  – 100 Ohm (±10%) differential on Layer 1 referenced to Layer 2. Trace width (W1) 13 mil ~ 0.33mm, Separation (S1) – 9 mil ~ 0.23mm.

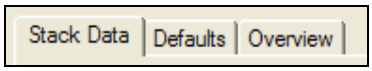
– 100 Ohm (±10%) differential on Layer 3 referenced to Layers 2 and 5. Trace width (W1) 6 mil ~ 0.15mm, Separation (S1) – 7.5 mil ~ 0.19mm.

– 75 Ohm (±10%) single-ended on Layer 6 referenced to Layer 5. Trace width (W1) 9.5 mil ~ 0.24mm.

- The trace dimensions and their tolerances – ± 20%.
- Finished copper weights – 1oz, 1.4 mil (35um).
- Solder mask requirements.

Inputting designers' information into Speedstack

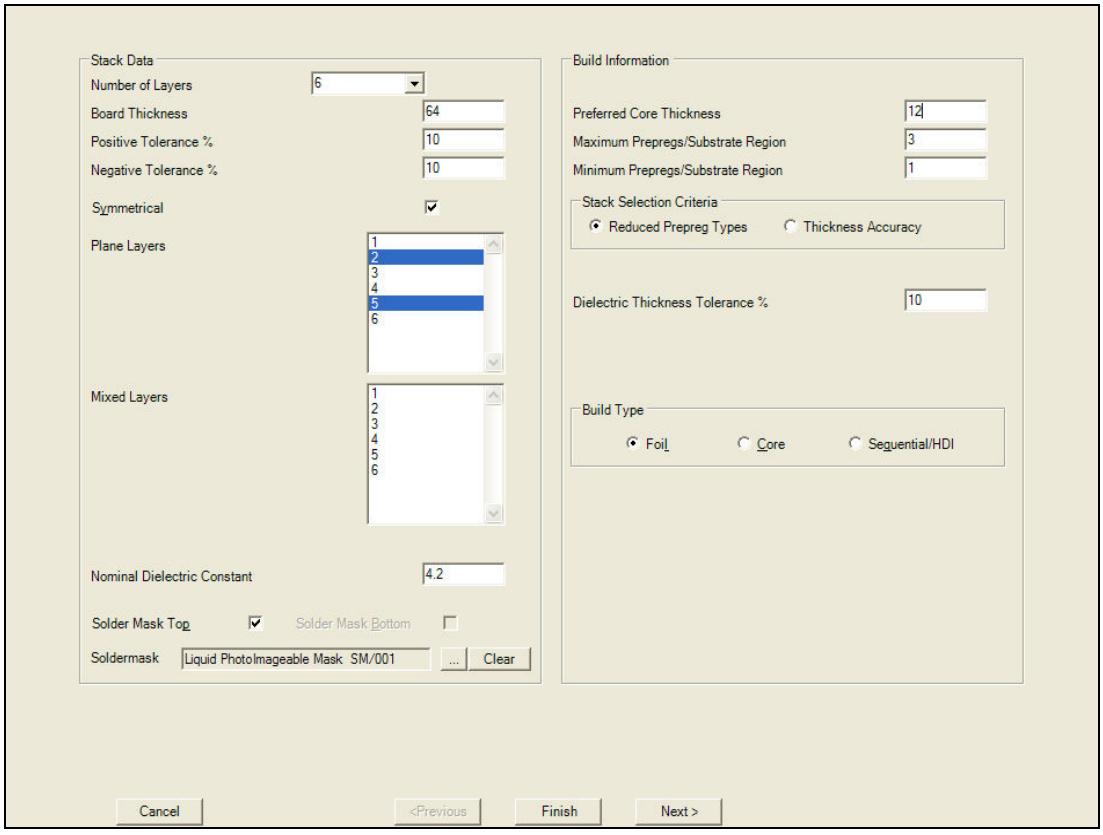
When Speedstack is first opened the Stack Builder screen is displayed. The Stack Builder screen allows for selection between stack data, the project defaults and stack overview.



The Stack Data screen provides a data entry interface for specifying stack parameters and predefined material filters.

Creating a new stack

From the File menu Choose New to begin a new stack. The Stack Data screen is displayed; enter the values from the manufacturer's data:



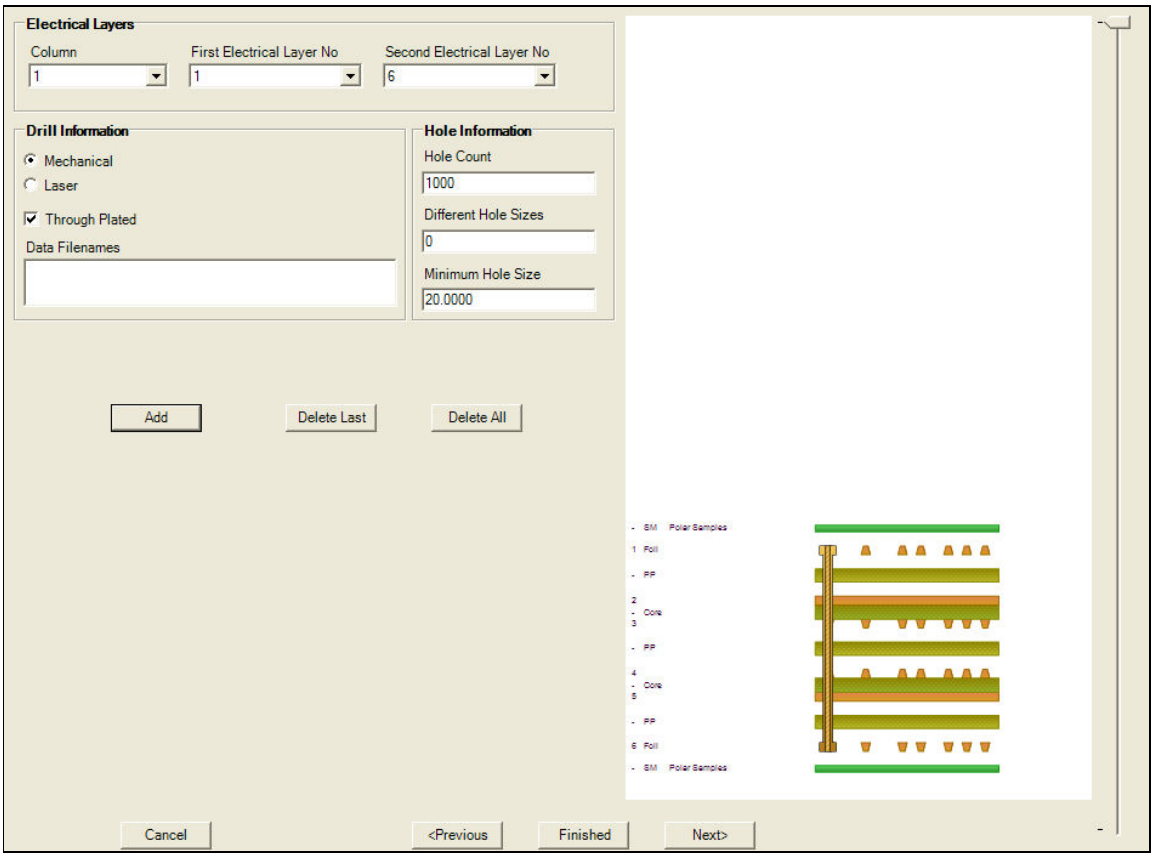
Adding stack data

For this example we specify a board thickness of 64 mil (1.6mm) and a tolerance of 10%.

We specify a symmetrical build, designate layers 2 and 5 plane layers and choose a solder mask from the materials library. Note that for a symmetrical build it is only necessary to specify a mask for the top layer.

We specify a dielectric constant of 4.2, a preferred core thickness of 12 mil and a maximum of 3 and minimum of 1 prepreg per substrate region and choose to build the stack with a minimum of prepreg types (in some applications accuracy of finished thickness will be of greater importance than reducing the number of prepreg types).

For this example we specify a Foil build. Click Next to progress to the Add Drills screen.

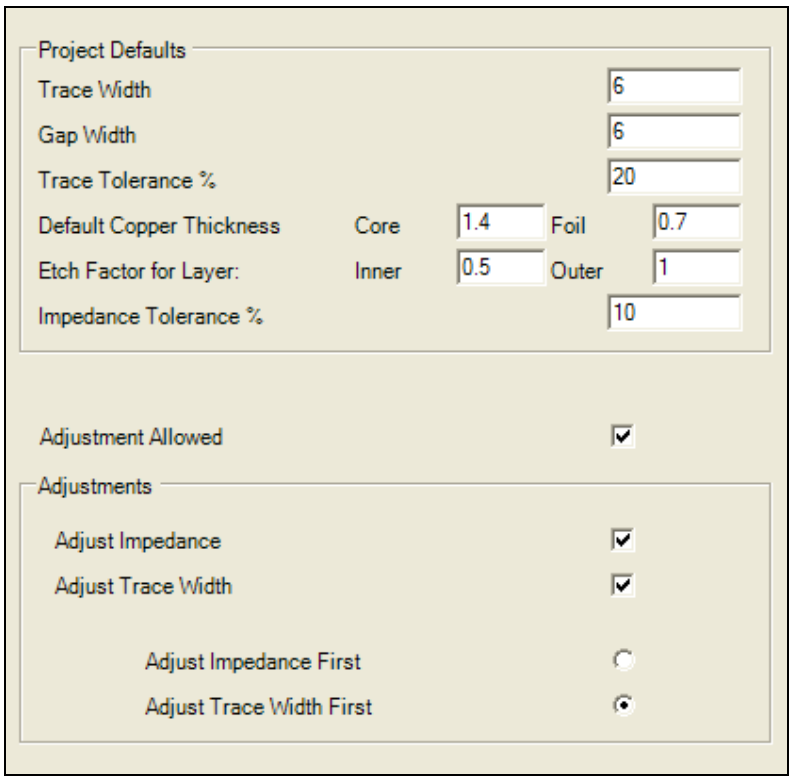


Adding drills

From the Add Drills screen choose the drill type, mechanical or laser and, for each drill, the first and second electrical layers; click Add. Up to six drill columns can be specified; for this example we specify a minimum hole size of 20 mil.

Changes made to the stack are reflected in the stack overview graphic. Click Next to display the Project Defaults screen

Use the Defaults screen to provide controlled impedance structure defaults for the current Autostack session.



The Project Defaults screen provides default values as a starting point for the impedance structures and other settings and provides for minor adjustments of impedance and trace widths to allow the Si8000/SI9000 goal seeker to produce a stack meeting all specifications.

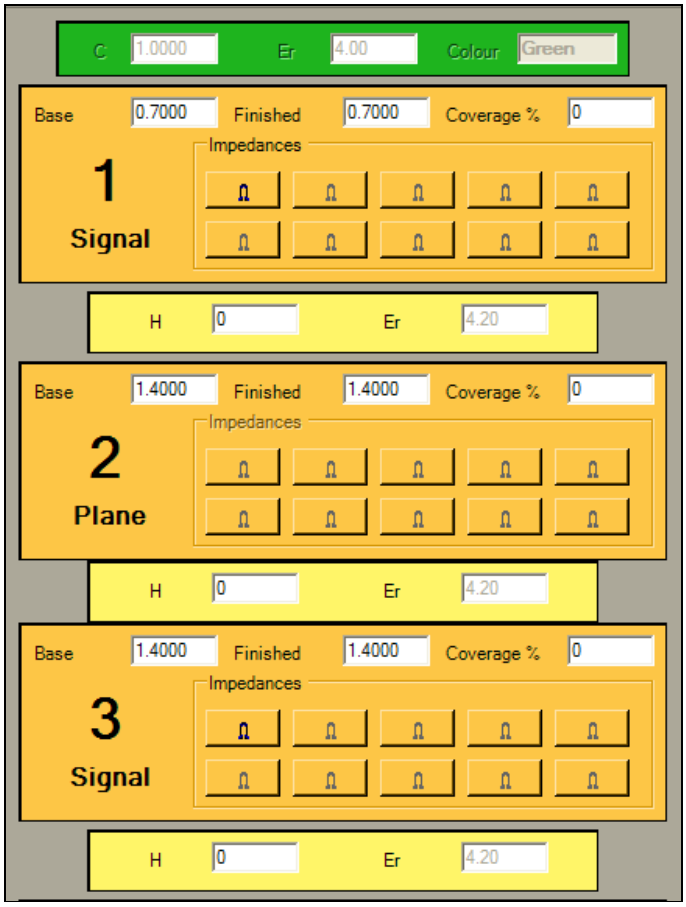
Set trace and gap widths, copper weights and etch factors to the values shown.

Impedance and trace width adjustments

Click the Adjustments Allowed check box to enable the adjustments options and allow the target impedance and the trace width to be adjusted within specifications; allow the trace width to be changed first. Click Finish; the screen returns to the Stack Definition Page with its graphical representation of the data fields.

With the stack defined we can add the finished copper weights and the impedance structures. In this example symmetrical mode has been selected so layer type and H values are disabled on the lower half of the stackup.

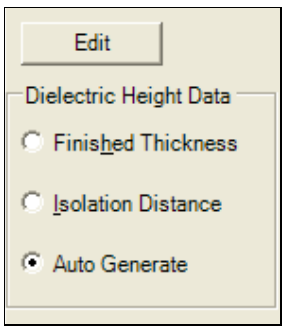
Note: Although the stack is defined as symmetrical, controlled impedance structures can be specified on an individual layer basis.



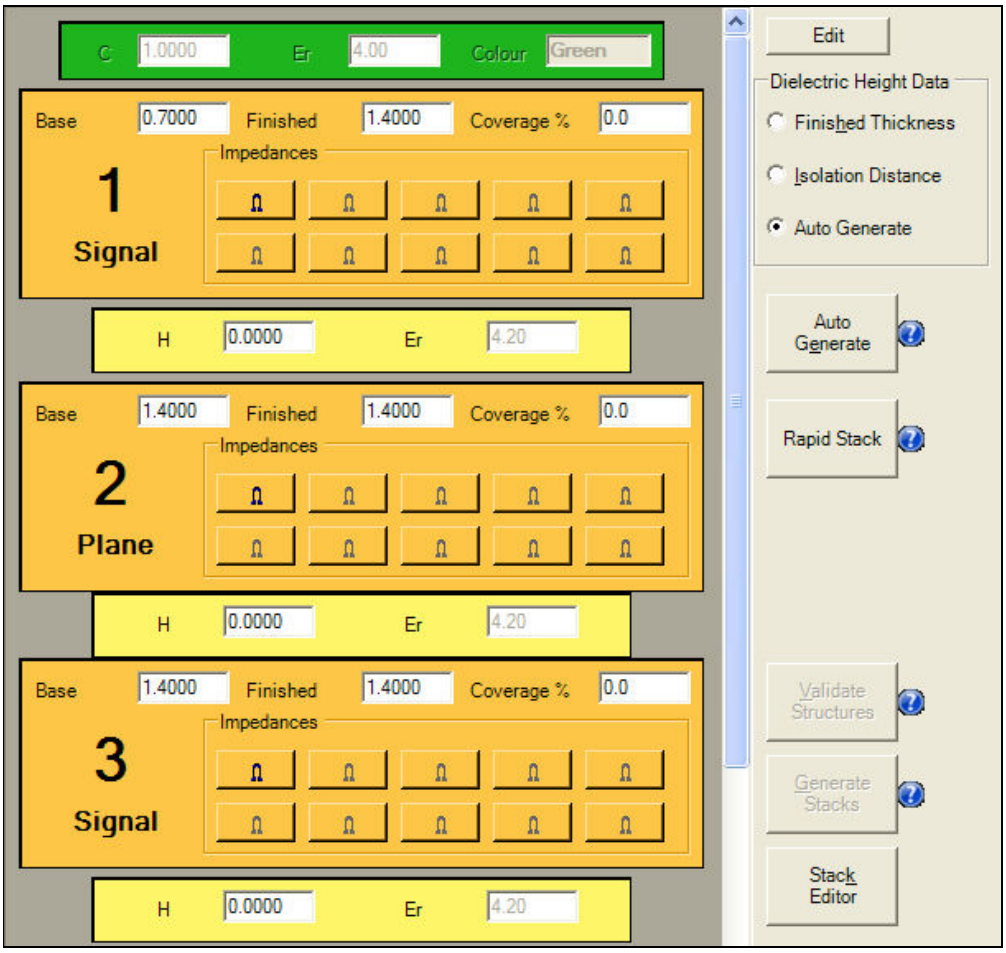
Adding copper weights

The stack is symmetrical so only the top half of the stack is shown. The finished copper weights – 1.4 mil ~ 35um – are taken from the sample designer supplied data. Note that the signal and plane layers and core and prepreg layers are shown as designated.

From Dielectric Height Data select the Auto Generate option to enable Autostack to derive dielectric heights automatically.

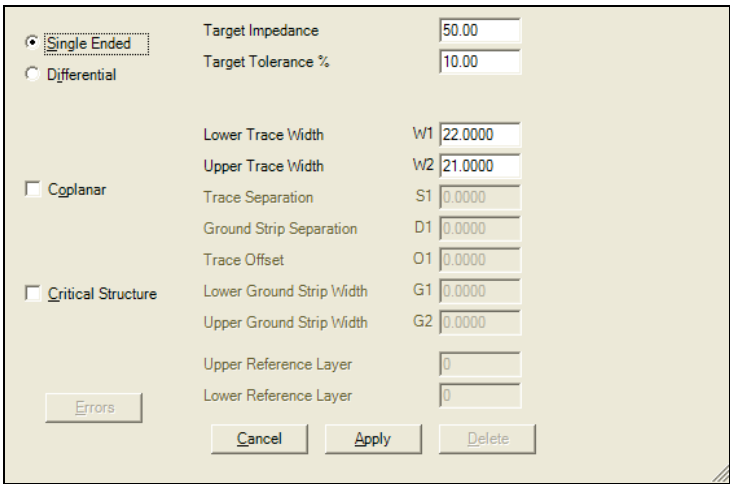


As symmetrical mode has been specified it is not necessary to setup layers 4, 5 and 6. Stack definition data supplied for layers 1 – 3 will be reflected into the lower half of the stack.

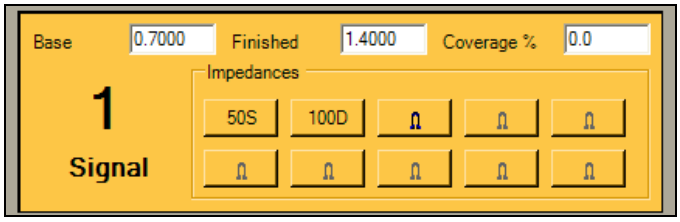


Adding impedance structures

Click the upper left Impedance button on Layer 1 to specify the first impedance structure via the Structure Data dialog – 50 ohm (±10%) single-ended on layer 1 referenced to layer 2. Trace width (W1) 22 mil ~ 0.56mm.



Click Apply and repeat for the remaining structures on their associated layers.



Up to ten impedance structures may be specified for each layer, note that for each impedance defined the omega symbol has been replaced with text describing the structure.

Click Auto Generate to create a set of candidate stacks that match the stack definition criteria.

Cost	Number Of	Prepreg Type	Lead Time	σ	-3 σ	Nominal Thickness	+3 σ
64	7	2	0	1.4062	61.9633	66.16	70.4003
65	7	2	0	0.9849	62.9306	65.86	68.84
66	6	1	0	2.1179	59.7689	66.16	72.4762
67	6	2	0	1.8902	62.3368	68.06	73.6779
67	7	2	0	1.4114	61.8894	66.16	70.3575
68	7	2	0	1.8455	62.5323	68.16	73.6055
68	8	2	0	1.5689	61.4105	66.16	70.8241
68	8	2	0	1.6158	61.2288	66.06	70.9238
69	9	1	0	1.6311	61.168	66.16	70.9544
70	9	2	0	1.7704	62.8093	68.16	73.4316

Using the Stack Preview screen, examine each stack and sort the stacks by cost, mean thickness, lead time for materials and the sigma functions. It will normally be most appropriate to choose the most cost effective or the most accurate stack, taking into account the material costs and availability, process costs, design parameters, etc.

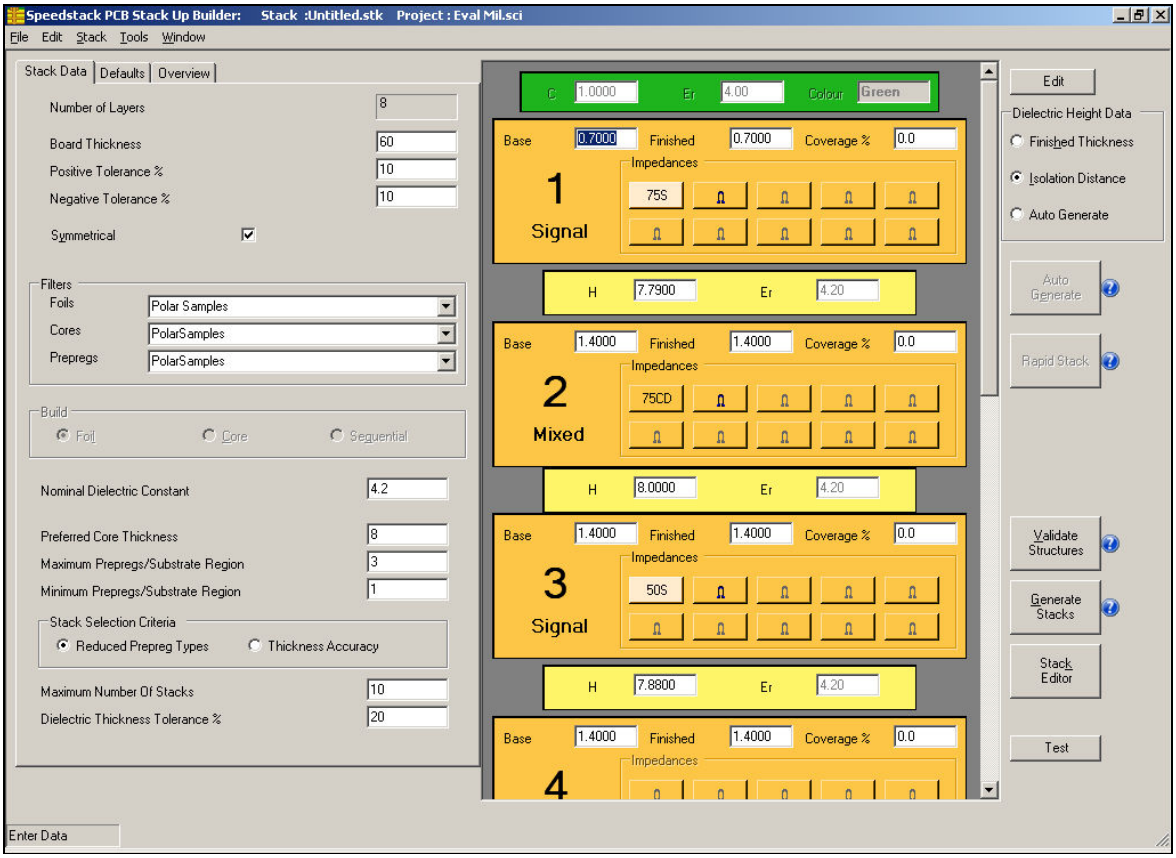
Click Retain original specified trace width, select the stack and click Apply. With the virtual stack chosen Speedstack will re-validate all impedance structures and open the Stack Editor window. See *Using the Speedstack Stackup Design System* for a detailed discussion of the Stack Editor.

Using the Speedstack Stackup Design System

The Speedstack Stackup Design System

Double-click the Speedstack icon to start the Speedstack program.

In installations with the Autostack (Virtual Stack Realization) feature activated Speedstack opens the Stack Definition screen; otherwise the Stack up Editor screen is displayed.



The Stack Definition screen

This section provides a brief introduction to the Autostack process. Detailed Speedstack definition training documentation is available from Polar Instruments.

Creating a new stack with Autostack

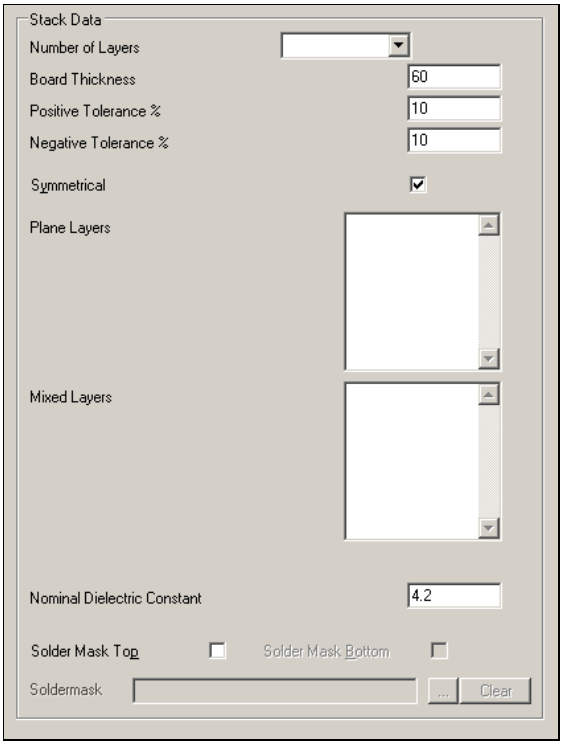
From the File menu select New to initiate a new stack. Most initial data are provided from the Configuration Options.

Stack data

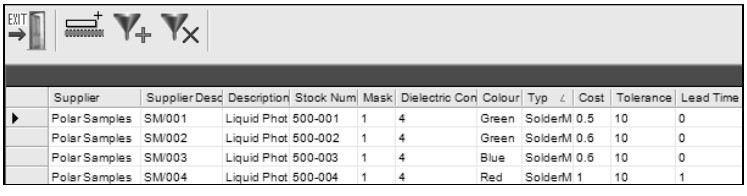
In the Stack Data section, select the required number of electrical layers and specify the board thickness and the dimension tolerances.

Specify the plane layers, mixed layers, dielectric constant (Er) and solder mask type.

If Symmetrical build is specified it will only be necessary to define the “top” half of the stack; Speedstack will reflect the supplied settings into the lower half of the stack.



If solder mask is to be used click the Solder Mask browse button to open the library at the Solder Mask database.



Supplier	Supplier Desc	Description	Stock Num	Mask	Dielectric Con	Colour	Typ	Cost	Tolerance	Lead Time
Polar Samples	SM/001	Liquid Phot	500-001	1	4	Green	SolderM	0.5	10	0
Polar Samples	SM/002	Liquid Phot	500-002	1	4	Green	SolderM	0.6	10	0
Polar Samples	SM/003	Liquid Phot	500-003	1	4	Blue	SolderM	0.6	10	0
Polar Samples	SM/004	Liquid Phot	500-004	1	4	Red	SolderM	1	10	1

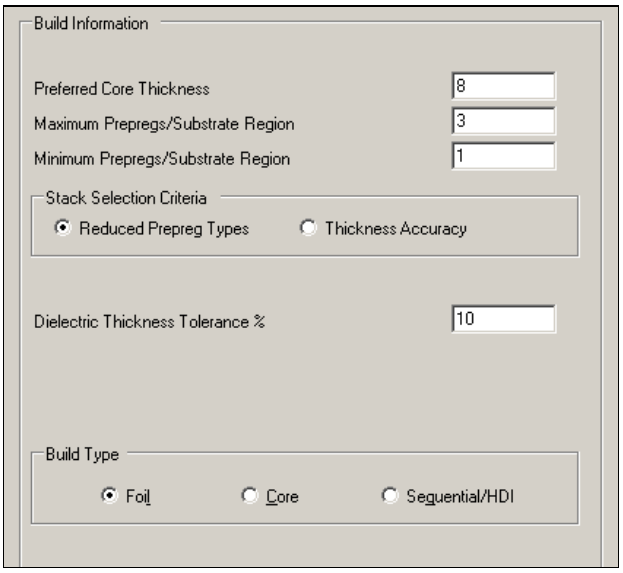
Select the mask and click the Add Material Above button; mask will be added to the top side (or both sides for a symmetrical build.)

Build Information

Use the Build Information section to refine the build parameters used by the Virtual Stack Realization engine.

Specify the preferred core thickness and the maximum and minimum numbers of prepregs per substrate; use the Stack Selection Criteria option box to direct the Autostack engine to design the stack for the lowest number of prepreg types or for accuracy of finished thickness.

Specify the tolerance for dielectric thickness and the build type (Foil, Core or Sequential build).

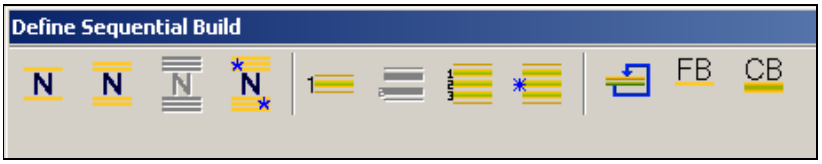


If required these defaults can be changed (for this project) on further pages. In addition, drills can be added or lamination and HDI sequences can be defined.

With the stack defined, for Foil or Core builds click Finish; all other parameters will be defined from the Tools/Options settings.

If Sequential/HDI is chosen via the Build Information screen click ‘Next’ to define the sequence.

Defining sequential builds



Sequential build toolbar

Type I stack

Type II stack

Type III stack

Set number of foils added to foil build

Foil build subsection with one core

Foil build subsection with two cores

Foil build subsection with three cores

Set number of cores in foil build subsection

Reset to foils and prepregs

Reset to foil build

Reset to core build

Upon first entry to the Define Sequential Build screen the stack view shows that the stack consists simply of foils and prepregs. The stack can then be defined as required.

Using the toolbar buttons shown above preset combinations can be defined.

Sequential build combinations

Name	Tooltip	Purpose
1N1	Type I	Makes foil build stack with 1 extra foil on either side
2N2	Type II	Makes foil build stack with 2 extra foil on either side
3N3	Type III	Makes foil build stack with 3 extra foil on either side
XNX	Set number of foils to be added to foil build	Makes foil build stack with X extra foil on either side
F1CF	Foil build sub-section with 1 core	Makes multiples of foil built sub-sections with 1 core in sub-section
F2CF	Foil build sub-section with 2 cores	Makes multiples of foil built sub-sections with 2 cores in sub-section
F3CF	Foil build sub-section with 3 cores	Makes multiples of foil built sub-sections with 3 cores in sub-section
FXCF	Foil build sub-section with X cores	Makes multiples of foil built sub-sections with X cores in sub-section
Reset	Reset to Foils and Prepregs	Makes stack simply of foils and prepregs probably as a start point for a more complex laminated stack
FB	Reset to Foil Build	Makes a foil build stack probably as a start point for a more complex laminated stack
CB	Reset to Core Build	Makes a core build stack probably as a start point for a more complex laminated stack

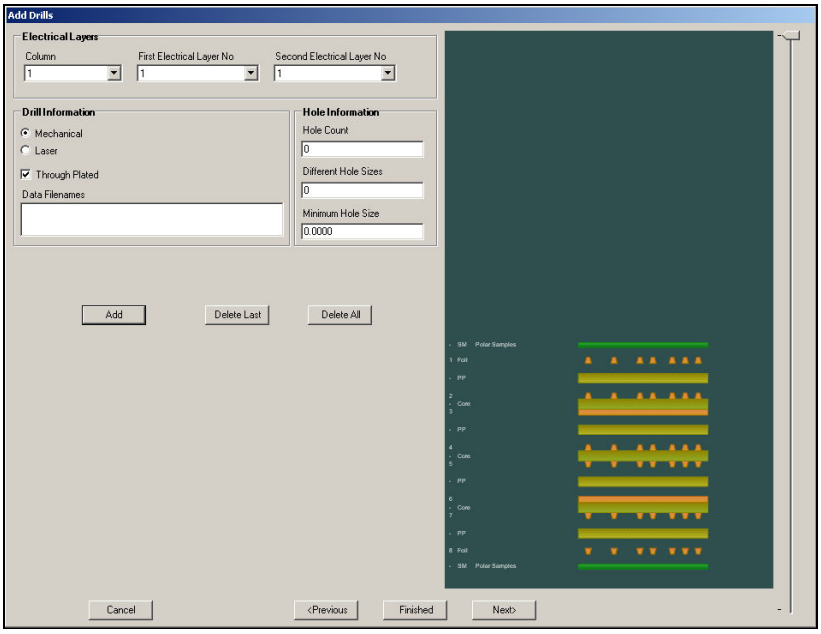
To produce non-standard sequences it is possible to start from any predefined sequence and by changing components, from combinations of foils and prepreg to cores and vice versa, any sequence can be defined (both practical and impractical.)

To select multiple components hold down the control key while left-clicking on materials.

Right click options

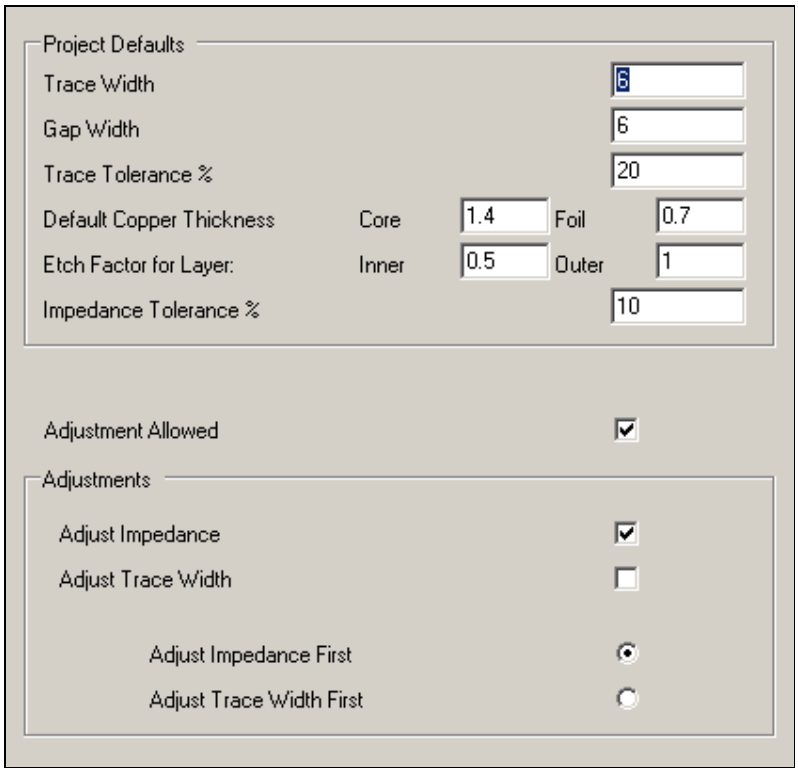
Right Click	Action
Single Foil	Mirror (invert) Foil
Single Prepreg	Nothing
Single Core	Convert to components, i.e. Cores and Prepreg
Two Cores with a prepreg sandwiched between	Convert to Core
N Materials	Copy block, this will copy a block of materials for pasting elsewhere in the stack. NB this will only copy the materials not copper layer types
Single Copper Material	Paste Block this will paste a block of materials in four different orientations

Adding drills



Drills are added in a similar manner to that below, see Core layer Information.

Project defaults



The Project Defaults screen allows the Tools/Options defaults to be overwritten *for the current project only*. It also allows for the setting of allowable adjustments to be made in the Automatic generation of stacks.

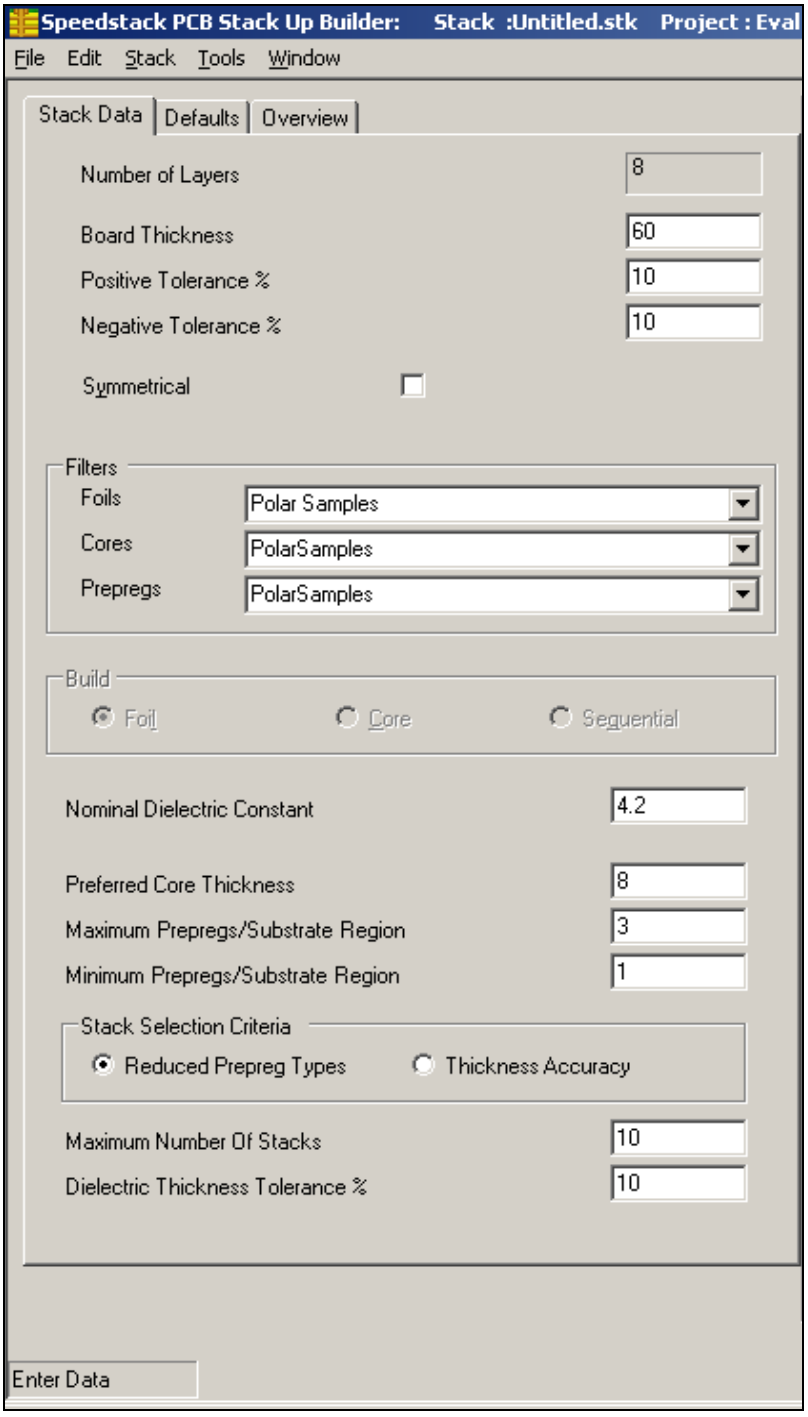
Allowing adjustments during goal seeking

When goal seeking takes place the initial goal seek is performed using the nominal values provided. Should that fail, the user may allow the target impedance and/or the nominal trace width to be varied in an attempt to find a solution.

The Adjustments Allowed check box enables the adjustments options: whether the target impedance and/or the trace width can be adjusted and, if both are allowed, which should be changed first.

When the Stack has been fully defined the screen returns to the Stack Definition Page.

Stack Definition page

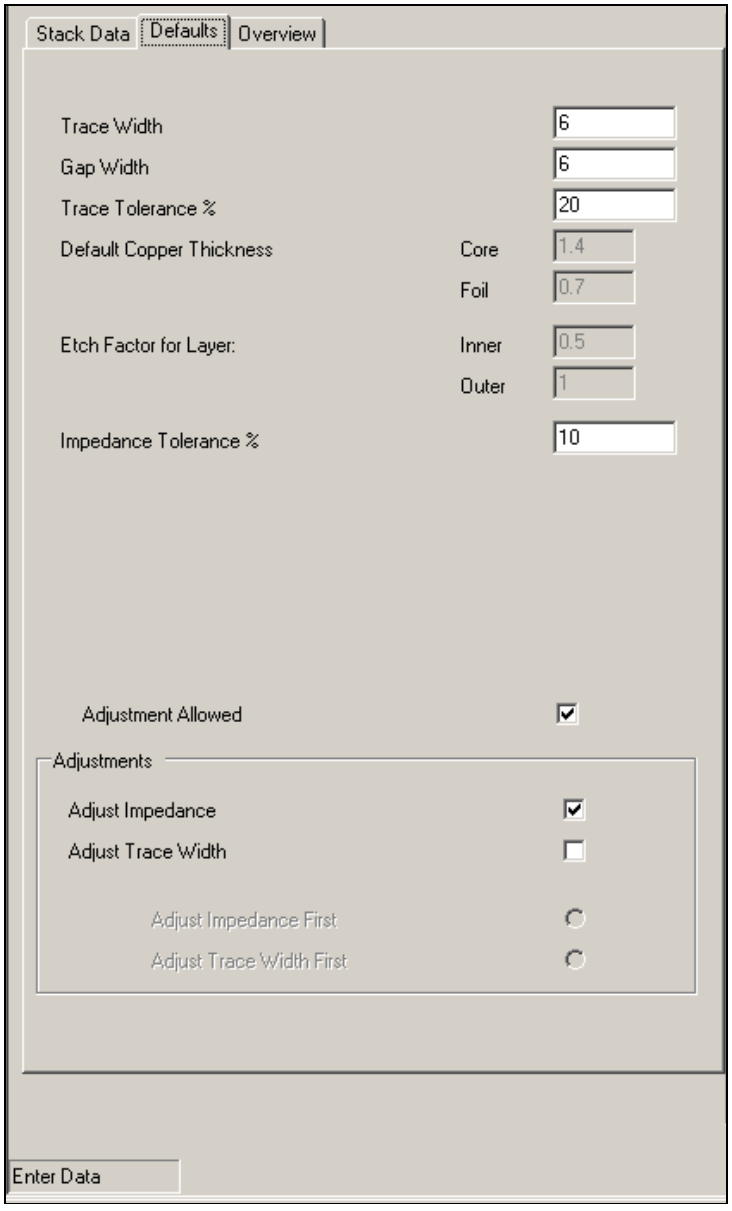


The left-hand side of the Stack Definition screen includes a series of tab-pages showing a summary of the data which has been selected. The screen also includes the means of selecting, via filters, the materials from the current library which are to be used. Many of the parameters provided in the definition stage can be amended.

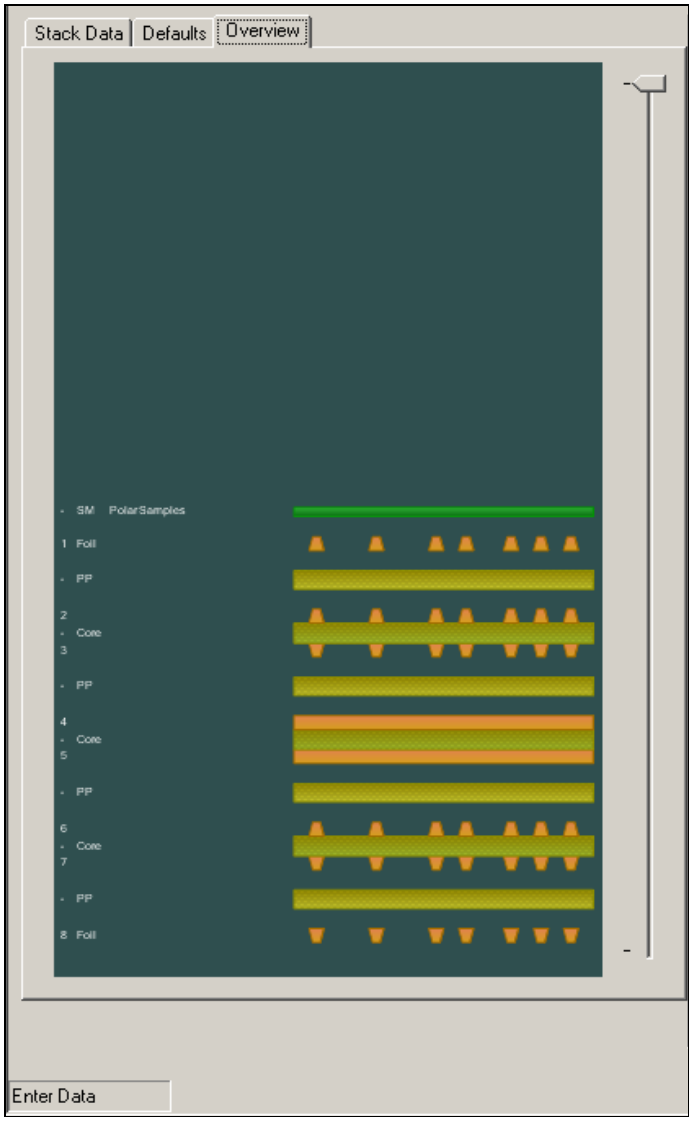
Filters

Where it is envisaged that a filter or set of filters will be used regularly then that/those filter(s) should be saved with the name “Default”. These will then be the default filters loaded on launch; they should be paired with the correct default library defined in the Tools/Options.

If a filter named “Default” is not available then the Filter with the name which occurs first in alphabetical order will be loaded on launch.



Stack Overview



Clicking on any material in the Overview screen will cause the stack representation to jump to that material, aiding the input of data on large layer count stacks.

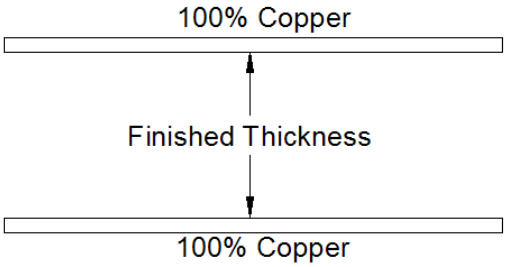
Speedstack will accommodate dielectric heights (H) calculated on the basis of *finished thickness* or *isolation distance*. H values are extracted from the stackup and used for calculating impedance (via the integrated Si8000 Controlled Impedance Quick Solver or Si9000 PCB Transmission Line Field Solver) in controlled impedance structures included in the stackup. H is the effective height of a dielectric substrate after the pressing of the stack.

The VSR engine will calculate for the minimum number of prepreg types (for ease of manufacture or minimum cost) or accuracy of board thickness at the user's option.

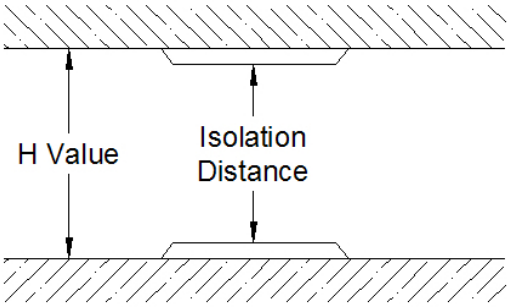
Specifying finished thickness

Finished thickness is the thickness of a prepreg after pressing between two solid sheets of copper, and should be defined in the materials library; it will be a lower value than the Base Thickness. Its value will be dependent upon the board shop's process parameters and is a critical dimension in many applications.

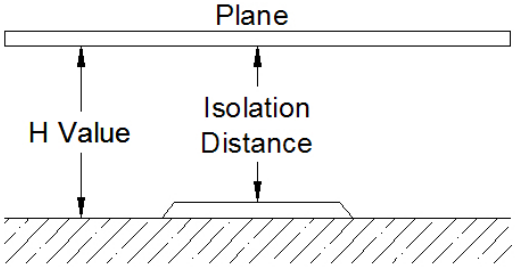
Speedstack keeps track of the finished thickness and tolerance, and allows fabricators to add in house post press thickness for prepreg layers, taking into account plating thickness where appropriate.



Copper may be embedded into the prepreg from either or both sides. Embedding copper in the prepreg reduces the thickness from the Finished Thickness. This reduced thickness is referred to as the Isolation Distance (see diagrams below).



Note: where more than one prepreg layer is involved the reduction is averaged across all the prepregs. A figure for Isolation Distance of less than zero implies an impossible build (i.e. the embedded copper totals more than the thickness of the prepreg).



The H Value is the sum of the isolation thickness and the full thickness of the adjacent copper(s). See Polar Instruments Application Note 507 for a discussion of calculating dielectric height with the Speedstack.

Adding controlled impedance structures

Apply the Stack Data and click on the Impedance buttons to add the controlled impedance structures for each layer, setting trace widths and H values if available. Up to ten structures may be specified for each layer; if the H values are unavailable then set for Autogenerate.

If a set of structures is required to be placed on more than one copper layer, define them on one layer, right click on that layer and select ‘Copy Structures’. Right click on the layer to receive these structures and select ‘Paste Structures’. Be aware that pasting structures will overwrite any existing structures on that layer, so define the common structures first then add any additional structures.

Critical structures

When defining structures for a layer a critical structure for that layer can be selected. This is the structure that will be the basis for all goal-seeking on that layer. The default critical structure is the one which has the widest trace width.

Validating structures

Click Validate Structures to validate each specified controlled impedance structure; valid structures may be unachievable with the current settings (H, trace widths, etc.); it may be necessary to return to the board designer to resolve. With all structures validated generate the stacks.

With all structures resolved the Speedstack will generate a series of stackups along with the associated costs.

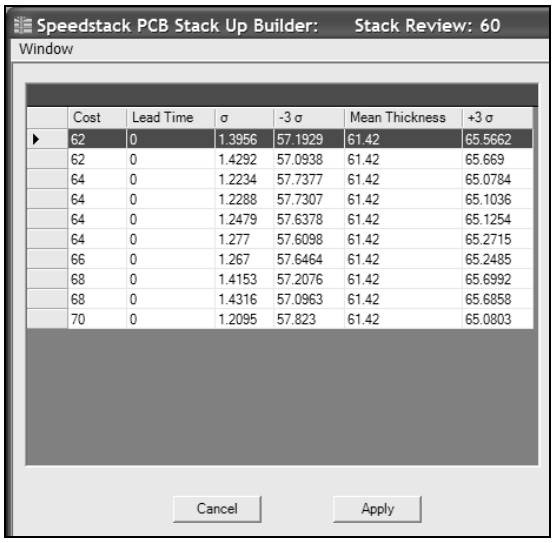
Reviewing the stack

Candidate stacks are displayed in the Stack Review screen (below). With the stacks generated, from the Stack Review screen specify the calculation method:

trim the trace widths to obtain the optimum impedance

calculate the impedances with the original trace widths

perform no impedance calculations.



The Stack Review screen

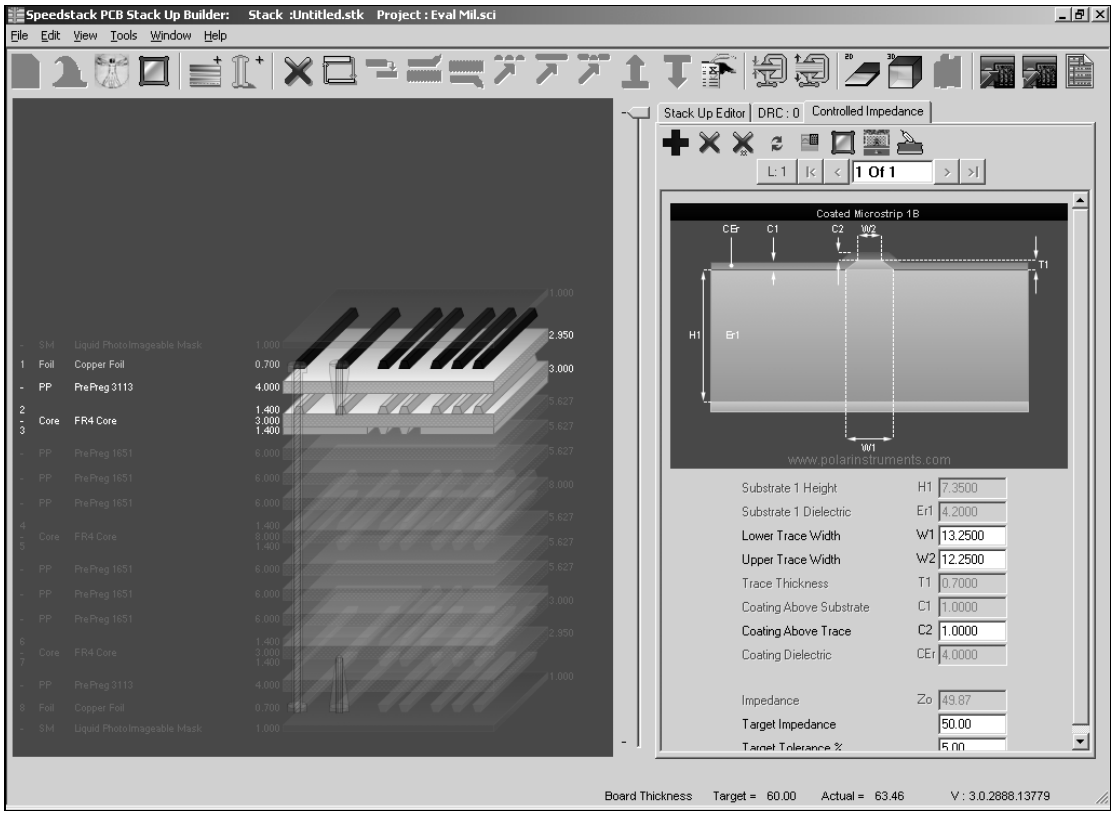
With the stacks displayed in the Stack Review screen, choose from the list of generated stacks and click Apply.

The completed stack will be transferred to the Speedstack Stackup Editor in asymmetrical mode.

Switch between the Speedstack screens, the Stack Definition screen, the Stack Review and the Stackup Editor screen using function keys, F10, F11 and F12.

Editing the stack

The completed stack may be edited in detail via the Stack Editor. The Stack Editor screen displays all details of the stack, including copper and prepreg materials, solder masks and ident layers, drilling information, controlled impedance structures and design rule check results. Controlled impedance structure data may be transferred between the Speedstack and the associated Polar field solver to goal seek for the target structure dimensions.



The Stack Editor screen

The Speedstack Stack up Editor screen comprises:

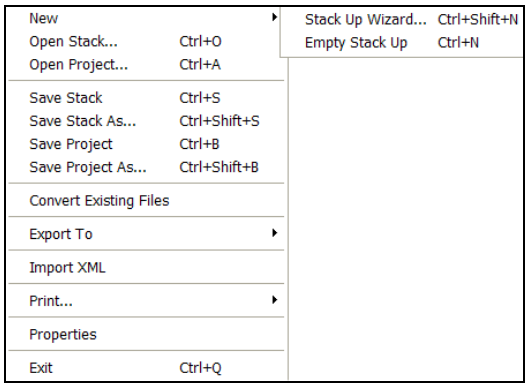
- The menu bar — drop-down menus containing all the Speedstack Editor commands
- The tool bar — incorporating short cut tool buttons to the most common menu commands
- The stackup build and construction window — where the board stack up is built and edited
- The Controlled Impedance window displaying the controlled impedance structures (if any) for the selected layer.
- Stack Up Editor/Notes tab— a free form text area for explanatory or commentary notes

- Design Rules Check (DRC) tab — allows design rules and manufacturing constraints to be specified and violations displayed
- Stack Up Information properties area — table containing information related to the whole stackup
- Selected Item Information area — properties table containing the attributes of the layer currently selected in the stackup

The Speedstack Menu System

The File menu

The File menu allows for creation of new stackups and projects and opening, saving, printing and converting existing stackups and projects.



Saving stackups

Click the Save button to save the stackup. Users are recommended to save the stackup frequently during the stackup creation process to avoid data loss; stackups are saved as .stk files, speedstack projects are saved as .ssd files.

Saving projects

Stackups that incorporate controlled impedance structures are saved as projects. Use the Save Projects command to save a stackup and its controlled impedance structures; projects are saved as .sci files.

Printing stackup information

To print the stackup information, choose the Print… command from the File menu.

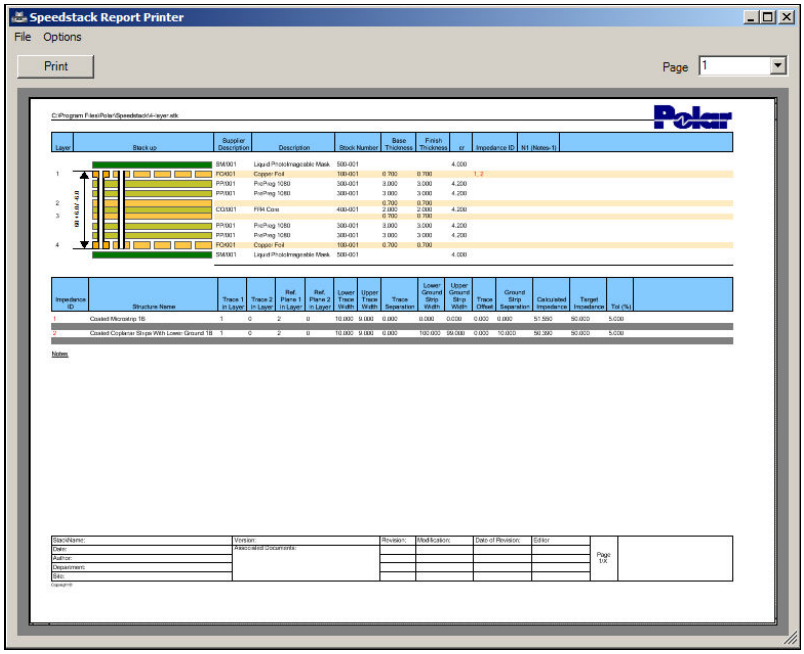
Select print options from the Print sub-menu:

Full Print includes the full stackup graphic (in either 2-D or 3-D aspect) with details of stackup layer materials and controlled impedance structures (dimensions, impedance, tolerance, etc.)
Summary report includes a 2-D diagram and details of materials in the stackup and controlled impedance structures
Print Technical Report A includes the Summary Report and information entered into the Stack File Properties.

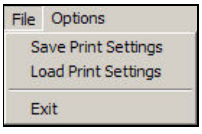
Print Technical Report B is a revised version of Technical Report A with options to print drilling and select data columns (see below).

Technical Report B

The Technical Report B print format provides options to customise the printout of the stackup and controlled impedance data. Select this print option under the File menu, the Printing window will appear showing a large preview of the printout.



Use the File menu under the Printing window to save and load print settings.



Whichever settings were last used in a session will become the default when the Printing window is next loaded.

The options menu contains all the settings for printing.

- Page Setup: standard page setup dialog to change paper sizes, printer (hardware) settings and margins.
- Stack Data Columns: select, combine and order the data columns available for the stack as desired.
- Font Size: a range of fonts sizes to print at.
- Margin Guides: Toggles on and off a boundary marking the margins of the page.
- Colors: Allows for the colors of printable items to be customised.
- Note Field Aliases: allows for the 5 free-text note fields (under material properties and material library) to be given a descriptive name when printing.
- Print Order: toggles the ordering of the Stackup notes and the Controlled Impedance table.
- Polar Logo: toggles on and off the Polar Instruments logo.
- User Logo: toggles on and off the user-defined logo (as set in the application configuration).
- File Path: toggles on and off the file path/file name
- Drills: toggles the drilling on and off
- Copyright: toggles on and off the copyright information
- Data Number Format: sets the precision of numeric data in the printout.
- Board Thickness Value: sets the board thickness value to either Percentage or Absolute/Actual.
- Restore Default Settings: resets settings to the default
- Data Alignment: specifies alignment (left, centre, etc.) for stack and impedance data

Assigning properties to projects and stackups

The stack file Properties dialog may be displayed automatically each time a new stackup is created (see Tools|Options|General) and provides a range of text fields for descriptive information, e.g. stackup author, company name, file create date, stackup name, version, etc.

From the File menu choose the Properties command to add descriptive text fields — information contained in the Properties dialog will be displayed on stackup printouts.

To display the Properties dialog each time a new stackup or project is created, from the Tools menu choose Options and click the check box below on the General tab

Exporting stackup information

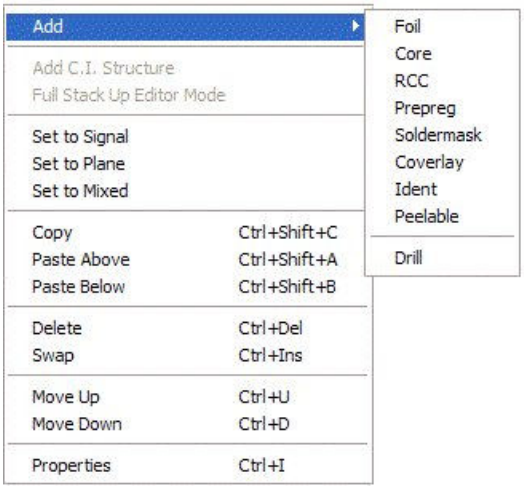
Speedstack incorporates the facility to export printed output in XML, Gerber, DXF, CSV as well as graphic image formats.

From the File menu choose the Export To command and choose the format from the Export To sub-menu.

Backing up stackups and libraries

It is strongly recommended that stackup files (assigned the .stk extension), project files (assigned the .sci extension) and library files (assigned the .mlbx extension) be backed up to a secure location.

The Edit menu



The Edit menu contains the commands necessary to create and modify board stack ups. The designer or fabricator works within the free-form stackup build and construction window and adds layers of core, prepreg, foil, etc., from the materials library. The items that can be edited depend upon whether the Stack Up Editor or Controlled Impedance tab is selected.

Layers can be changed to signal, plane or mixed, moved up or down or copied and pasted, or assigned properties as required.

The Speedstack will apply design rules to the finished stackup to ensure compliance with good board design, (for example, the Speedstack will check for symmetrical layers, misplaced layer types, adjacent copper layers, etc.)

The View menu

The View menu allows the Speedstack to display the stackup in a 2-dimensional or 3-dimensional aspect.

The Speedstack toolbar

The Speedstack toolbar comprises shortcut links to the most popular commands.

Note: the toolbar buttons will activate/deactivate to allow stack editing or controlled impedance calculations. Pause the mouse over each tool button to display the tool's screen tip

File operations

 Create new stackup

 Stackup Wizard

Stack Building Operations

 Symmetrical Mode

 Mirroring Mode

 Add layer to the stackup

Click to select the layer type. The list of layer types is displayed in the associated sub-menu.

Layers available include:

Foil…	Add foil layer to the stackup
Core…	Add core layer
Prepreg…	Add prepreg layer
RCC…	Add resin coated copper layer
Soldermask…	Add solder mask
Coverlay…	Add Coverlay layer
Ident…	Add screened ident layer
Peelable…	Add peelable mask

 Add mechanical/laser drill between layers

Editing the stackup

 Delete selected stackup layer or drill

 Swap selected material

 Copy material of the selected layer

 Paste material above selected layer

 Paste material below selected layer

 Set the selected electrical layer as a signal layer

 Set the selected electrical layer as a plane

 Set the selected electrical layer as a mixed signal/plane layer

 Move selected layer up one layer

 Move selected layer down one layer

 Display properties dialog for the selected layer or drill

 Apply Finished Thickness

 Reset Finished Thickness

Changing the stackup view


Display 2-dimensional view


Display 3-dimensional view

Managing the materials library


Display materials library

Exchanging data with the Si8000 or Si9000 Field solver


Copy controlled impedance data to Field Solver


Paste Controlled Impedance Data From Field Solver


Re-engineer Current Stack

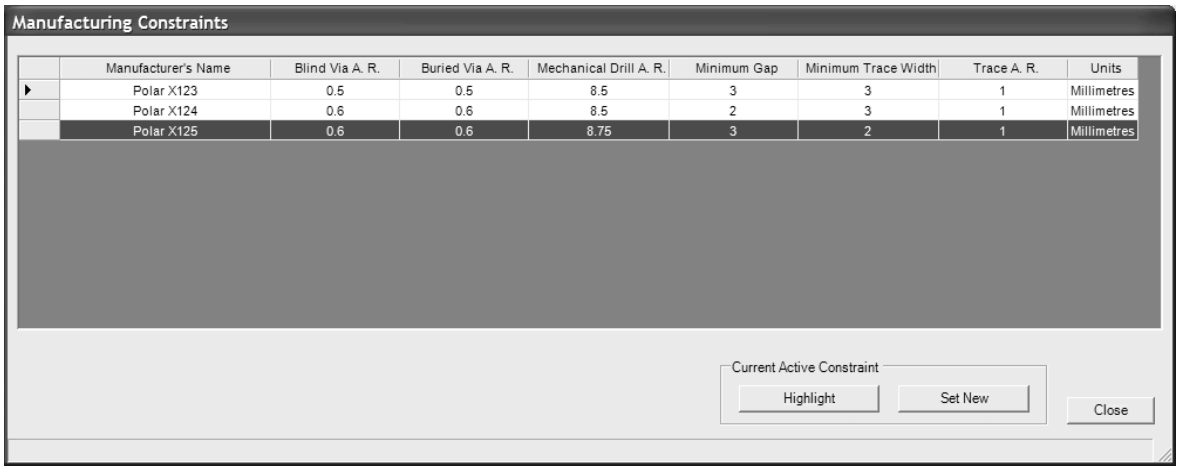
Configuring the Speedstack

When first run, the Speedstack environment is initialised to its factory settings. These may require adjustment before outputting a finished stackup and/or project. Default settings are changed using Tools|Options, Tools|Manufacturing Constraints and Tool|Edit Thickness Options.

Manufacturing Constraints

The Manufacturing Constraints options consist of a collection of manufacturing capabilities, minimum gaps and trace widths, buried and blind via and trace aspect ratios, drill aspect ratios, etc. that can be applied during design rule checking (see figure below).

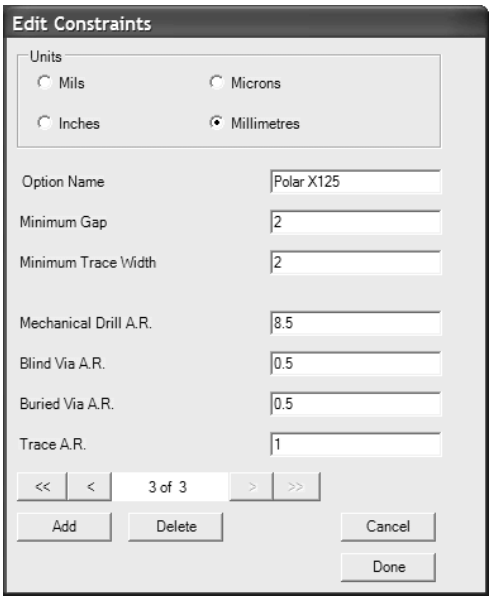
They will normally refer to differing levels of technology offered by one or more PCB manufacturers for a range of prices. The required information (shown in the example below) can normally be obtained from the manufacturer.



Click the Highlight button to highlight the current active constraint; to apply a new constraint select the constraint row and click Set New.

Editing and adding constraints

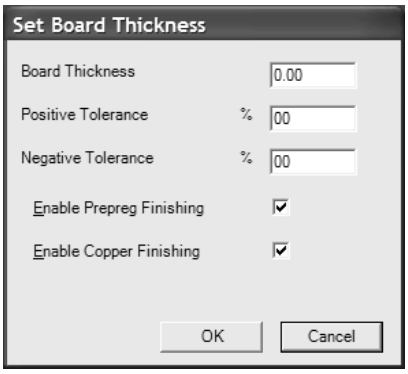
To modify a constraint or add a new constraint, double click within the constraint row to be edited.



Modify each setting as required; click Done to confirm the settings and close the dialog.

To add a new constraint click the Add button, fill in the settings fields and click Done to finish. The new constraint will be added to the table of current constraints. Click the Delete button to remove the constraint from the list.

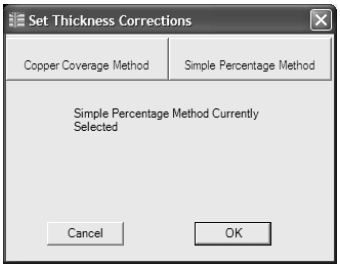
Setting the board thickness



Uncheck Enable Finishing options to allow the finished thickness to be modified via the layer Properties dialogs (the Apply and Reset Finishing buttons are disabled).

Thickness Options

From the Tools menu choose the Edit Thickness Options command to display Set Thickness Corrections dialog. Speedstack offers two methods: Simple Percentage Method and Copper Coverage Method

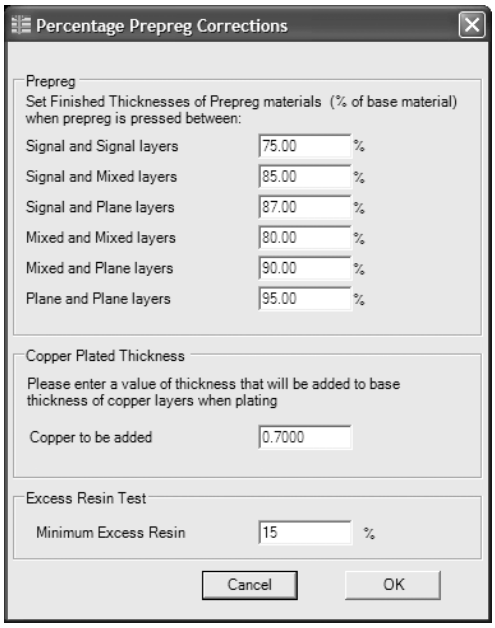


Each method requires that the amount of copper to be added where plating is required be set. In addition, where the Excess Resin design rule check is used the minimum acceptable value must be set.

Simple Percentage Method

The Simple Percentage Method allows the user to set the percentage of Prepreg base height, which will be used to determine the Isolation Distance. The percentage is set for each electrical layer type pair.

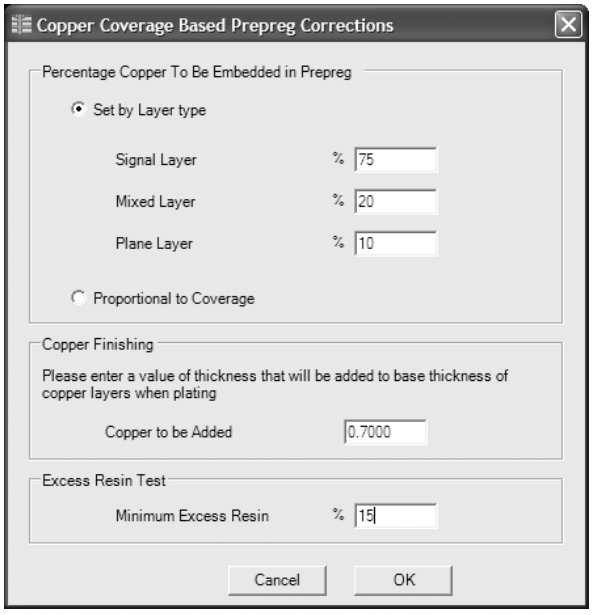
- Signal – Signal
- Signal – Mixed
- Signal – Plane
- Mixed – Mixed
- Mixed – Plane
- Plane – Plane



Copper Coverage method

The Copper Coverage method allows the user to set the amount of copper that will be embedded into the Prepreg.

This can be set as a single value for each electrical layer type. Alternatively the amount of copper embedded will be calculated on an electrical layer by layer basis dependent upon the copper coverage for the layer set in the properties window. The greater the copper coverage the smaller the amount of copper that is embedded.



Note: The two methods of finishing are not compatible with each other. The Copper Coverage method requires that the finished thickness of prepregs be entered in the library; that

value stays locked in the stack unless the Simple Percentage method is set up; if Reset Finishing is then clicked the finished thickness reverts to the base thickness.

Environment and default settings

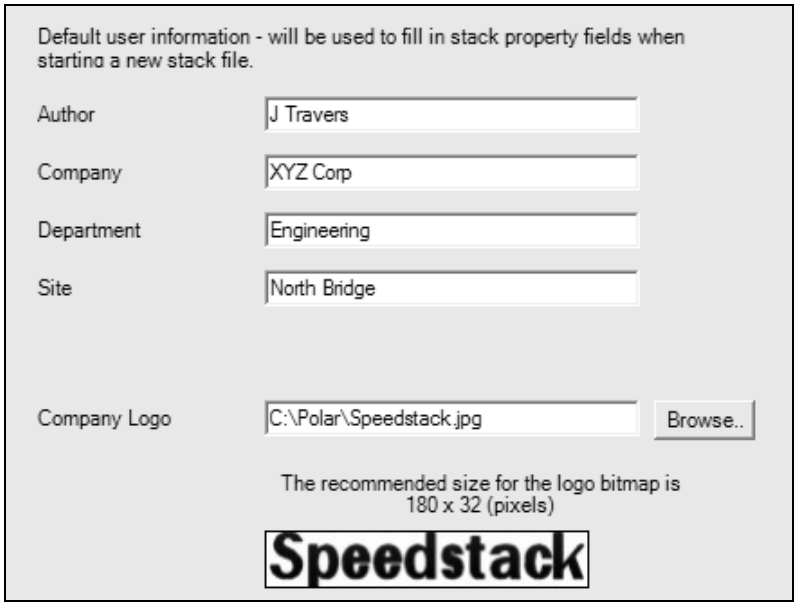
From the Tools menu choose the Options command to display the Configurations Options dialog.

Setting user defaults

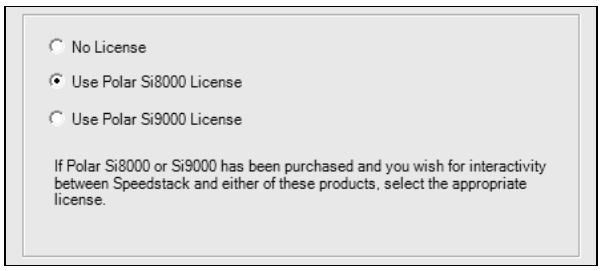
Information added to the User tab will be transferred to the File Properties dialog and used on printouts

Click the User tab

Enter information as appropriate into the associated text fields; optionally, select a graphic for use as the company logo — optimum graphic size is 180 x 32 pixels — the graphic is printed in the preview box.



Controlled impedance calculations

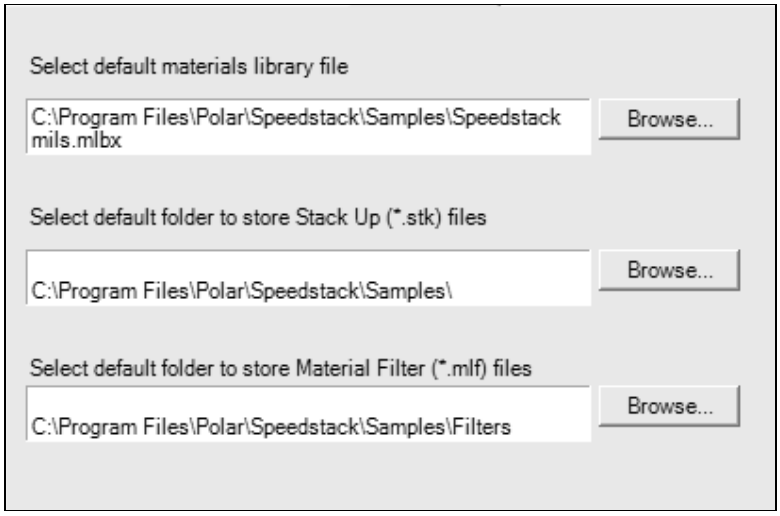


To activate the Speedstack controlled impedance function, ensure that the Si8000 or Si9000 is installed; from the Licencing tab choose either Use Polar Si8000 License or Use Polar Si9000 License option as appropriate.

Choosing default file locations

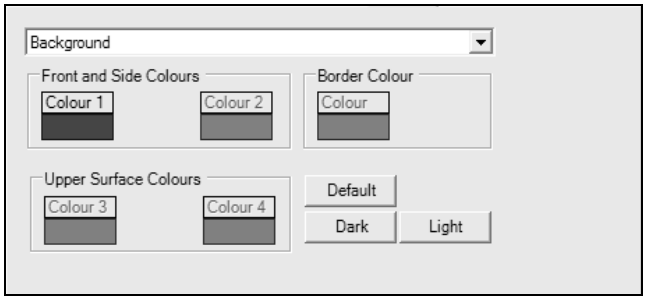
Users can choose which materials library the Speedstack uses at start-up. Click the File Locations tab and use the Browse button to navigate to the library (.mlbx) file.

The File Locations tab provides for default locations for stackup or project files and Material Filter (.mlf) files. Browse to the target folders and click OK to confirm (create new folders if necessary).



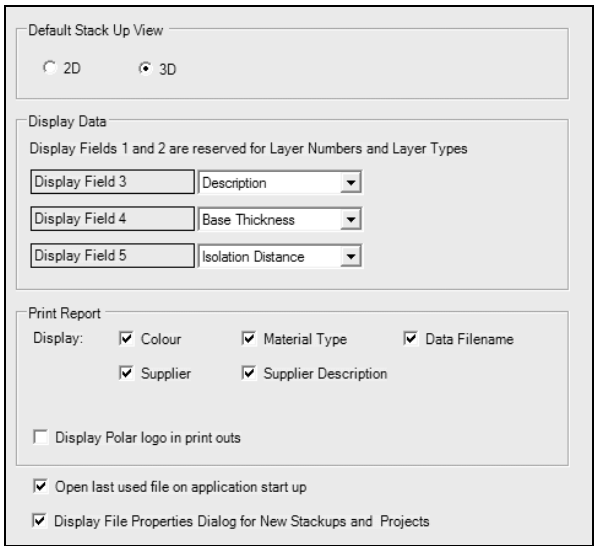
Choosing background and stackup layer colours

Choose the Colours tab to change stackup component colours from their factory defaults.



Specifying the default view and opening file

Select the General tab to specify the Default Stackup View (two or three-dimensional).



From the Display Data section select which data to display alongside the stackup; from the Print Report section select which data to display in the printout, click the Open last used… check box to specify that Speedstack should open the last used file on start-up.

Clicking the Display File Properties Dialog… will display the File Properties Dialog each time a new stackup or project is initiated.

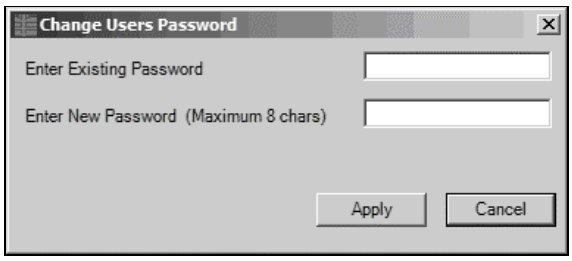
Security — setting passwords

The Speedstack security system provides for multi-level password protection. If a User password is defined, it will be requested each time the Speedstack is started. Setting an Administrator password will prevent unauthorised changes to the Speedstack configuration. Select the Passwords tab, and then Log In.

Default Passwords are blank for both the User and the Administrator. With blank passwords the password protection is transparent, and no protection is provided.

Click Set New Password.

Chose whether it is the User password or the Administrator password that is to be changed.



Enter the existing Password; this will be validated when moving to the Enter New Password text box. If the password is incorrect the focus will not leave the “Enter Password” text box.

Enter the new password then retype it in the Confirmation text box that will appear. The two passwords will be compared and if different will enforce password re-entry.

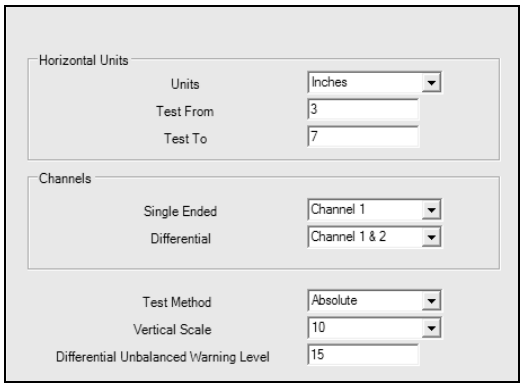
Note: the new Users password will not be applicable until the program is re-started.

The Administrator’s password will be requested each time the Configuration Options are opened.

Specifying default CITS test file parameters

The Speedstack allows the user to generate a CITS test file for each controlled impedance structure within the stack. Each test file contains the test parameters (test units, distance, number of channels, etc.) to be used when testing the stack’s controlled impedance structures using a Polar CITS (Controlled Impedance Test System).

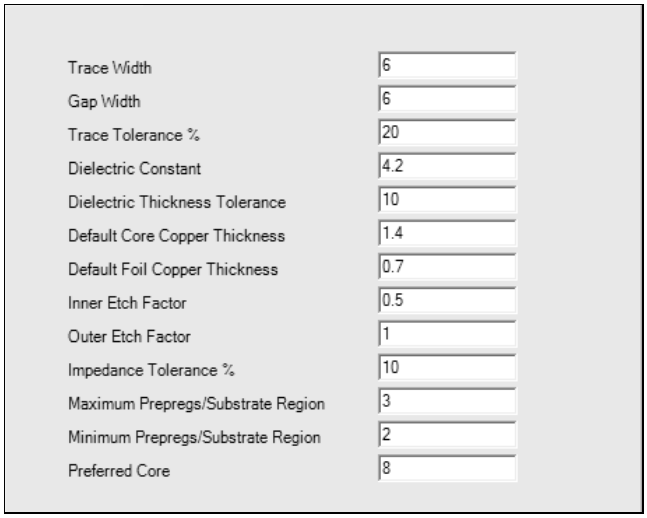
Select the CITS Test tab to specify the default test parameters to be used when initiating a CITS test file.



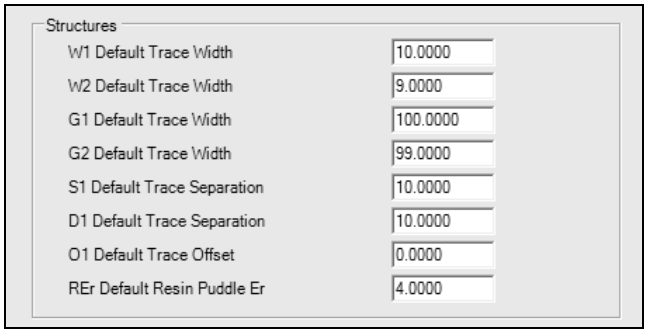
The test file may be edited via the Edit Test Data dialog.

Specifying default Autostack settings

The Autostack options will be used as starting values for the Stack Definition window when creating a new stack. They will typically be obtained from the manufacturer's material library.

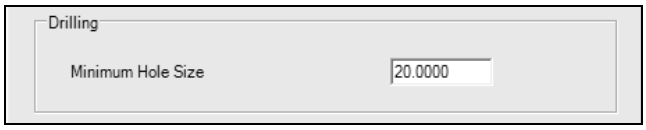


Specifying default trace parameters



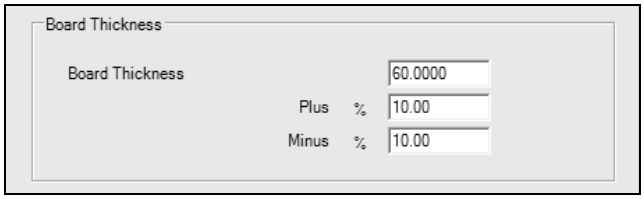
When adding a new structure default values are entered for the trace widths and separations. These values are set under the 'Defaults' tab

Specifying minimum drill hole size



In the Drilling section set the default value for the minimum drill hole size.

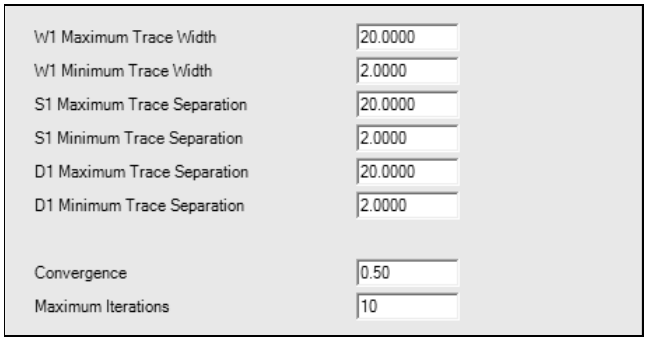
Specifying default board thickness



In the Board Thickness section set the default values for board thickness and tolerances.

Specifying Goal Seeking Parameters

Click the Goal Seeking tab to specify the defaults for trace widths and separations used during goal seeking.



During goal seeking the calculated value for impedance will progressively converge upon the target value. In the Convergence text box specify the difference between the target impedance and the actual impedance at which goal seeking will terminate.

Use the Maximum Iterations text box to limit the number of iterations used during goal seeking.

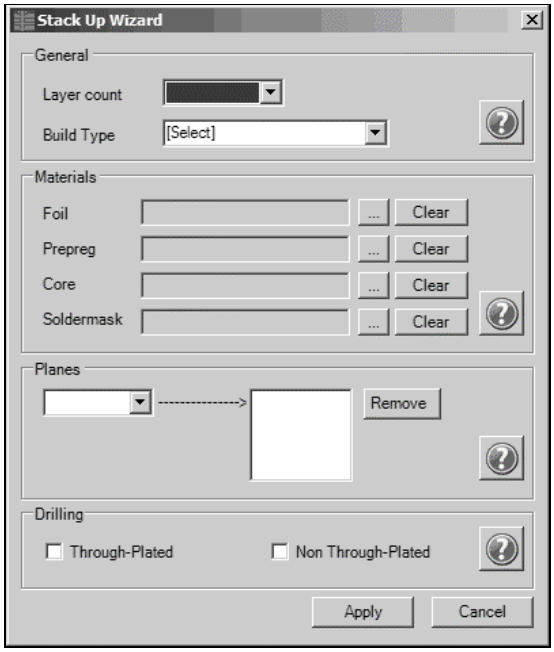
Creating and editing stackups

Stackups may be created manually using the Stackup Wizard or using the editing window.

Using the Stackup Wizard

Stackup wizard button

The Stackup Wizard guides the user through the process of creating complex stackups in only a few steps. Click the Stackup Wizard button or choose Stackup Wizard from the File|New sub menu. The stackup editing window is cleared and the Stackup Wizard displayed.



Using the Wizard the user can specify the layer count and build type, stackup materials, planes and drill types in a single operation.

Electrical layer count

Begin by specifying the electrical layer count — up to 64 electrical layers may be specified. Choose the number of layers from the drop down list box.

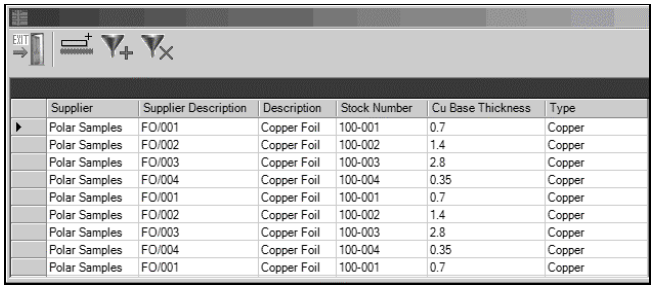
Build type

Choose the build type (Foil or Core) from the drop down list box. Core builds contain only core materials; most builds will be foil builds — containing internal layers of cores with two outer foils.

Choosing stackup materials

Note; if Core build type has been specified the Foil material control will be disabled.

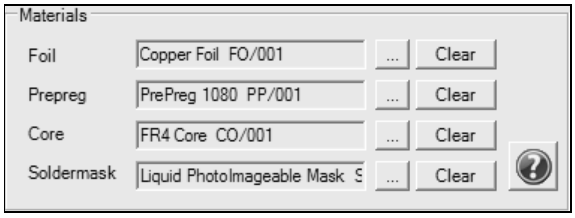
To include a foil layer click the Foil Add Material button; the library of foil materials is displayed. Choose the foil material from the list of materials available and click the Select Highlighted Material button; the material is added as a foil layer to the stackup.



Supplier	Supplier Description	Description	Stock Number	Cu Base Thickness	Type
Polar Samples	FO/001	Copper Foil	100-001	0.7	Copper
Polar Samples	FO/002	Copper Foil	100-002	1.4	Copper
Polar Samples	FO/003	Copper Foil	100-003	2.8	Copper
Polar Samples	FO/004	Copper Foil	100-004	0.35	Copper
Polar Samples	FO/001	Copper Foil	100-001	0.7	Copper
Polar Samples	FO/002	Copper Foil	100-002	1.4	Copper
Polar Samples	FO/003	Copper Foil	100-003	2.8	Copper
Polar Samples	FO/004	Copper Foil	100-004	0.35	Copper
Polar Samples	FO/001	Copper Foil	100-001	0.7	Copper

Repeat the procedure for prepreg and core materials and the (optional) solder mask layers.

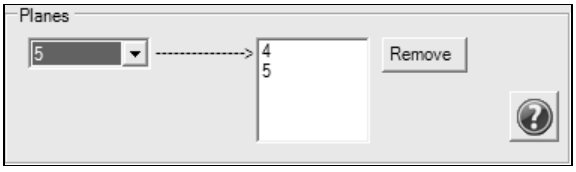
Use the Clear button to remove a layer from the stackup.



Stackup materials selected

Nominating power planes

Use the drop down list box to specify that a plane should be a power plane. Select all planes as required. To remove a power plane from the list select the plane number from the list and click Remove.



Layers 4 and 5 specified as power planes

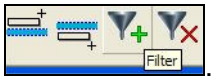
Adding drill information

To add a drill information between electrical layer 1 and the last layer click the Through-Plated and Non-Through-Plated check boxes as required.

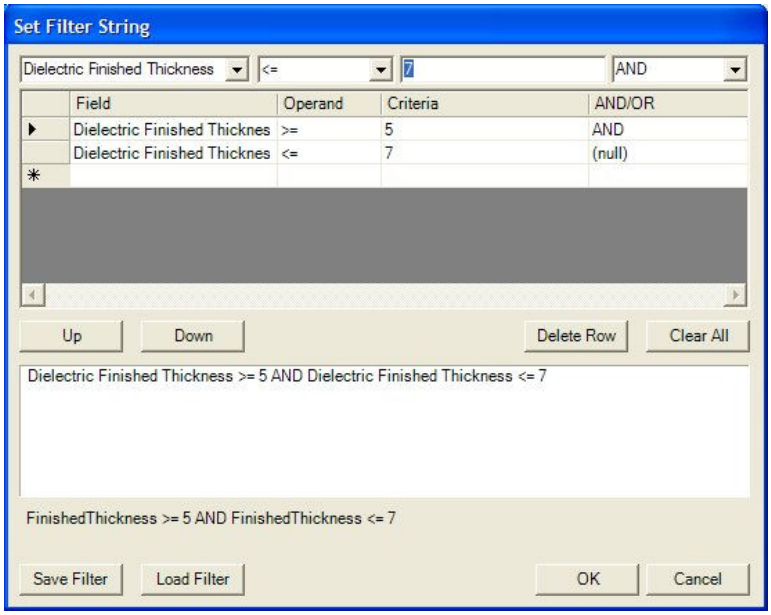
With all build options specified click Apply to complete the stackup. The finished stackup appears in the stackup window.

Filtering Materials

When using the Stack Wizard, adding or swapping materials, available materials (Foils, Prepregs, etc.) are listed in the associated material library dialog. Lists can be filtered for materials matching desired parameters (dielectric thickness, Er, etc.)



In the library window click the 'Filter' button to display the Set Filter String dialog.



Filter strings can be created and saved for future use. To recall an existing filter click the Load Filter button, choose the filter file and click OK.

Building the filter string

Build the filter string by selecting parameters, operands and criteria from the drop-down boxes. If the AND/OR box is selected another row is automatically added to the grid. The filter language is a sub-set of common database commands.

Use the Up/Down buttons to select a row for deletion. The arrowhead at the side of the grid indicates the selected row.

Click OK to apply the filter immediately to the selected library. If desired, save the filter string for future use. (The

Speedstack provides for interaction between the library dialog and filter form. This allows complex strings to be built line-by-line and tested without saving until the string is completed.)

When saving the filter choose a descriptive name for the file that reflects the purpose of the filter. The Speedstack automatically names the files for the material type.

Using the Like operator

Use the Like operator to filter results via wild card characters. The characters * and % can be used to represent groups of starting or ending characters.

For example, specifying Like 'Po%' or 'Po*' as the criterion for the Suppliers field will show all suppliers beginning with 'Po'.

Similarly, specifying Like '%es' or '*es' as the criterion for the Suppliers field will show all suppliers ending with 'es'.

Click the Clear Filter button to display all materials of the selected type.

Creating stackups manually

The Speedstack allows the designer to add or edit stackup layers in any order, from top to bottom, bottom to top or from the centre layer outwards. In this example we create a four-layer stackup, starting at the centre core layer and adding layers above and below.

Adding layers to the stackup

Display materials library

Items added to the stackup are added from the currently open materials library. The Speedstack opens Program Files\Polar\Speedstack\default.mlb if it exists; if a different library is required, open it via the Materials Library command.

Note: the Speedstack does not ship with the default.mlb library. For this discussion open one of the two sample library files, Speedstack inch.mlb or Speedstack mm.mlb (stored in the Program Files\Polar\Speedstack\Samples folder at installation time for a default installation.)

Caution: Consistency of units

When defining dimensions for a stackup (for example, layer thicknesses) ensure that all measurements are defined using the same units (mils, mm, etc.) throughout the structure and its libraries.

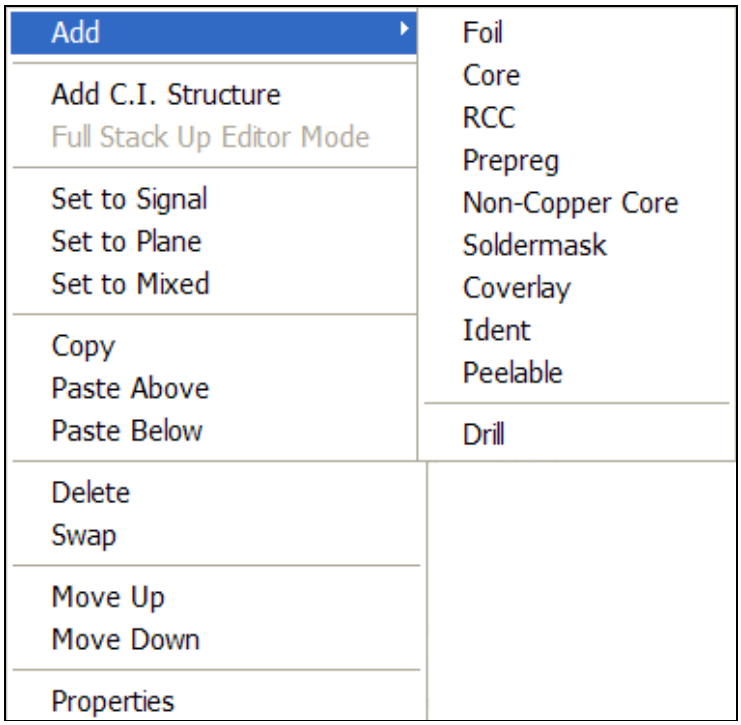
Note: the libraries supplied for these examples are preloaded with sample data only.

Click the File|New command to clear the stackup screen and notes and information text areas.

Click the File|Save Stackup or Save Project command to save the stackup or project. Users are recommended to save stackups or projects frequently during the stackup creation process to avoid data loss. Stackup files (.stk), project files (.sci) and library files (.mlb) should be backed up to a secure location.

Editing the stack

When editing the stack it will probably be most convenient to right click an object in the stack and select the associated command from the context menu. The menu will reflect the commands available for the selected object — commands that are not appropriate for the object are greyed out.



Alternatively, select the object (copper, prepreg, core, etc.) with the left mouse button and choose the command from the Speedstack toolbar.

Adding a core layer

Click the Add Layer Material button and choose Core…the Core library is displayed

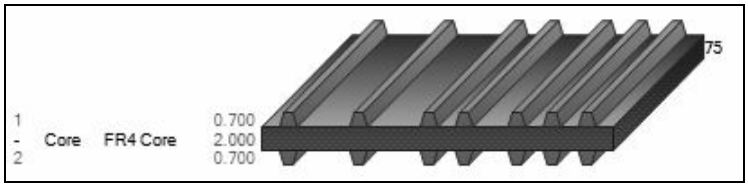
The Core library contains full details of the core material, including base and finished thicknesses, dielectric constant, and upper and lower copper thicknesses.

Base Thickness	Finished Thickness	Dielectric Constant	Upper Cu Thickness	Lower Cu Thickness
0.05	0.05	4.2	0.018	0.018
0.05	0.05	4.2	0.035	0.035
0.05	0.05	4.2	0.07	0.07

Click on the column button to sort the library list by the selected column.

Choose a core type from the list of cores and click the Add Above button

Add core above selected layer. The core is added to the stackup screen.



Stackup core layer

Layers may also be added below the selected layer.

Add core below selected layer

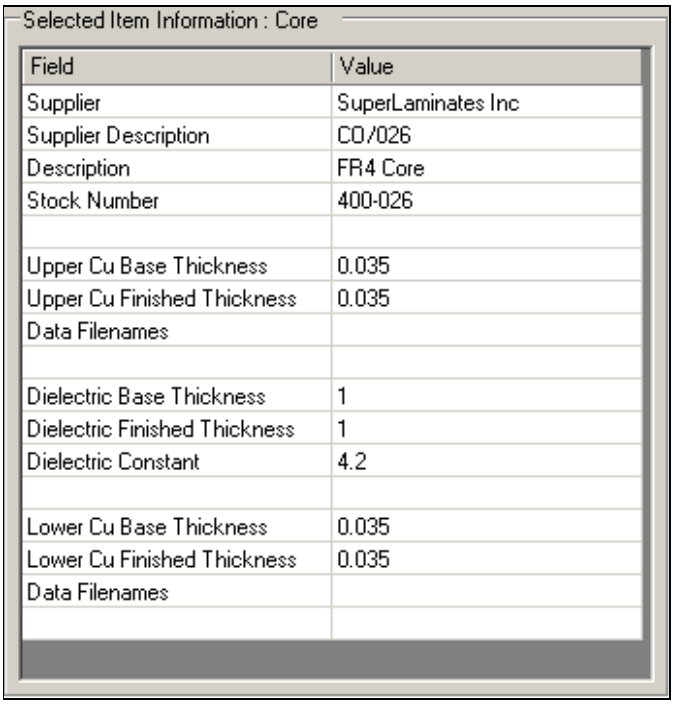
As each layer is added the stackup information table is updated to reflect the current status of the stackup.

Stack Up Information

Field	Value
Electrical Layer Count	2
Stack Up Thickness	1.0700
Dielectric Thickness	1.0000
Copper Thickness	0.0700

Stackup information table

With the core selected, the Selected Item table displays the properties of the core.



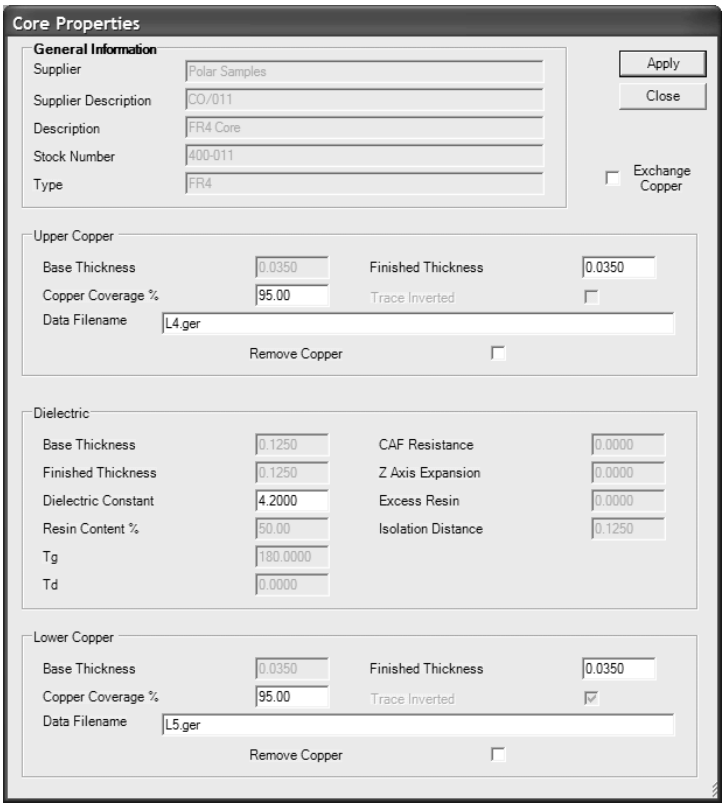
Core layer information

Editing the selected layer properties

To change the properties of the selected object (for example, to modify the dielectric constant or the value for the finished thickness of the dielectric), right click the object in the stackup and choose Properties from the shortcut menu; in this example the Core Properties dialog is displayed.

(Note that the Enable Finishing setting in the Tools|Set Board Thickness dialog must be unchecked to enable Finished Thickness to be specified manually.)

Change the value for Dielectric Constant or Finished Thickness to the corrected value and click Apply.



Adding data file names

If available, add the data file name(s) to the upper and lower copper layers and click Apply.

Close the dialog when all changes are completed.

Changes will be reflected in the Stackup Information table

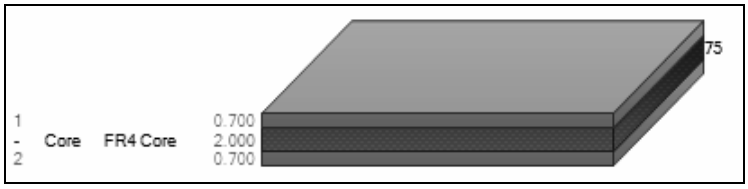
Changing a layer function

In this example we change both signal layers above and below the core dielectric to planes.

Set Layer Plane

Click the lower signal layer and click the Set Layer Plane button. Repeat for the upper signal layer.

The changes are reflected in the stackup window



Exchanging layers

Library Swap button

To change just the core dielectric (leaving the copper layers unaffected), right click the core material (for example the FR4 in the graphic above) and choose Swap from the context menu or left click the core material and click the Swap Selected Material button. Choose the new core type from the

library and click the Swap button. The layer properties will change to reflect the new material and changes appear in the Stackup Information table.

Adding Prepreg layers

Add Layer Material button

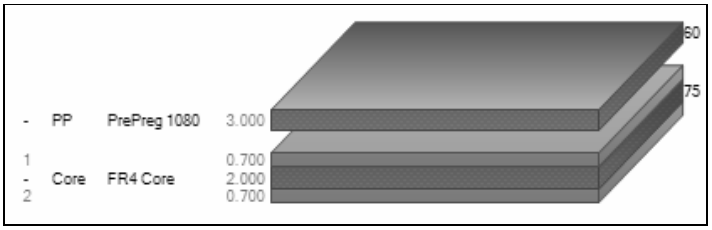
With the core selected, click the Add Layer Material button and choose Prepreg…; the Add Prepreg library is displayed.

Description	Stock Number	Base Thickness	Finished Thickness	Dielectric Constant
PrePreg 1080	300-001	0.075	0.075	4.2
PrePreg 3080	300-002	0.077	0.077	4.2
PrePreg 3113	300-003	0.102	0.102	4.2
PrePreg 1651	300-004	0.152	0.152	4.2
PrePreg 7628	300-005	0.2	0.2	4.2

The Prepreg library contains details of the Prepreg material, including the Prepreg's base and finished thickness and dielectric constant.

Add Prepreg Above

Choose the Prepreg material from the database and click the Add Prepreg Above button.



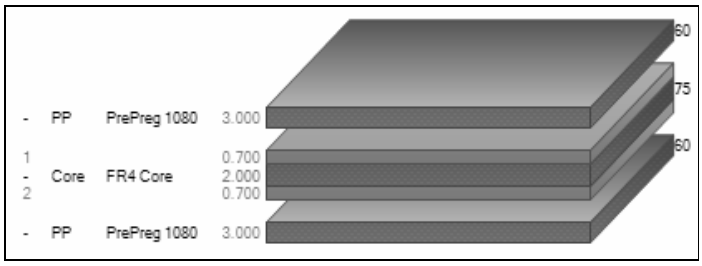
The Prepreg layer is added above the core.

To change the properties of the Prepreg material right- click the layer and choose Properties from the short cut menu. For example, the value for Finished Thickness can be modified to reflect the effects of the pressing process.

Add Prepreg Below

Click the Add Prepreg button to display the Add Prepreg library and click the Add Below button

The layer of Prepreg is added below the core.



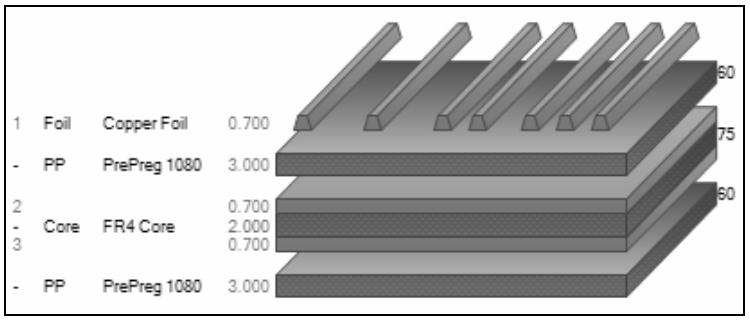
Modify the properties as necessary.

Adding a foil layer

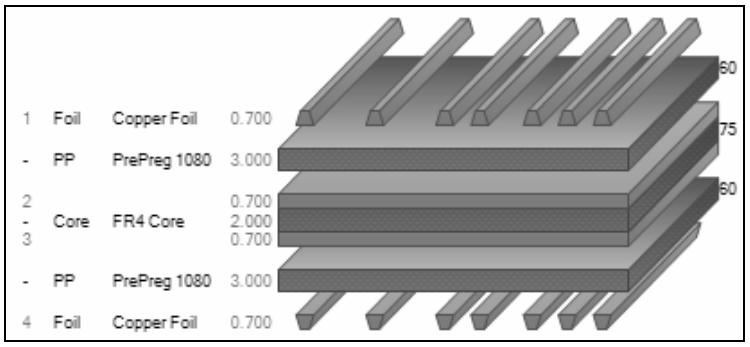
Select the upper layer of Prepreg and click the Add Layer Material button and choose Foil to display the copper foil library.

	Supplier	Supplier Description	Description	Stock Number	Cu Thickness
▶	SuperLaminates Inc	FO/001	Copper Foil	100-001	0.018
	SuperLaminates Inc	FO/002	Copper Foil	100-002	0.035
	SuperLaminates Inc	FO/003	Copper Foil	100-003	0.07

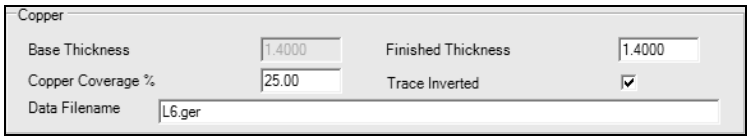
Choose the foil type and click Add Above, the copper foil layer is added above the selected Prepreg layer.



Repeat the procedure for the lower Prepreg layer: select the lower Prepreg layer and add a layer of copper foil below the layer.



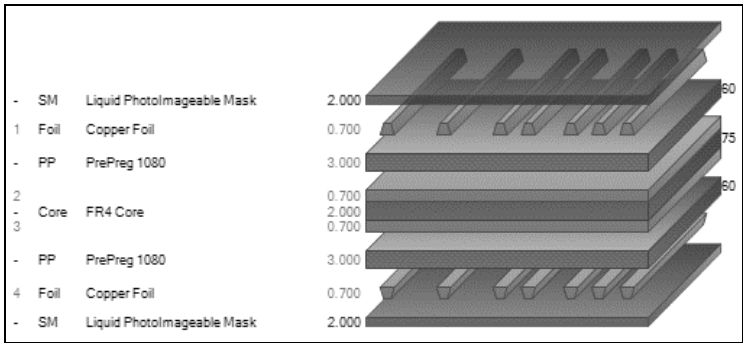
To alter the foil properties, right-click the foil layer and choose Properties. Using the Properties dialog the user can, for example, specify that the trace is shown inverted.



Note the stackup is built symmetrically about the centre layer.

Adding solder mask layers

With the upper layer of foil selected, click the Add Layer Material button and choose Soldermask to add a layer of LPI solder mask above the foil. Repeat the process for the lower foil layer.

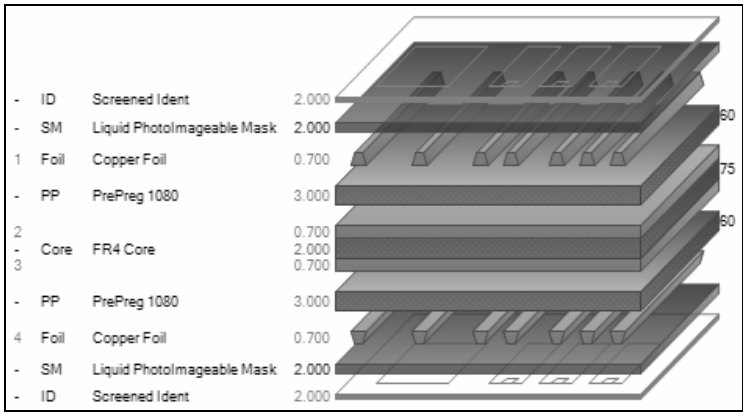


Adding the Ident layers

Select the lower LPI Soldermask layer and click the Add Layer Material button and choose Ident to add a layer of Screened Ident below the layer. The sample Ident library includes ink thickness and colour

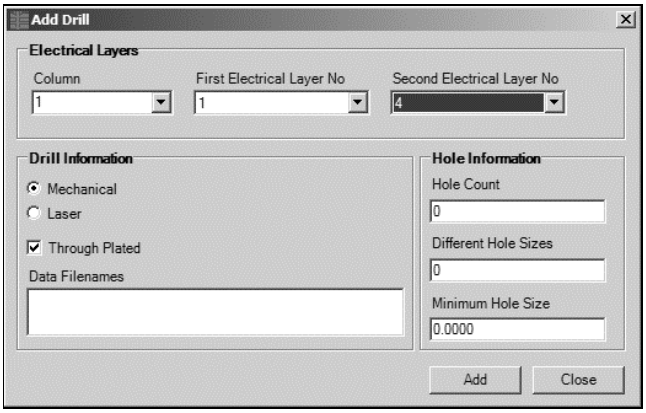
	Supplier	Supplier Description	Description	Stock Number	Ink Thickness	Ink Colour
▶	SuperInks Inc	ID/001	Screened Ident	600-001	0.05	White
	SuperInks Inc	ID/002	Screened Ident	600-002	0.05	Yellow
	SuperInks Inc	ID/003	Screened Ident	600-003	0.05	Black

Repeat for the upper layer.



Adding a drill

To add a drill between layers click the Add Drill button; the Add Drill dialog is displayed.



Select the column in which to place the drill.

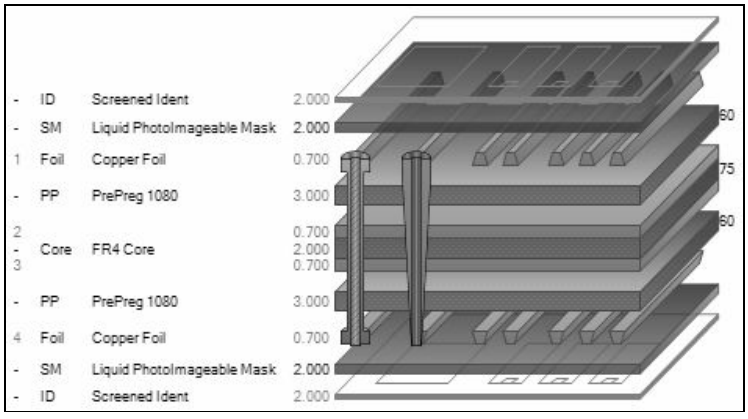
Choose the first and second electrical layer numbers (layers 1 and 4 in the example).

Specify the drill type, mechanical or laser and whether through plated. Note that with laser drills the order of drill layers is important, e.g. layer 1 and 4 is different from layer 4 and 1.

Optionally, add the NC drill data filenames.

Optionally, add the hole count, number of different hole sizes and the minimum hole size. Click Add and close the dialog. The drill information is added to the stackup. In the example we have added through plated and laser drill information.

This completes the stackup; the finished stackup is shown below



Completed stackup

Deleting a layer

Delete layer

To remove a layer from the stackup select the layer and click the Delete button.

Copying layers

Copy Material

With layers defined it will often be found more convenient to copy an existing layer and paste it into the stackup than to create a new layer “from scratch”. Select the layer to be copied and click the Copy Material button.

Click the layer nearest the destination location and choose Paste Above or Paste Below as appropriate

Note: when modifying the stackup it may be necessary to redefine the drill information to reflect the changes.

Moving materials

Move selected layer up one layer

To move materials within the stackup use the Move Up and Move down buttons.

Move selected layer down one layer

When a material is moved it is exchanged with the layer above or below, respectively.

Applying finishing

Apply Finished Thickness

To apply the finished thickness factor throughout the board, click the Apply Finished Thickness button with no material selected.

To reset the finished thickness back to the original base thickness of the materials throughout the board, click the Reset Finished Thickness button with no material selected.

Reset Finished Thickness

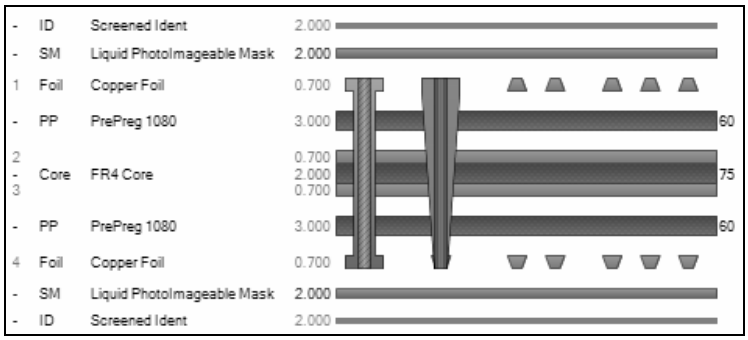
Note: when applying or resetting finishing, if a material is selected it will be necessary to specify whether finishing is to be applied to the selected material only or the whole stack.

Displaying the stackup in 2-dimensional view

View 2D button

To change the view of the stackup from its default 3-dimensional aspect, click the View 2D button.

The stackup is displayed in 2-dimensional view.



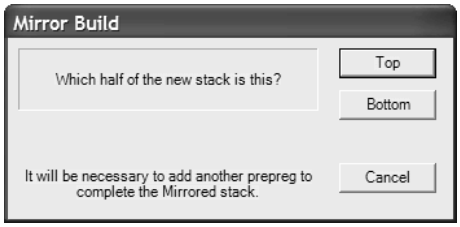
Display 3D button

Click the View 3D button to restore the 3 dimensional view.

Mirror Build

Mirror Build allows the designer to consider the stack in two halves, designing and building, for example, just the top half and mirroring the structure into the lower half.

Build the top half of the stack, including any controlled impedance structures and click the Mirror Build button; specify whether the current set of layers is the upper or lower half of the stack. To maintain symmetry, Speedstack will add a layer of material as appropriate to the stack;



the stack is reflected symmetrically into the lower half.

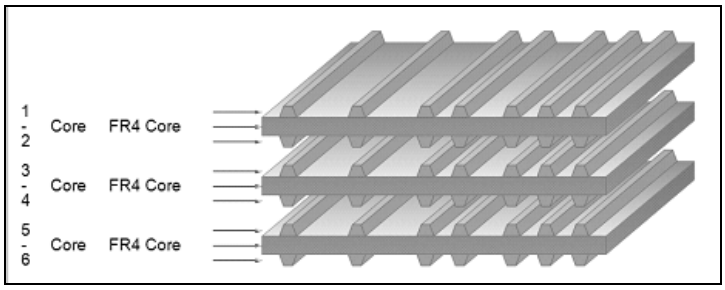
Symmetrical Build

In Symmetrical Build mode the Speedstack maintains stack symmetry as the stack designer creates or edits a stack. Changes in one half of the stack are reflected in the opposite half of the stack to ensure a symmetrical stack.

In this example we build an 8-layer stack – we begin with three cores and then illustrate how to use Symmetrical Build.

Creating a new stack

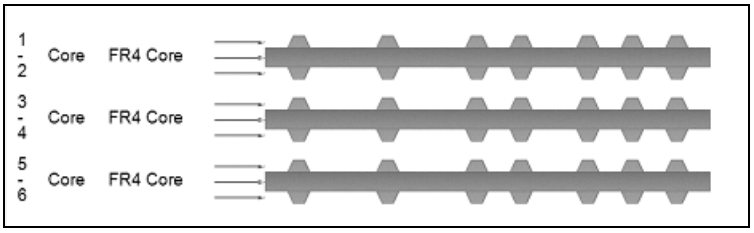
Create a new empty stackup and add three cores.



When constructing complex structures it will often be found easier to use the two dimensional aspect.

View 2D button

To change the view of the stackup from its default 3-dimensional aspect, click the View 2D button. The stackup is displayed in 2-dimensional aspect.



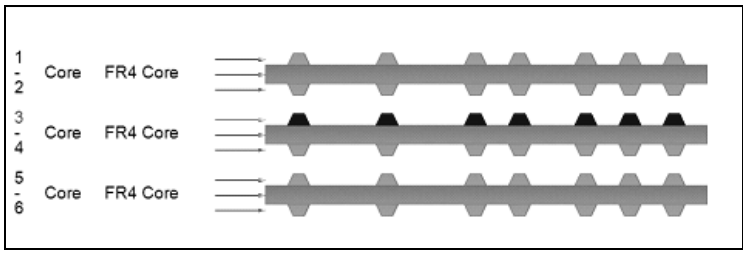
Adding a prepreg layer in Symmetrical Mode

In this example we need to add prepreg layers between cores to achieve the required dimensions.

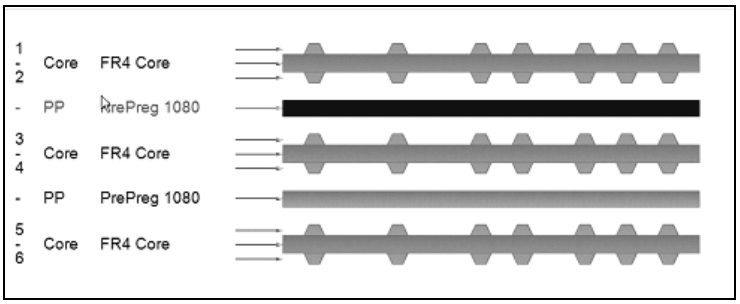
Symmetrical mode button

Switch to Symmetrical Mode and work in the top half of the stack – in Symmetrical Mode as layers are added to the top half of the stackup the Speedstack will add layers to the lower half of the stackup to maintain stack symmetry.

To add a layer of prepreg between layers 2 and 3 select layer 3 (the selected layer is shown highlighted in the figure below).

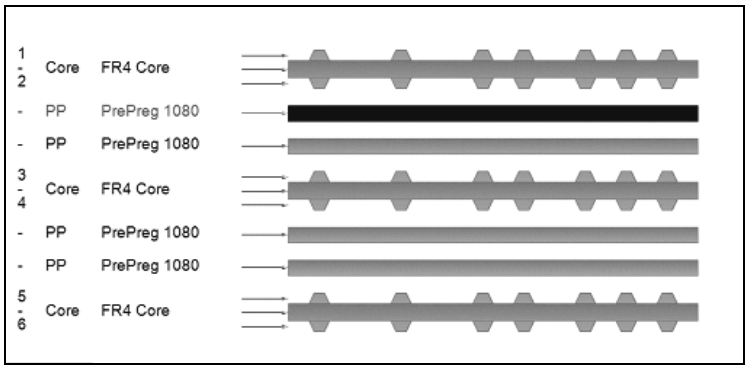


Click the Add Material button and add a layer of prepreg above layer 3 (shown highlighted in the figure below); the prepreg layer is automatically reflected in the lower half of the structure.

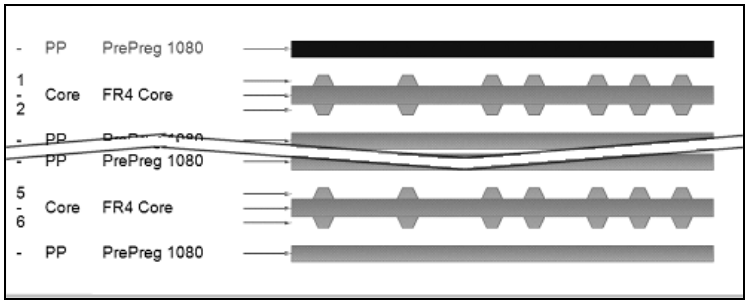


Adding a second prepreg layer

Now we add a second layer of prepreg above the layer just added; the new prepreg layer is reflected in the structure below

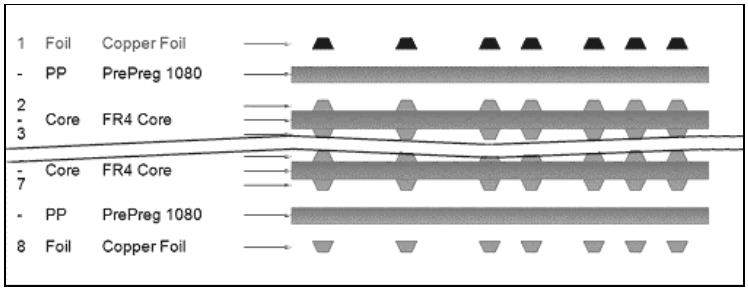


Next we add a layer of prepreg above L1 in the upper half of the stackup; the Speedstack automatically maintains stack balance by adding the corresponding layer below L6

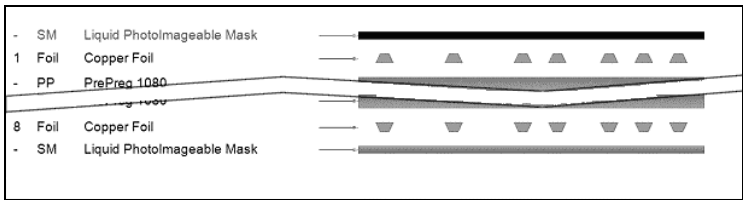


Adding foil, LPI and Ident layers

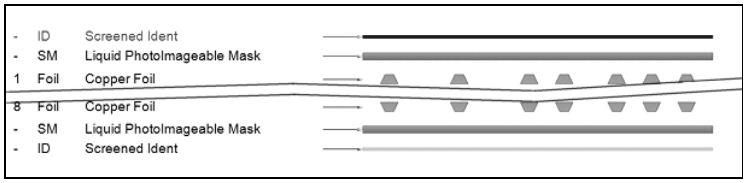
Next, we add a foil layer (L1 below) which is mirrored as L8; as part of the process the Speedstack inverts layer L8.



Next, LPI solder mask is applied to the top side of the stackup and reflected on the bottom side.

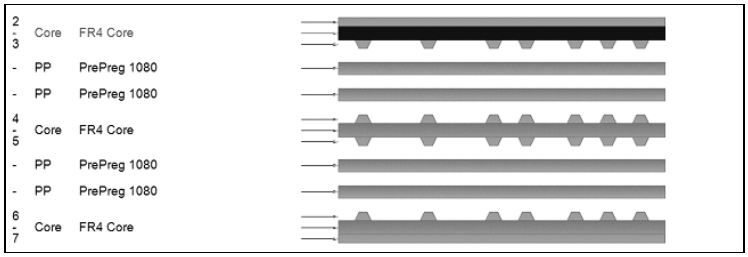


Ident layers (which are not considered components of electrical symmetry) will not be automatically reflected by the Speedstack as they are added and must be applied separately to each side of the board.

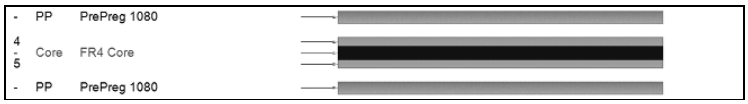


Assigning ground planes

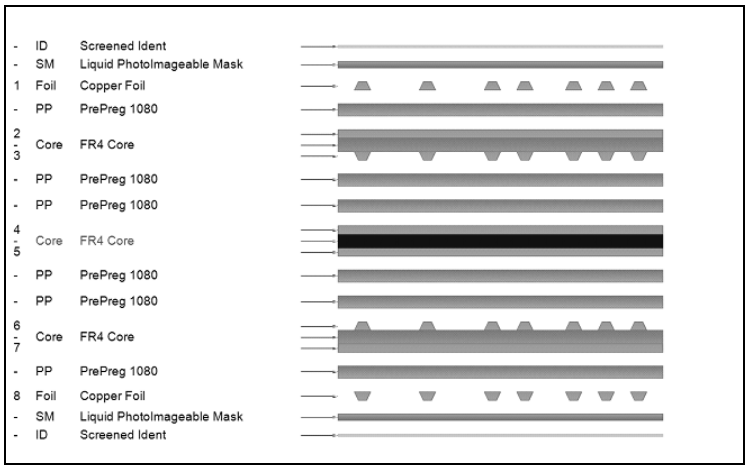
With all the material in place we assign ground planes; we begin with layer L2 – it's reflected in layer L7.



We repeat the process for the other ground plane layers; layer L4 is designated a ground plane, the change is reflected in L5 in the lower half of the stack.



The completed stack is shown below



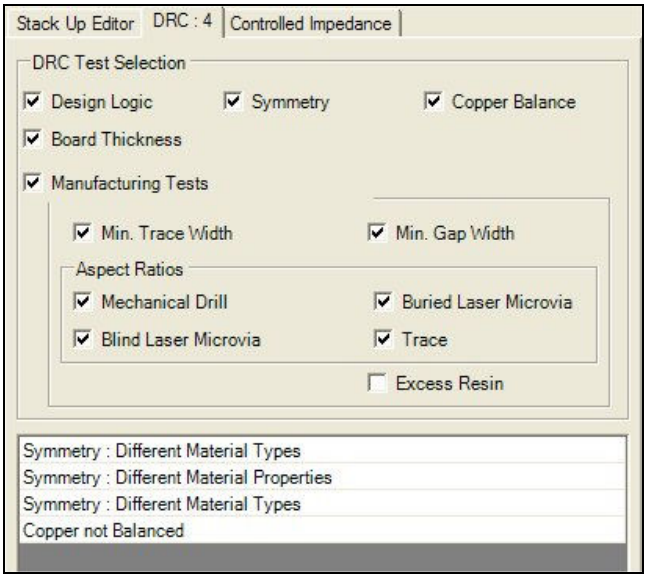
Design Rule Checking

The Speedstack includes facilities to check for errors in stackup design, such as layers placed in invalid order or asymmetrical structures. The condition of the design rule checkboxes is carried over from session to session.

The Design Rule Checker (DRC) displays results in the DRC dialog. As each design rule is broken the Speedstack increments the error count on the DRC tab.

Viewing design rule errors

Click the DRC tab to view errors.



The Design Rule Checker checks include checking for:

Two Adjacent Copper Layers

Resin Coated Copper on Internal Layer

External Prepreg

Internal Solder Mask

Internal Ident

Internal Peelable Mask

Symmetry – Different Material Types

Copper not Balanced

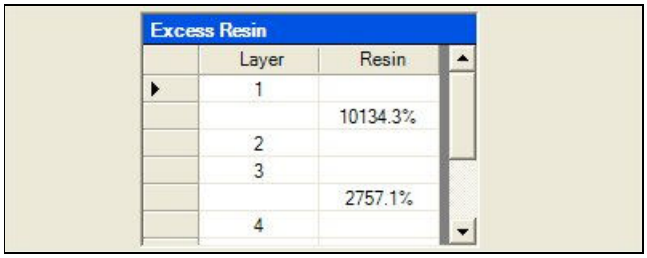
Board Thickness (If the board is outside tolerance the Stack Information in the Stack editor is displayed in red)

Manufacturing tests

- Minimum Trace width (Test carried out when calculating Controlled Impedance)

- Minimum Trace Separation (Test carried out when calculating Controlled Impedance)
- Drill Aspect Ratios for Plated holes
- Track Aspect ratio
- Excess Resin test

If the Excess Resin check box is ticked values are shown as below; scroll through the layers as required



Users can choose to display all errors or to select from a combination of Design Errors, Symmetry errors and Copper balance errors, etc.; check the boxes as required.

Click on the errors shown in the list to highlight the errors in the stackup screen. Errors are highlighted in red.

Correcting design rule errors

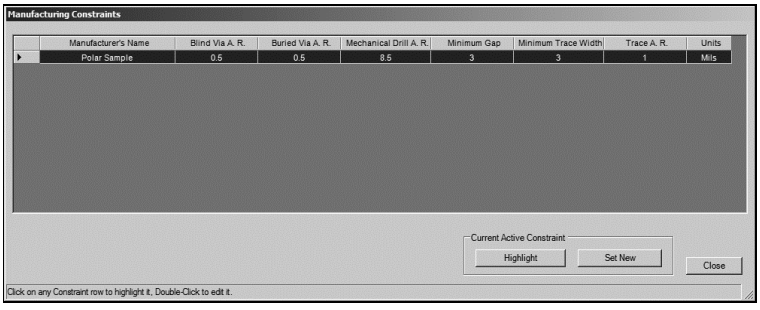
Users are strongly recommended to work through and correct errors in the order in which the errors are listed. Note that clearing each error may clear other errors in the process.

Manufacturing tests should be fixed before sending the PCB for manufacture. Hole sizes should be adjusted to comply. Failures with track and gap should be corrected, possibly by changing prepreg thickness and/or dielectric constants.

A collection of manufacturing constraints can be defined and the required one selected.

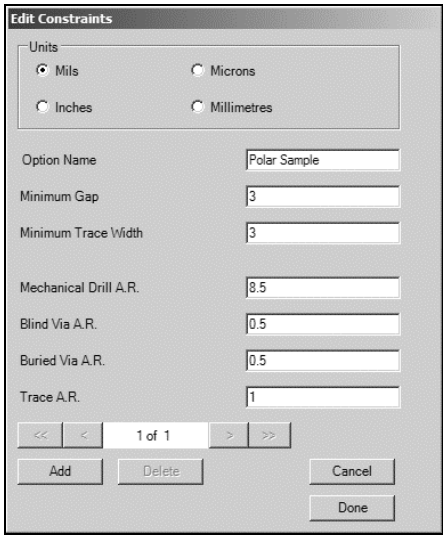
Creating and using manufacturing constraints

From the Tools menu, select Manufacturing Constraints: the Manufacturing Constraints window opens, displaying any manufacturing constraints added.



By default there will always be at least one. It is important to always have one constraint set active.

Double-click on a constraint row will bring up the Edit Constraints dialog; use the dialog to add, delete or edit constraints.



To Edit a constraint set, use the navigation buttons to select the set to modified, change the values as required and then press Done.

To Delete a constraint set, use the navigation buttons to select the set, then press Delete.

To Add a new constraint set, press the Add button, this will add a new (empty) constraint row, enter the name and constraint values and press Done.

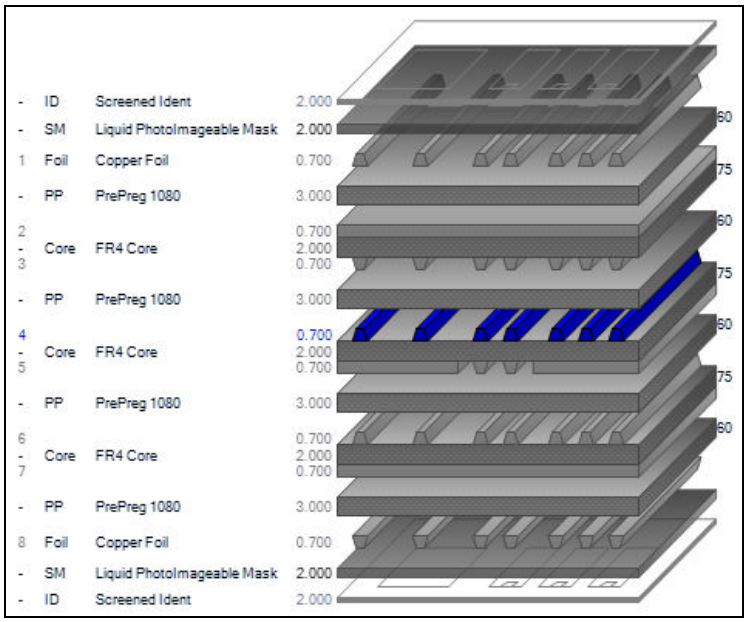
Adding controlled impedance structures

Note: before controlled impedance structures are added the stack must be fully defined (at least in terms of coppers). Attempting to add or delete coppers, or changing layer types will result in all controlled impedance structures being removed.

The Speedstack incorporates the facility to add controlled impedance structures to a layer in the stackup. The Speedstack is integrated with the Polar Instruments Si8000/9000 Controlled Impedance Field Solver so impedance values for a structure may be calculated at the click of a button.

Structure parameters may be copied to the Field Solver for processing (for example by the Si8000/9000 Goal Seeking function) and calculated values pasted back to the Speedstack for insertion into the stackup.

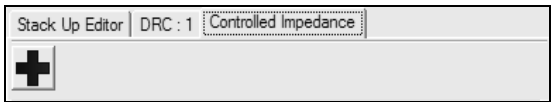
In this example we add a controlled impedance structure to signal layer 4 of the sample stackup below.



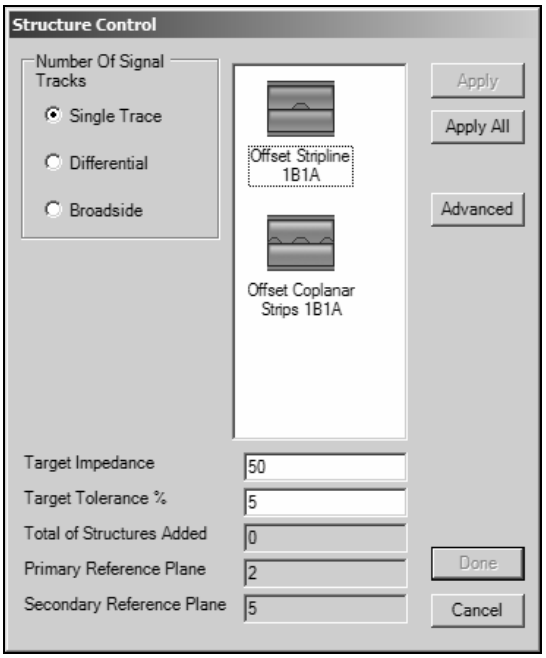
Sample stackup (showing signal layer 4 selected)

Note that in this example layer 5 is a mixed signal/plane layer. Potential reference planes for signal layer 4 are therefore plane layer 2, mixed signal/plane layer 5 and plane layer 7.

With layer 4 selected, click the Controlled Impedance tab. The Add Structure button is displayed.



Click the Add Structure button; the Structure Control dialog is displayed containing the controlled impedance structures applicable to the selected layer in the stack. Choose values for the target impedance and tolerance. If necessary, resize the Structure Control dialog to view all structures.



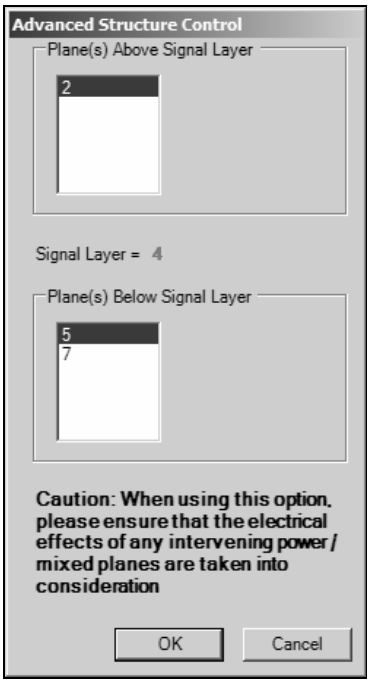
Click the Single Trace, Differential or Broadside option button as appropriate (in this case, we choose Single Trace|Offset Stripline 1B1A).

Note: Broadside only appears as an option where the signal trace is between two reference planes.

Specify the values for Target Impedance and Tolerance.

Choosing reference planes

As there are multiple reference planes available (layers 2, 5 and 7, it will be necessary to specify which planes to use for this structure. Click the Advanced button.

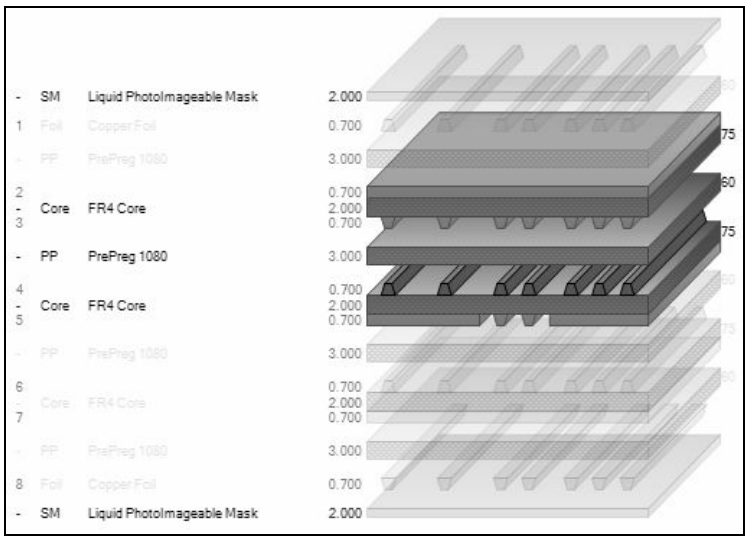


Choose a reference plane from the list of available planes. In the example structure plane layer 2, mixed plane 5 and plane layer 7 are available for reference.

Note: if plane layer 7 is chosen as reference, it will be necessary to take into account the electrical effects of mixed signal/layer plane 5.

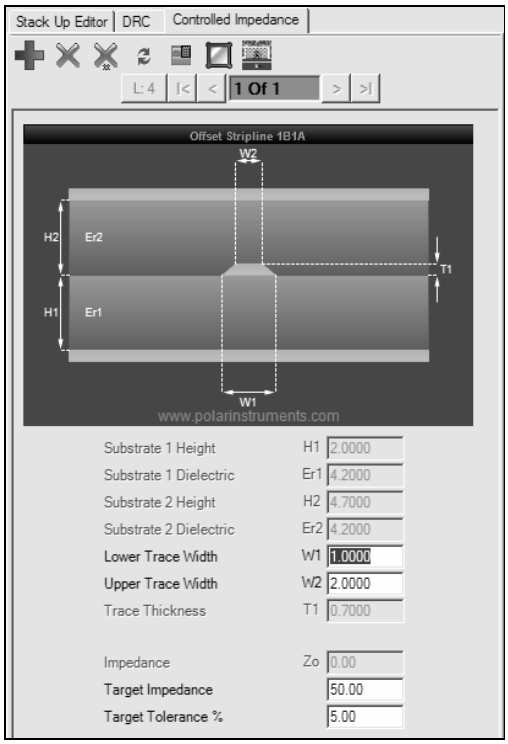
In this example we choose mixed signal/plane layer 5. Press OK to confirm.

Repeat for all structures to be added. Click Apply for each structure then click Done to finish. In this example we choose a single structure.



The stackup window changes to reflect the selected signal layer and its associated reference planes.

The applied structure is displayed in the Controlled Impedance pane.



The window displays the parameters of the controlled impedance structure. Fields shown "greyed out" are values derived from the choice of materials in the stackup. For this structure, enter appropriate values for lower and upper trace widths.

Calculate button

Click the Calculate button to display the impedance value of the structure with the current parameters. The parameters may then be varied to alter the value of the final impedance. In the example above the user can vary the trace width in order to approach the value of the target impedance; other parameters are changed by modifying the stackup dimensions (for example, core thickness H1).

Clicking Apply All in the Structure Control dialog adds a single instance of all structures matching the stackup layer and the chosen criteria; the user can then choose the structure producing the value nearest the target impedance and delete the structures that are not needed. Controlled impedance operations are performed via the Controlled Impedance toolbar.

Controlled impedance toolbar

Controlled Impedance toolbar

 Add controlled impedance structure to current layer

 Delete structure from current layer

 Clear all structures from current layer

 Refresh and calculate impedance

 Calculate structure

 Mirror Structures

 Goal Seek

Display layer and Navigate through structures

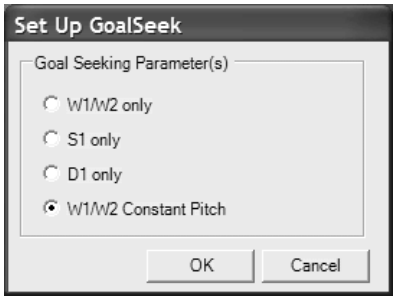
Changing parameter values

Clicking the Calculate function yields a value for impedance. The user can now vary parameters (for example, the dielectric height) to yield a value for impedance closer to the target impedance. For this example, select the dielectric layer; click the Swap Selected Material button and choose a different core (ensure the same dimensional units are used throughout the structure) and click the Refresh and Calculate Impedance button. The impedance is recalculated to its new value. To arrive at a solution acceptably close to the target impedance, use the goal seeking function of the Si8000 to alter other parameters (in this case, upper and lower trace widths).

Goal seeking with the Speedstack

The Speedstack provides the facility to solve for horizontal parameters (e.g. trace width and separation, ground strip separation) to produce the target impedance (or calculate that the target impedance is unachievable with the current values).

 Click the Goal Seek button to display the Set Up Goal Seek dialog; the options available will depend on the controlled impedance structure.



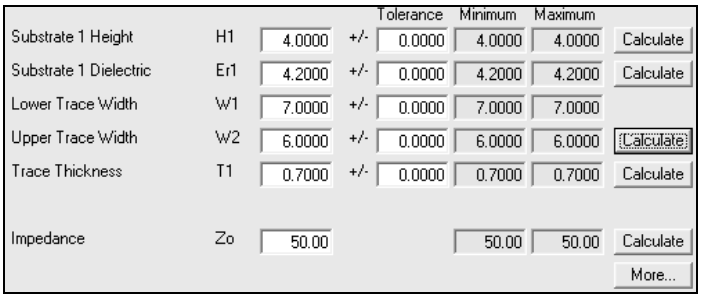
Click OK; the Speedstack attempts to arrive at the target impedance by iteratively modifying the specified parameters. It may be necessary to add or delete prepregs to achieve the target impedance.

Goal seeking with the Si8000/9000

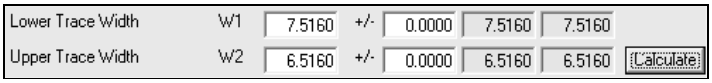
The Speedstack Stackup Design System is fully integrated with the Si8000/9000 Controlled Impedance Field Solvers. Users can transfer Stackup layer dimensions to the Field Solver, solve for stackup parameters to produce the target impedance (or calculate that the target impedance is unachievable with the current values) then transfer the solved dimensions back to the Speedstack.

Ensure the Field Solver is running and that its units match the Speedstack units. With the stackup parameters displayed in the Controlled Impedance window, click the Copy to Field Solver button to transfer the current Speedstack parameters to the Field Solver. Switch to the Field Solver and click the Paste from Speedstack button to load the parameters into the associated Field Solver fields.

For the example data below we seek a final value for impedance of 50 Ohms; H1, Er1 and T1 are fixed.



Click the Upper Trace Width Calculate button to goal seek on trace width. The Field Solver returns values for trace width to produce 50 Ohms final impedance.



Click the Copy to Speedstack button, switch to the Speedstack and click the Paste from Field Solver button to display the solved parameters for the target impedance. It may be necessary to round some dimensions (e.g. the dielectric heights) to the nearest practical values and recalculate the impedance.

Using Speedstack materials libraries

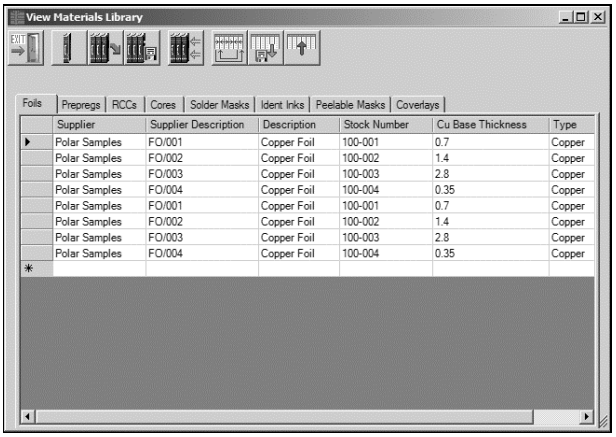
The materials libraries allow designers to manage their own libraries of board materials.

Click the Materials Library button to display the Materials Library window.

Materials Library

Working with the materials libraries

When the Speedstack is started the material library specified as the default materials library file (via Configuration Options|File Locations) is opened.



Supplier	Supplier Description	Description	Stock Number	Cu Base Thickness	Type
Polar Samples	FO/001	Copper Foil	100-001	0.7	Copper
Polar Samples	FO/002	Copper Foil	100-002	1.4	Copper
Polar Samples	FO/003	Copper Foil	100-003	2.8	Copper
Polar Samples	FO/004	Copper Foil	100-004	0.35	Copper
Polar Samples	FO/001	Copper Foil	100-001	0.7	Copper
Polar Samples	FO/002	Copper Foil	100-002	1.4	Copper
Polar Samples	FO/003	Copper Foil	100-003	2.8	Copper
Polar Samples	FO/004	Copper Foil	100-004	0.35	Copper

Each library component type is accessible via its associated tab. Click on the Tab to view or edit the component type.

Materials library toolbar

The Materials Library is managed via its toolbar

Clear Materials Library

Open Materials Library

 Save Materials Library

 Import Material into the Library

 Select & arrange Column fields

 Save column arrangement

 Load column arrangement

Creating a new library

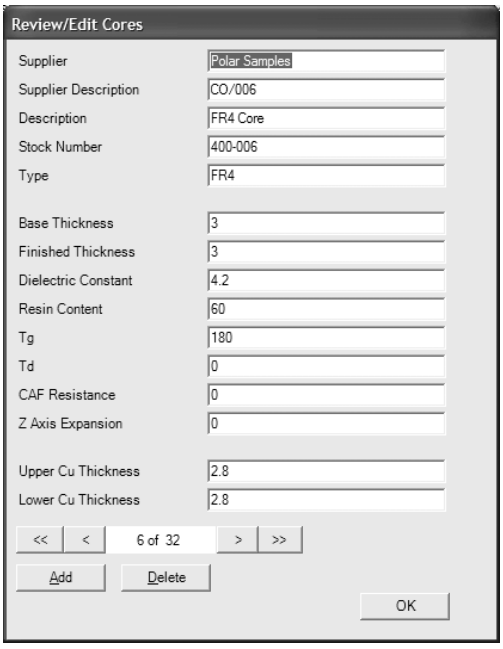
To create a new library, click the Clear Materials Library button; the library is removed from the library manager. Click the Save Materials Library button to create the new library. To have the library load as the Speedstack starts, specify it as the default materials library file via Configuration Options|File Locations.

Adding material to the library

Caution: consistency of units

When defining dimensions, e.g. layer thicknesses, for a stackup ensure that all measurements are defined using the same units (mils, mm, etc) throughout the structure and its libraries.

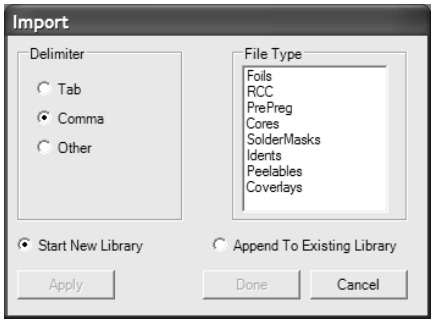
Open the library to be modified. To add materials to a library click the associated component type tab; click onto a material, or empty line. An editing box will open which will contain the material clicked on, or the last material in that type library. The material can be edited or deleted, or a new material can be added. To speed up the process of adding families of materials, when a material is added the properties of the last material are copied to the new material. The details can then be edited. Clicking OK will add any new materials to the end of the list.



Importing material to the library

The Speedstack allows users to add existing material lists to its library; material data must be arranged in the format and order used by the Speedstack library.

Sample files in comma separated value format and Microsoft Excel spreadsheet and template formats suitable for importing to the Speedstack are included in the Speedstack|Material Library Import folder. Click the Materials Library button to open the Library, and then click the Import button to open the Import dialog.



Creating a new materials library

Choose the Start New Library option and choose the field delimiter type. The library import function can accept files in a variety of formats, tab delimited, comma separated and Excel worksheet and template formats. Sections of the sample files included with the Speedstack are shown below.

	1	2	3	4	5
1	* Cores				
2	*				
3	*Type	Supplier	Supplier Description	Description	Stock Number
4	FR4	Polar Samples	CO/001	FR4 Core	400-001
5	FR4	Polar Samples	CO/002	FR4 Core	400-002

Sample library file in Microsoft Excel format

```
* Cores,,,,,,,,,,
*,,,,,,,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric
*Type,Supplier,Supplier Description,Description,Stock Number,Upp
Thickness,Dielectric Constant,Resin Content,Tg
FR4,Polar Samples,CO/001,FR4 Core,400-001,0.7,0.7,2,2,4.2,75,180
FR4,Polar Samples,CO/002,FR4 Core,400-002,1.4,1.4,2,2,4.2,75,180
FR4,Polar Samples,CO/003,FR4 Core,400-003,2.8,2.8,2,2,4.2,75,180
FR4,Polar Samples,CO/004,FR4 Core,400-004,0.7,0.7,3,3,4.2,60,180
FR4,Polar Samples,CO/005,FR4 Core,400-005,1.4,1.4,3,3,4.2,60,180
```

Sample library file in comma separated format

Files for importing into the library must be in the above format, with columns in the correct order. Examine the sample files supplied in the Material Library Import subfolder for more information. (It may be helpful to export data files from the current system into Microsoft Excel and save in Microsoft Excel workbook or text file format.)

Specify the delimiter if necessary and choose the file type (Foil, RCC, Prepreg, etc.) and click Apply. Choose the file from the list displayed in the Open dialog and click Open. Repeat the procedure for every file type; Click Done when all file types have been imported. Save the file as an .mlbx library file.

Adding material data to an existing library

To add material data to an existing library, open the library and click the Import Material button

Selecting Materials from the Library

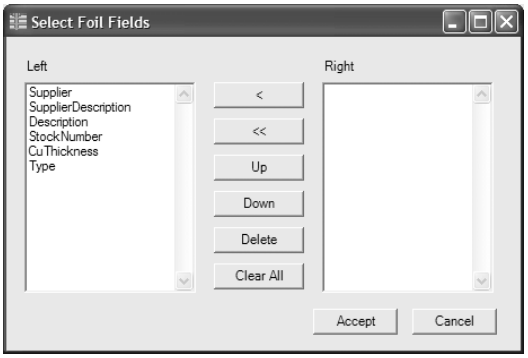
Column Order (Materials Library)

The default setting displays all columns. The columns displayed and the order they are displayed can be set in the materials Library form.

Arranging Columns in Library Forms

The Library windows can be customised in respect of which columns to display and in which order.

Click the Go to Materials Library button and select Arrange Columns; the dialog associated with the selected material tab (Foils, Prepregs, etc.) is opened.



The Left box of the dialog shows the columns that will be displayed and the order top to bottom is the order they will be displayed left to right in the library window.

Click Accept to return to the Materials Library, which will show the columns as set.

Until the column order is saved the column order is only available during the current session. Click Save Column Order to define the selected column order as the default order whenever the program is run.