PCB Layer Calculation and Documentation Tool

User Guide

Speedstack
PCB Stackup Builder

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Speedstack User Guide

POLAR INSTRUMENTS LTD

Speedstack Specifications

Maximum layer count	64+
Via rules	Conventional, blind and buried
Materials library	Foils RCC foils Cores Prepregs Solder masks Ident inks Peelable masks Coverlays Bondply Adhesive Flexible cores
Post press compensation	Yes (user defined)
Finished thickness compensation	Yes
Cu thickness calculation	Yes
Board thickness calculation	Yes
User library	Yes
Save builds	Yes

Personal Computer Requirements

Computer	IBM PC AT or compatible
Processor	Pentium 1GHz or better
Operating system	Windows XP SP1 or later
Environment	Requires .NET Framework v1.1 and above
System memory required	2GB recommended
Hard disk space required	200MB (min.)
Video standard	SXGA (1280 x 1024) or higher Hi color 16 bit or higher
CDROM/DVD drive	
Mouse	Microsoft compatible
Licensing	Fixed: Parallel/USB key
	Floating FlexLM licence (Windows servers only)

Guide To The Manual

Introduction	Introduces Polar Instruments Speedstack.
Getting started with Speedstack	Steps through the process of creating a simple stack from a set of manufacturer's data.
Configuring Speedstack	Setting up the Speedstack environment including license options, crosshatch and structure defaults, goal seeking parameters and file locations.
Using Speedstack	Discussion of the Speedstack user interface; creating and editing stackups.
Adding controlled impedance structures	Working with the Si8000/Si9000 field solver to add controlled impedance structures to the stackup model. Using the goal seeking facilities of the field solver to obtain the correct impedance for a structure.
The Speedstack Materials libraries	Using the Speedstack materials libraries, creating new libraries, adding material to the library.
Design rule checking	Using the Speedstack Design Rule Checker to correct stackup design errors.

Contents

Introduction to Speedstack

Speedstack PCB Stackup Builder

Polar's Speedstack PCB Stackup Builder is designed to accelerate the PCB stack design process and deliver significant reductions in the amount of time consumed in PCB stackup documentation and control. Given designer specifications the PCB fabricator can use the Speedstack Stackup Builder to create in just a few steps the most cost effective stack for the range of available materials. Speedstack offers interconnect designers (PCB layout engineers), PCB front-end engineers and fabricators a fast and professional solution to layer stackup creation. Speedstack provides formal documentation for everyone involved in ensuring the correct materials are used in the build process.

Speedstack PCB

Speedstack is a versatile PCB layer stackup design tool featuring powerful and easy to use graphical stackup editing capabilities. For PCB fabricators Speedstack PCB interfaces with the industry standard Polar Si8000m PCB Controlled Impedance Field Solver. It includes a link and license for Polar's Si8000m, using the proven Polar Si8000m multiple dielectric boundary element field solver to provide the impedance data for the stack. In addition, Speedstack PCB licence holders have full access to the stand alone Si8000m Quick Solver licence.

Speedstack PCB is especially tailored for PCB fabricators and PCB brokers – any one with a requirement to design or communicate controlled impedance PCB stackups.

Speedstack PCB customers are able to share stackups and read impedance requirements from designers who are using Speedstack Si.

Speedstack Si

For electronic engineers involved in stackup design Speedstack Si interfaces with the Polar Si9000e PCB Transmission Line Field Solver.

Both Speedstack Si and Speedstack PCB are able to directly output controlled impedance test files associated with each

stackup. For the fabricator this is an ideal way to link the impedance test requirements to a particular job. For the OEM this offers a clear method of sending impedance test specifications out to suppliers or brokers. Designers and fabricators can work together and select the best material combinations for minimising build costs. Fabricators can share their in house material libraries with OEMs and ensure the most effective material choice is employed in the build.

Speedstack Flex

Speedstack Flex allows OEM designers to create accurate and efficient flex-rigid PCB stackups in just a few minutes, with error-free documentation for tighter control over the finished board. For PCB fabricators, Speedstack Flex provides the flexibility to quickly calculate the impact of substituting alternative materials to improve manufacturability and reduce cost while maintaining the specified parameters and performance of the board. Speedstack Flex can be used in conjunction with the Si8000m and Si9000e field solvers when modelling and documenting mesh/crosshatch ground. Structure data and mesh geometry can be readily shared between Speedstack and the field solvers.

Speedstack HDI

Speedstack's HDI navigator quickly guides you through the sequential sub-stack lamination sequence and presents the complete assembly in a parsed graphical display that shows each phase of the multi-step lamination sequence of an HDI PCB. There is no limit to the number of press cycles that can be documented. User-definable settings within the navigator allow engineers to display layers in transparent, invisible or 3D mode. Speedstack HDI makes re-ordering and renaming sub-stacks quick and easy with the Speedflex Navigator. This is especially useful for HDI constructions.

Rapid stackup creation

Users may specify the stackup semi-automatically with the powerful Stackup Wizard or alternatively build the stack manually, layer by layer. Speedstack is flexible and allows full manual editing of stacks created by the Stackup Wizard.

Easy stackup editing

The Speedstack allows the user to view stackup in 2D or 3D format. Layer and material annotation is clear and easy to read and each layer may be selected and queried to display the associated material type and properties, including the associated data file. Visible drill information ensures that designers instantly know which layers support conventional, blind and buried vias.

Speedstack allows you rapidly to build and share stacks and verify via aspect ratios and track spacing rules. The stack file contains base material information combined with layer description and a complete listing of transmission line structures deployed in the stack. Keeping all stack information in one file ensures that manufacturing data is accurately shared between original designer and fabricator.

High quality documentation and file format

Speedstack saves the stack in efficient electronic format and outputs stack graphics in a variety of formats to suit your requirements. Stack data may be output in GERBER, DXF, BMP, JPEG, TIFF and XML. In addition, the stack data can be exported in comma-separated form for inclusion in other systems. Speedstack's high quality customisable printouts make it easy to discuss alternate builds and pricing impacts with fabricators.

Applications engineers, front end and production engineers benefit from receiving stack information in an intuitive, easy to understand format. The Speedstack .sci file contains full details of the layer stackup of a particular job. If changes are necessary or preferred stacks are to be shared with customers, Speedstack can cut the time for documentation and information sharing to a fraction of the time taken when employing traditional methods such as spreadsheet, word processor or presentation software.

Integration with the Si8000/Si9000

The Speedstack is fully integrated with the Polar Si8000m Controlled Impedance and the Si9000e PCB Transmission Line Field Solvers so the user can quickly add controlled impedance structures to layers in the stackup. The designer or board fabricator can use the Goal Seek facility of the Si8000m/Si9000e field solvers to arrive rapidly at the controlled impedance structure parameters to produce the target impedance.

Materials library

The Speedstack supports a flexible materials library. This allows the designer to use standard materials data and also provides the facility to create new material libraries. PCB fabricators can also build libraries of commonly stocked materials to give interconnect designers visibility of the materials held in stock. Speedstack thus supports three types of library – custom user libraries of materials, generic designer libraries of materials of given dielectric characteristics (for example, thicknesses) along with a comprehensive set of materials libraries from PCB base

material suppliers who are members of the Polar Speedstack Material Partner program.

Speedstack's Virtual Material mode

Speedstack provides *Virtual Material* mode allowing you to build and experiment with stackups (for example to examine the effects on impedance structures of different trace widths or dielectric heights) without requiring real materials to be entered into a materials library.

In Virtual Material mode you use the Stackup Wizard to enter a few details about the stack, the number of layers, overall board thickness, plane layers, etc., along with solder mask and copper thickness. Speedstack will then build a stack to the specified board thickness by equally distributing the dielectric regions. If a preferred core thickness is specified the software will maintain the dielectric thickness for core regions but then equally distribute prepreg regions to reach the target board thickness.

Preferred builds

PCB fabricators are able to create and share preferred builds and exchange the associated information with designers. Build data also includes blind and buried via specification. This simplifies the task of sharing stackup and drilling information between board shops and the design community.

Dimensional information

Finished board thickness is a critical dimension in many applications; Speedstack keeps track of the finished PCB thickness and tolerance, and allows fabricators the flexibility of adding in-house post-press thickness for prepreg layers. Additionally, Speedstack takes into account plating thickness where appropriate.

High layer count boards

On boards with high layer counts it can be very easy to make a change that would produce a non-symmetrical stack. The Speedstack Design Rules Check monitors symmetry across the stack, and ensures that material symmetry is maintained. Speedstack also makes it easy to set the symmetrical build mode to ensure that any changes you make are applied equally across the stack.

Supplier management

When multiple-sourcing PCBs or when moving from prototype to volume production, the stack and fabrication design rule checks ensure that the manufacturing capabilities of your chosen suppliers are not overlooked. In addition the

professional documentation output from the SB8000/SB9000 ensures that layer stack information is accurately conveyed to PCB suppliers.

Graphical interface

Speedstack offers an easy to interpret graphical interface. Clearly showing the layers supporting blind and buried vias, Speedstack also records the data file for each layer (including ident and peelable mask layers). The graphical interface is especially designed to simplify the process of communication between interconnect designer and fabricator. OEMs who need to manage boards sourced from multiple suppliers will also find this facility invaluable. In addition to physical layers Speedstack adds mask and notation for electrical layers.

Interfacing with other systems

Speedstack is able to load an XML file on launch. If an XML file (.stkx) filename parameter is specified on the command line it will import this file into Speedstack.

Speedstack can call an external program / utility / script via the External Utilities menu options. The menu items are configured within the Configuration option.

Installing Speedstack

Installing and activating Speedstack

It will be necessary to install and activate the product license and set operating options prior to building stacks or performing calculations with Speedstack.

Contact Polarcare@polarinstruments.com for installation/activation directions.

Download the software from the supplied link.

Uninstalling the software

Caution: Prior to uninstalling, make a copy of the Speedstack folder structure and store in a safe place.

To uninstall the Speedstack software:

Windows XP

Click the Windows Start button and choose Settings and Control Panel. Double-click Add/Remove Programs and choose Speedstack from the list. Click Remove.

Windows 7/8

From the Charms bar choose Settings|Control Panel; select Programs and Features and right click Speedstack and choose Uninstall.

Getting started with Speedstack

Online tutorial guides

Polar's web site provides online downloadable guides to familiarize users with the operation and features of the software; click the link below to download the Getting Started guide, along with tutorials for stack editing, managing the materials library and working with manufacturing constraints and controlled impedance structures.

http://www.polarinstruments.com/help/speedstack/tutorials/

Using Speedstack Stackup Builder

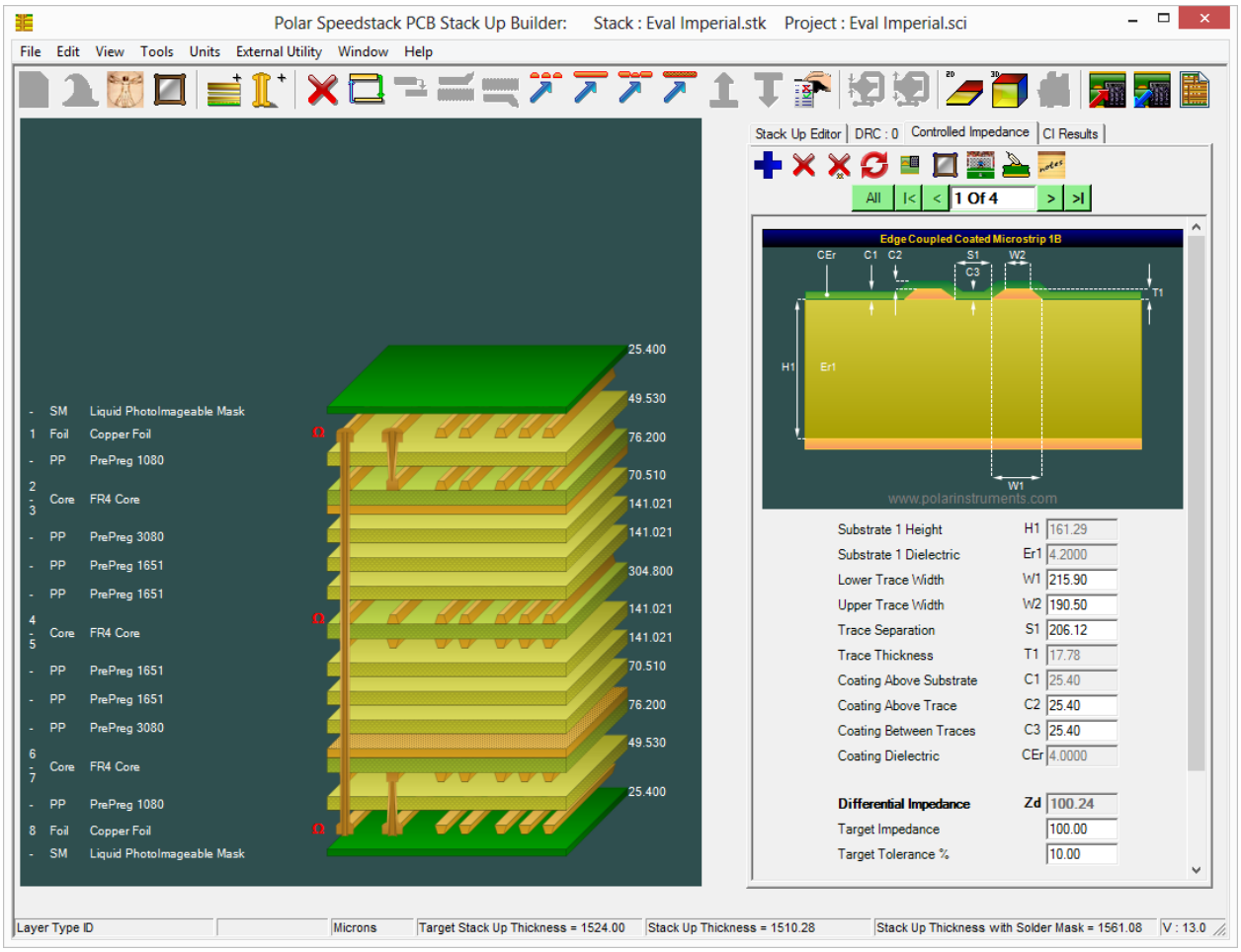
Speedstack Stackup Builder

Double-click the Speedstack icon to start the Speedstack program and display the Stack Editor.

The Stack Editor

The Stack Editor screen displays all details of the stack, including copper and prepreg materials, solder masks and ident layers, drilling information, controlled impedance structures and design rule check results.

Controlled impedance structure data may be transferred between Speedstack and the associated Polar Si8000m or Si9000e field solver to goal seek for the target structure dimensions.



The Stack Editor screen

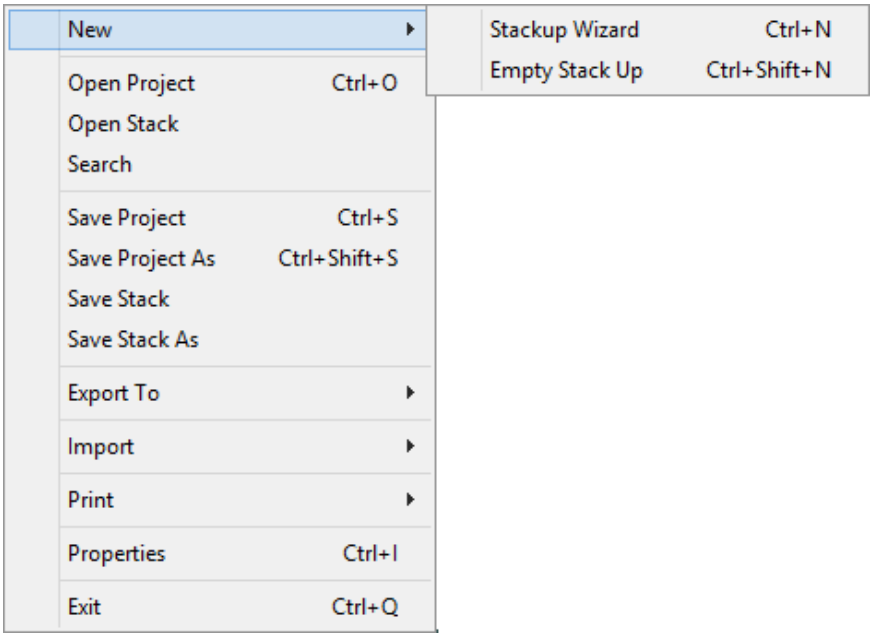
The Speedstack Stack up Editor screen comprises:

- The Menu bar — drop-down menus containing all the Speedstack Editor commands
- The Tool bar — incorporating short cut tool buttons to the most common menu commands
- The Stackup Build and Construction Window — where the board stack up is built and edited
- The Controlled Impedance window displaying the controlled impedance structures (if any) for the selected layer.
- Stack Up Editor/Notes tab— a free form text area for explanatory or commentary notes
- Design Rules Check (DRC) tab — allows design rules and manufacturing constraints to be specified and violations displayed
- Stack Up Information properties area — table containing information related to the whole stackup
- Selected Item Information area — properties table containing the attributes of the layer currently selected in the stackup

The Speedstack Menu System

The File menu

The File menu allows for creation of new stackups and projects and opening, saving, printing, importing and exporting existing stackups and projects.



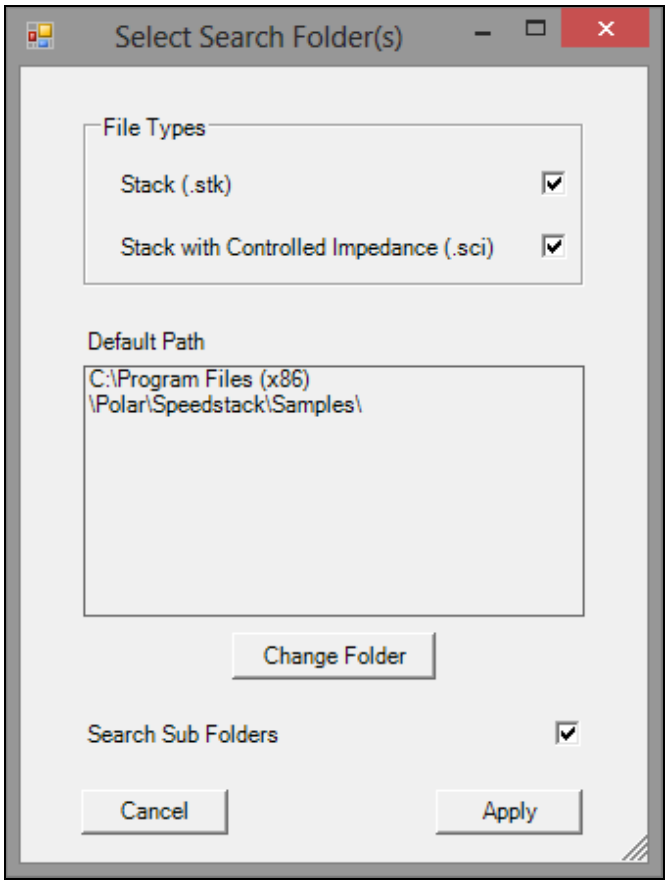
Opening projects
Stackups that incorporate controlled impedance structures are saved as projects. Click Open Project and navigate to the project folder; projects are saved as .sci files. The stackup along with all its design rule checking settings and controlled impedance information is loaded.

Saving stackups
Click the Save button to save the stackup. Users are recommended to save the stackup frequently during the stackup creation process to avoid data loss; stackups are saved as .stk files.

Saving projects
Use the Save Projects command to save a stackup and its controlled impedance structures.

Searching for stackups and project files

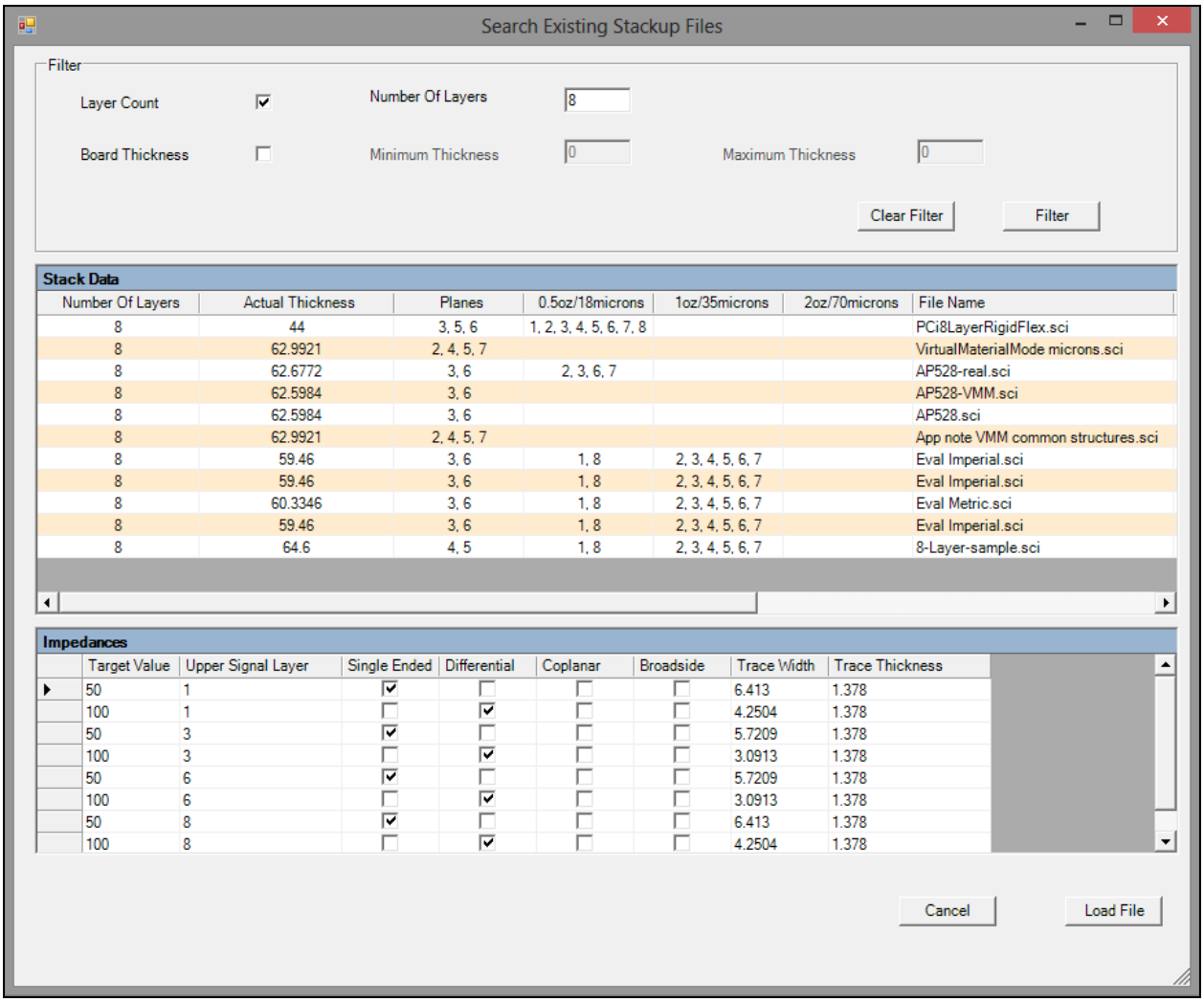
When creating new stackups and projects it will often be found convenient and timesaving to reuse an existing stack or project, modifying as required and the saving as a new stack or project. From the File menu choose Search and click Change Folder to navigate to the collection of stacks.



Choose from stacks and/or projects (stacks with controlled impedance;) with the folder chosen, click Apply.

Supplying search criteria

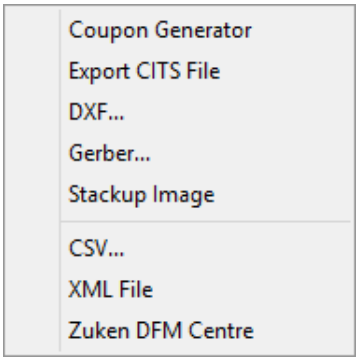
The stackups and projects within the chosen folder structure are displayed. If appropriate supply criteria, layer count, board thickness, etc. and click Filter.



Step through the list, choose the matching stack or project and click Load File.

Exporting stackup information

Speedstack incorporates the facility to export stack data to external programs. From the File menu choose Export To and choose the format from the Export To sub-menu.



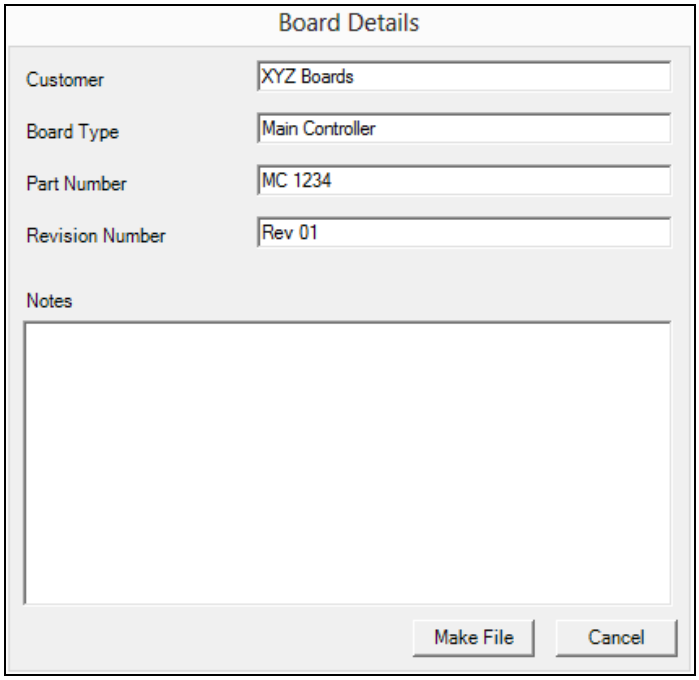
Note: the Import Export option is controlled by a purchasable license – contact polarcare@polarinstruments.com for license information.

Coupon Generator

Stacks may be exported to the Polar CGen Coupon Generator for subsequent processing into test coupons. Click Export To|Coupon Generator – open the file in CGen.

Export CITS File

Use the Export CITS File to create test files for Polar CITS controlled impedance test systems. Supply board details via the Board Details dialog.



Click Make File to generate .cif files (CITS test files).

Generating printed output

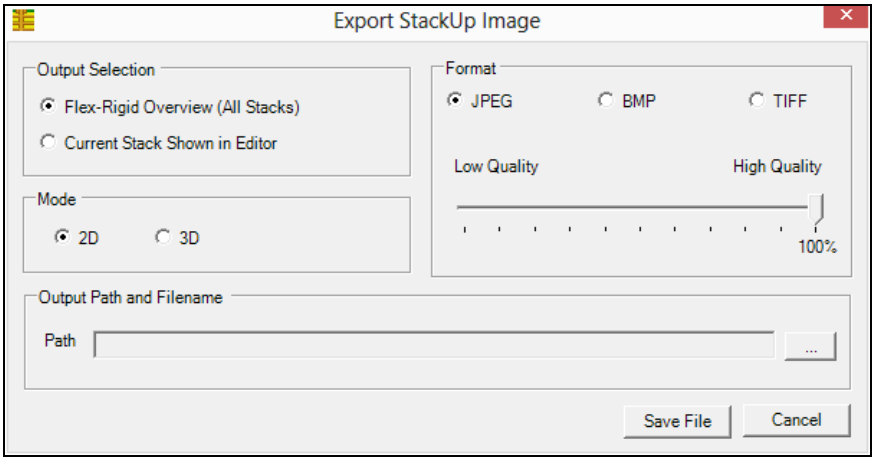
Speedstack can generate printed output in DXF, Gerber, CSV and XML, as well as graphic image formats.

DXF, Gerber, CSV and XML files

Choose DXF…, Gerber…, CSV… or XML File and navigate to a suitable folder, name the file as appropriate and save.

Stackup images

Speedstack can export stackup images in JPEG, BMP and TIFF file formats. Select from 2D or 3D displays.



The Low Quality – High Quality slider specifies JPG quality.

Choose the Flex-Rigid Overview (if appropriate) to display the master stack and associated sub-stacks or Current Stack Shown in Editor. Specify the destination folder and file name and save.

Zuken DFM Centre

The Zuken DFM Center PCB manufacturing pre-processing and CAM system integrates directly with Polar Instruments' Speedstack PCB system. Navigate to a suitable folder and save the file (XML format).

Assigning properties to projects and stackups

The stack file Properties dialog may be displayed automatically each time a new stackup is created (see Tools|Options|General) and provides a range of text fields for descriptive information, e.g. stackup author, company name, file create date, stackup name, version, etc.

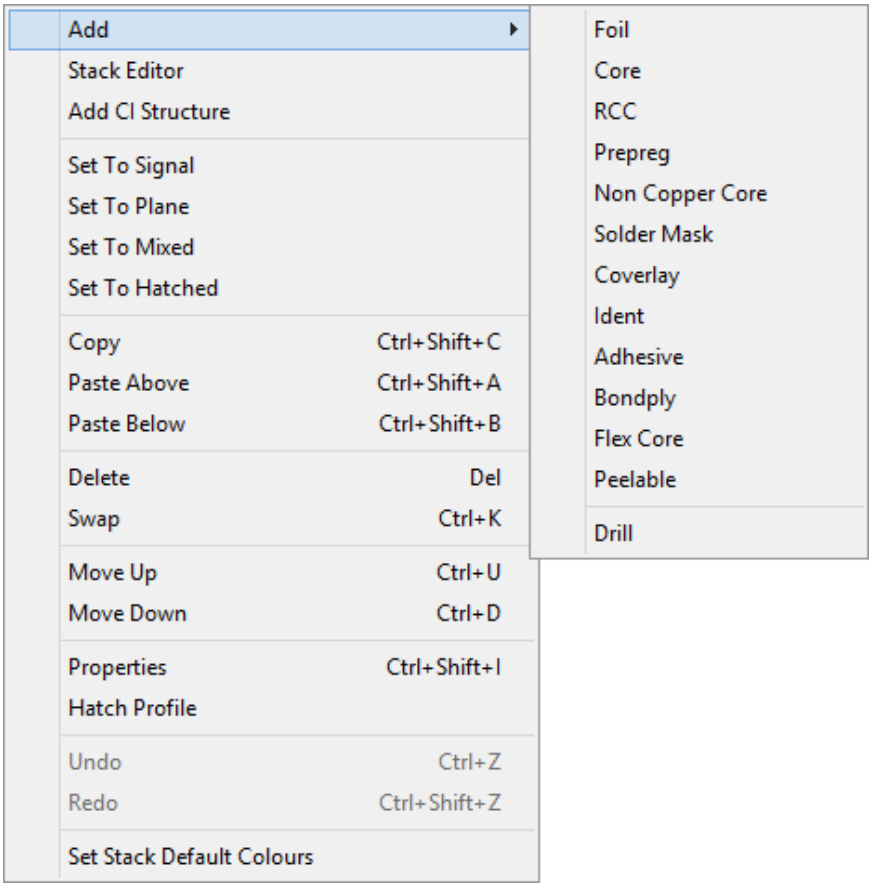
From the File menu choose the Properties command to add descriptive text fields — information contained in the Properties dialog will be displayed on stackup printouts.

To display the Properties dialog each time a new stackup or project is created, from the Tools menu choose Options and click the check box below on the General tab

Backing up stackups and libraries

It is strongly recommended that stackup files (assigned the .stk extension), project files (assigned the .sci extension) and library files (assigned the .mlbx extension) be backed up to a secure location.

The Edit menu



The Edit menu contains the commands necessary to create and modify board stack ups. The designer or fabricator works within the free-form stackup build and construction window and in Materials Library mode adds layers of foil, core, prepreg, etc., from the materials library.

Speedstack provides the option to switch easily between Material Library and Virtual Material modes allowing the stack designer to build and experiment with stackups (for example to examine the effects on impedance structures of different trace widths or dielectric heights) without requiring real materials to be entered into a materials library.

Controlled impedance structures can be added to the stack.

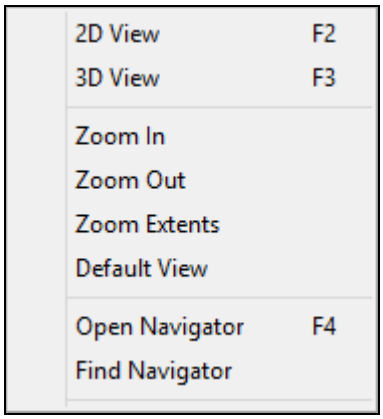
When Add CI Structure is selected Speedstack switches to the Controlled Impedance pane and allows the designer to add structures appropriate for the selected layer. The items that can be edited depend upon whether the Stack Up Editor or Controlled Impedance tab is selected.

Layers can be changed to signal, plane, mixed or hatched, moved up or down or copied and pasted, or assigned properties as required.

Use the Delete and Swap commands to delete materials or swap materials from the Materials Library.

The View menu

Use the View menu to change the Stack Editor display whilst adding or removing materials or modifying or refining the stack.



The View menu allows Speedstack to display the stackup in a 2-dimensional or 3-dimensional aspect.

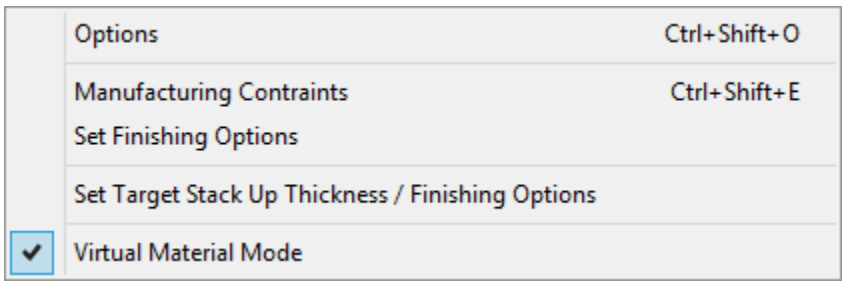
Zoom In to get a close-up view of the stack or Zoom Out to see more of the stack at a reduced size. Zoom Extents will adjust the zoom level to display the whole stack.

Hint: Click the mouse centre button/wheel to Zoom Extents.

With the Flex HDI option installed choose the Open Navigator command to view the master and associated sub-stacks. The floating Navigator window may get covered by other application windows when switching between programs; – use the Find Navigator to display a reduced Navigator window at the top left screen corner.

The Tools menu

Use the Tools menu to configure Speedstack.



The Options command displays the configuration options, manufacturing constraints, target stack thickness and finishing options. See *Configuring Speedstack* for details.

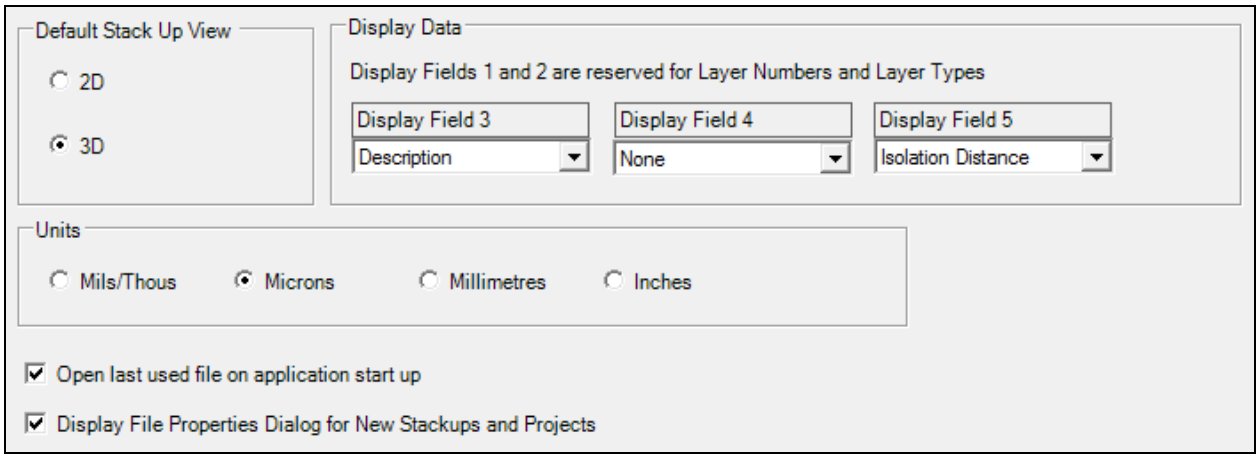
Configuring Speedstack

When first run, the Speedstack environment is initialised to its factory settings. These may require adjustment before outputting a finished stackup and/or project. Default settings are changed using Tools|Options, Tools|Manufacturing Constraints and Tool|Set Finishing Options.

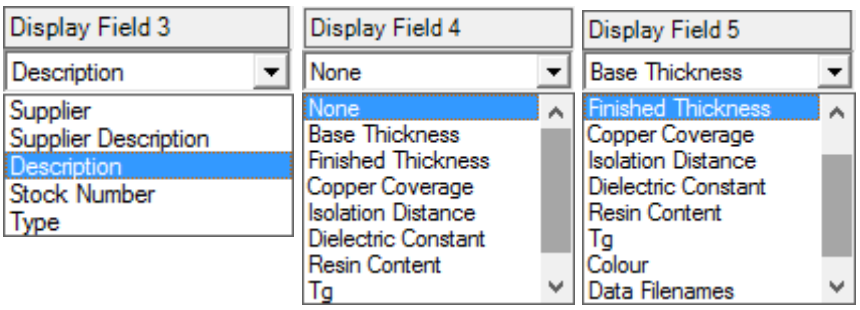
Environment and default settings

From the Tools menu choose the Options command to display the Configurations Options dialog.

General Options



Choose the Default Stackup View – 2D or 3D; select the data fields that will appear alongside the stack in the Stack Editor

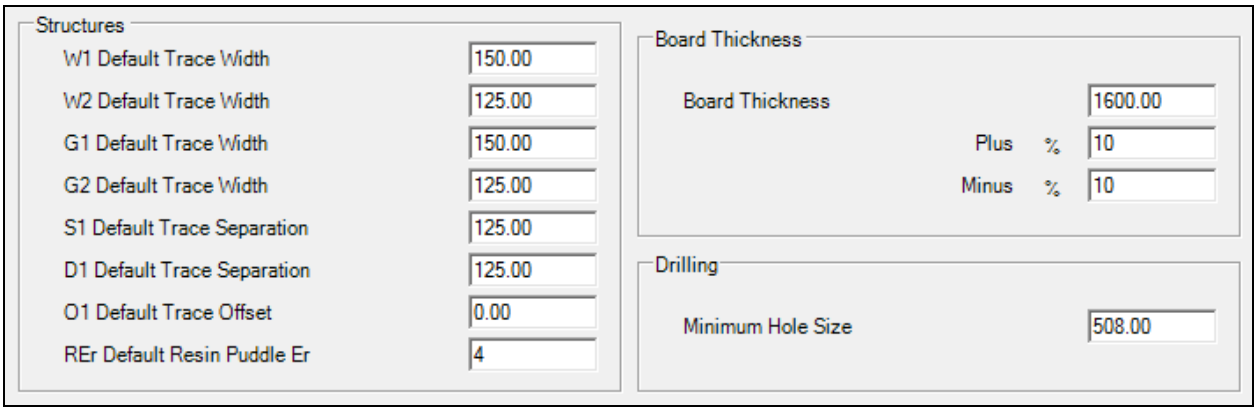


Choose the stackup units; Speedstack supports Mils/Thou, Microns, Millimetres and Inches. Click the Open last used… check box to specify that Speedstack should open the last used file on start-up.

Note: Processed Thickness is the Finished Thickness for copper layers and Isolation Thickness for dielectric layers.

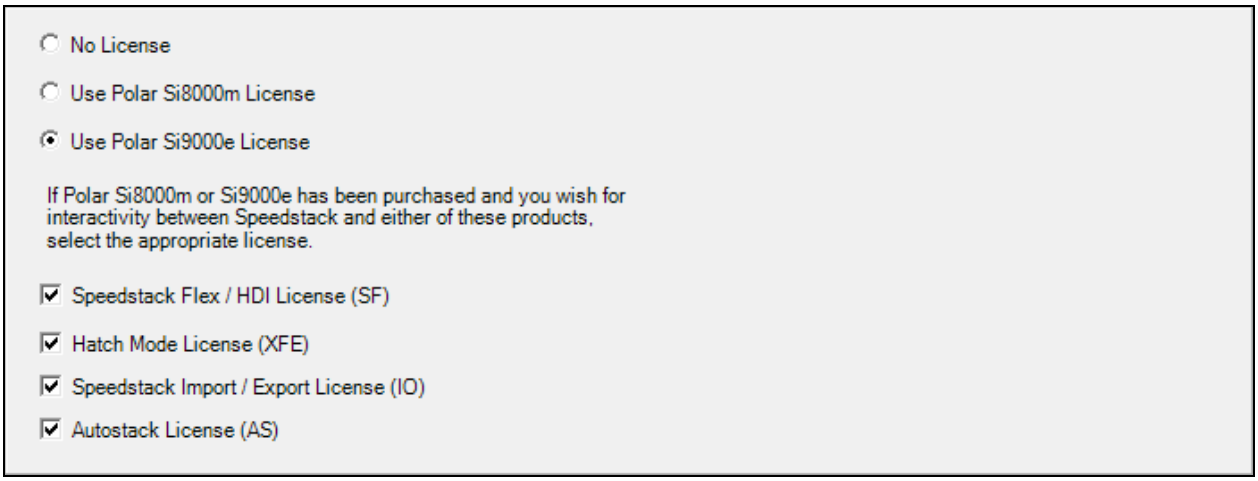
Clicking the Display File Properties Dialog… will display the File Properties Dialog each time a new stackup or project is initiated.

Structure Defaults



When adding new controlled impedance structures default values are entered for the trace widths and separations. Use the Structure Defaults tab to specify the default structure parameters, board thickness and minimum drill hole size.

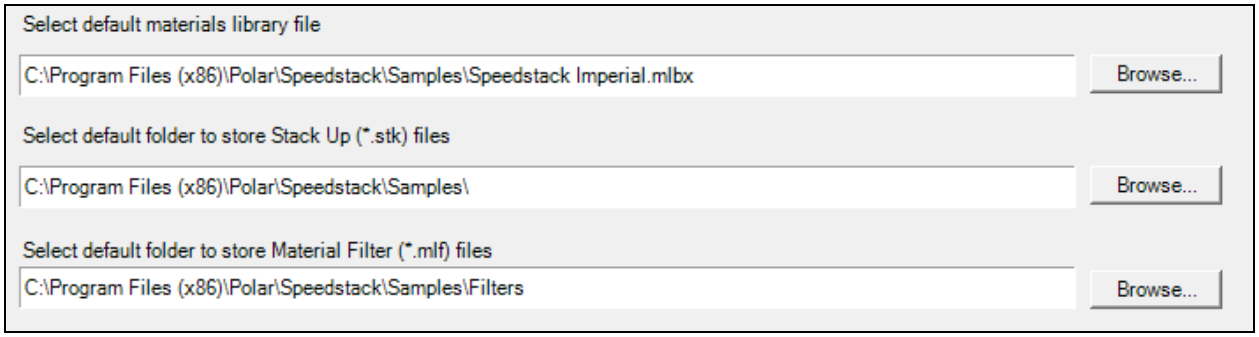
Licensing



Use the Licensing tab to tick the purchased licensing options.

To activate the Speedstack controlled impedance function, ensure that the Si8000 or Si9000 is installed; from the Licensing tab choose either Use Polar Si8000m License or Use Polar Si9000e License option as appropriate.

Choosing default file locations

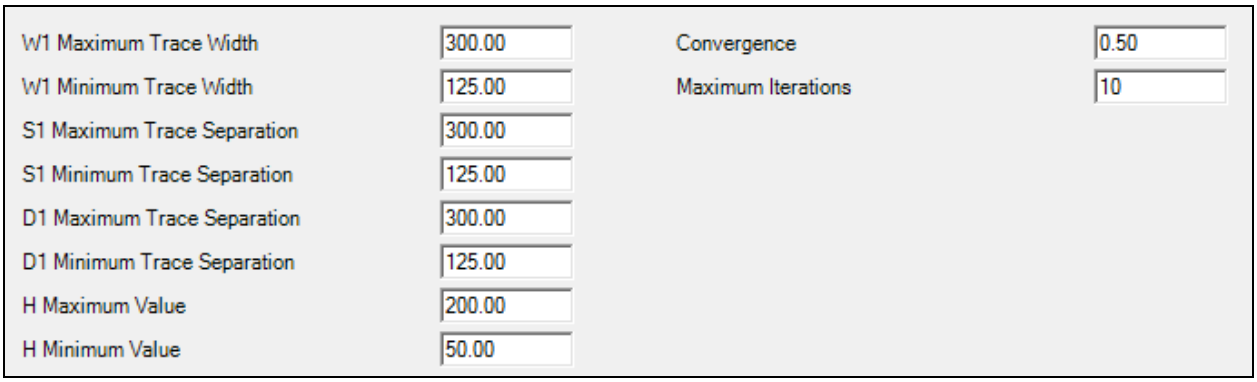


Use this dialog to choose which materials library the Speedstack uses at start-up. Click the File Locations tab and use the Browse button to navigate to the library (.mlbx) file.

The File Locations tab provides for default locations for stackup or project files and Material Filter (.mlf) files. Browse to the target folders and click OK to confirm (create new folders if necessary).

Specifying goal seeking parameters

Click the Goal Seeking tab to specify the default values for trace widths and separations used during goal seeking.

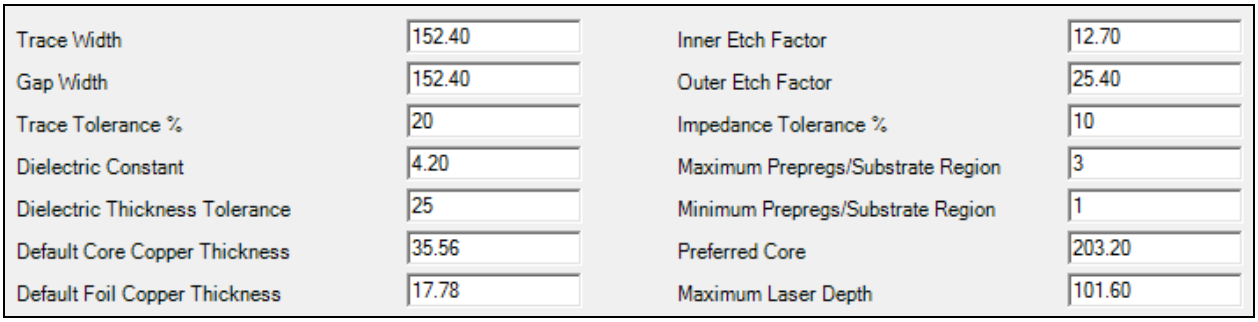


During goal seeking the calculated value for impedance will progressively converge upon the target value. In the Convergence text box specify the difference between the target impedance and the actual impedance at which goal seeking will terminate.

Use the Maximum Iterations text box to limit the number of iterations used during goal seeking.

Specifying default Autostack settings

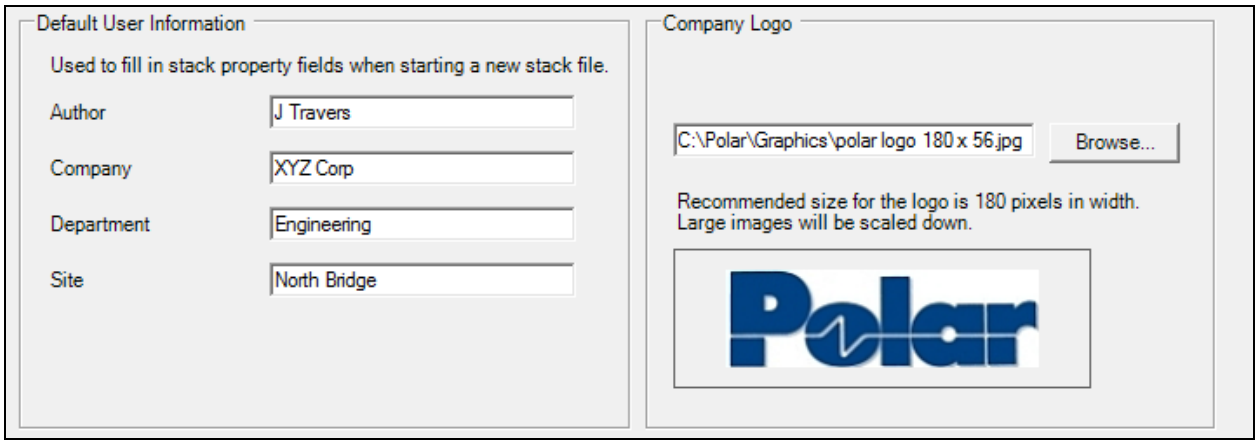
The Autostack settings will be used as starting values for the Stack Definition window when creating a new stack. They will typically be obtained from the manufacturer's material library.



Setting user defaults

Information added to the User tab will be transferred to the File Properties dialog and used on printouts

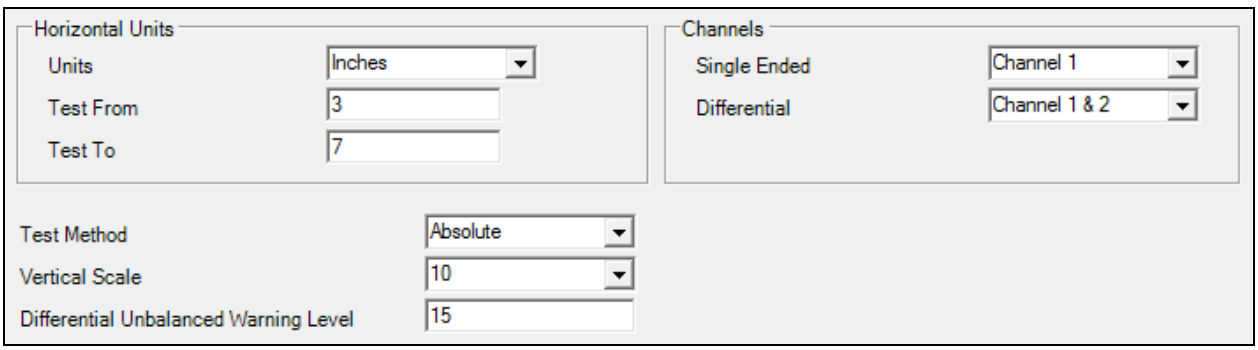
Enter information as appropriate into the associated text fields; optionally, select a graphic for use as the company logo — optimum graphic size is 180 x 32 pixels — the graphic is printed in the preview box.



Specifying default CITS test file parameters

Speedstack allows the user to generate a CITS test file for each controlled impedance structure within the stack.

Select the CITS Test tab to specify the default test parameters to be used when initiating a CITS test file.



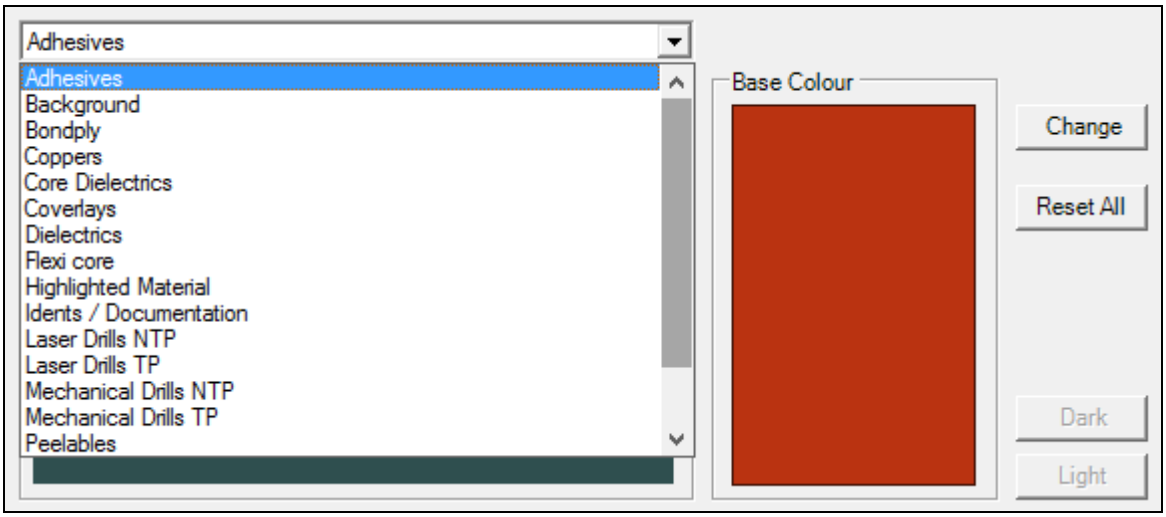
Each test file contains the test parameters (test units, distance, number of channels, etc.) to be used when testing

the stack's controlled impedance structures using a Polar CITS (Controlled Impedance Test System).

The test file may be edited via the Edit Test Data dialog.

Choosing background and stackup layer colours

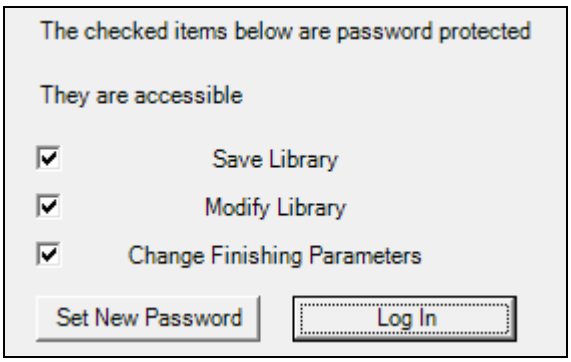
Choose the Colours tab to change stackup component colours from their factory defaults.



Click Reset All to return to cancel changes.

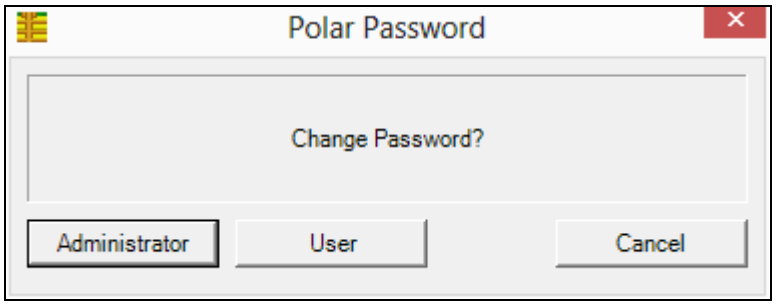
Security — setting passwords

The Speedstack security system provides for multi-level password protection. If a User password is defined, it will be requested each time the Speedstack is started. Setting an Administrator password will prevent unauthorised changes to the Speedstack configuration. Select the Passwords tab, and then Log In.

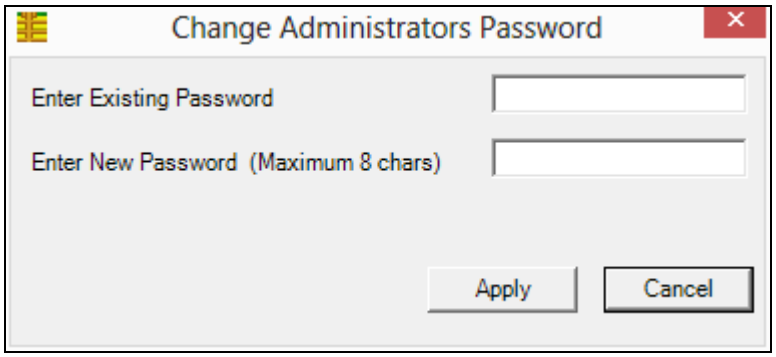


Default Passwords are blank for both the User and the Administrator. With blank passwords the password protection is transparent, and no protection is provided.

Click Set New Password.



Chose whether it is the User password or the Administrator password that is to be changed.



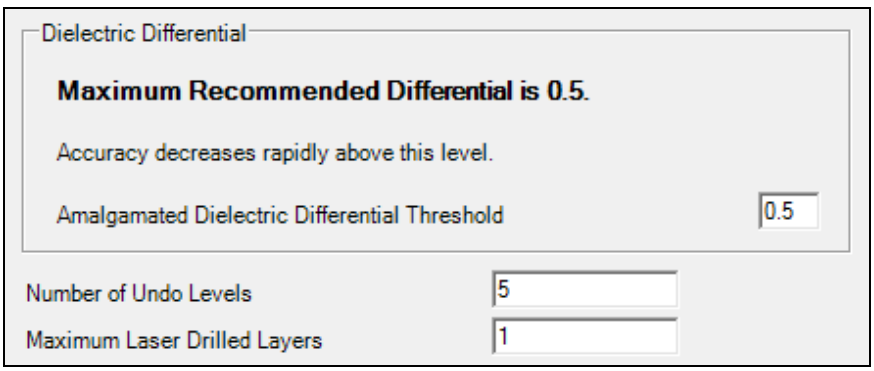
Enter the existing Password; this will be validated when moving to the Enter New Password text box. If the password is not correct the focus will not leave the “Enter Password” text box.

Enter the new password then retype it in the Confirmation text box that will appear. The two passwords will be compared and if different will enforce password re-entry.

Note: the new Users password will not be applicable until the program is re-started.

The Administrator’s password will be requested each time the Configuration Options are opened.

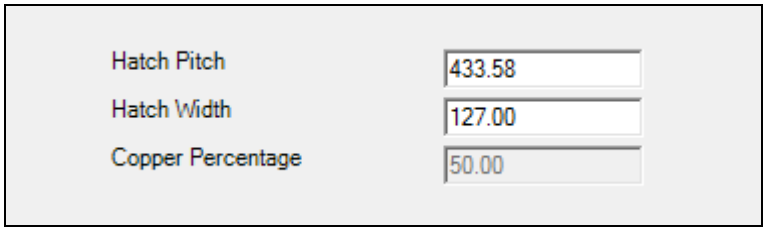
Miscellaneous Options



Use the Miscellaneous tab to specify the maximum Dielectric Differential when working with multiple dielectric structures; choose the number of levels of editing Undo and the

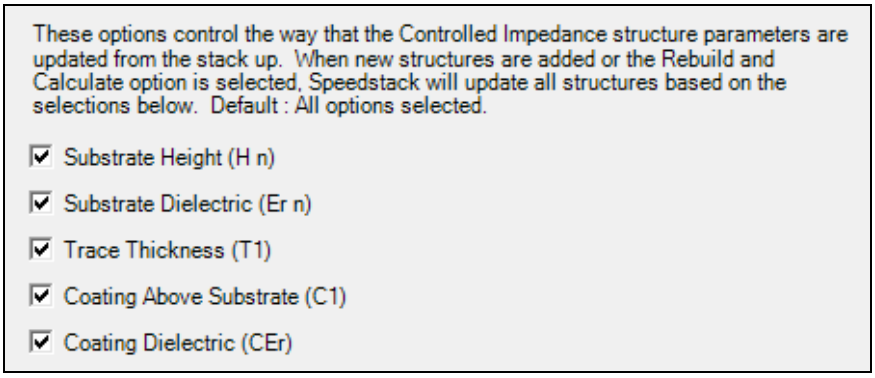
maximum number of layers a laser drill can span. (Exceeding this number will produce a Drill not Valid error message.)

Hatch Defaults



Use the Hatch Defaults tab to specify the default values for Hatch Pitch and Width and Copper Percentage when setting a plane to hatched (see Hatch Configuration.)

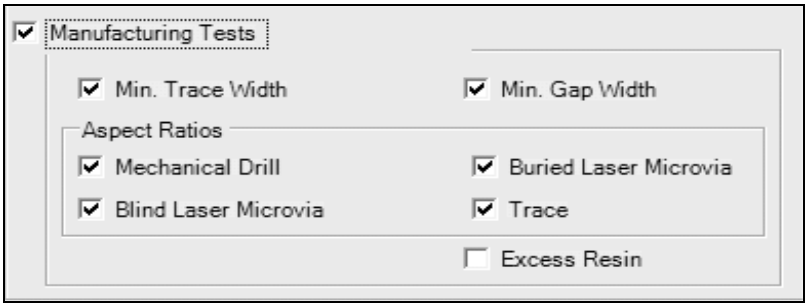
Rebuild and Calculate Structures



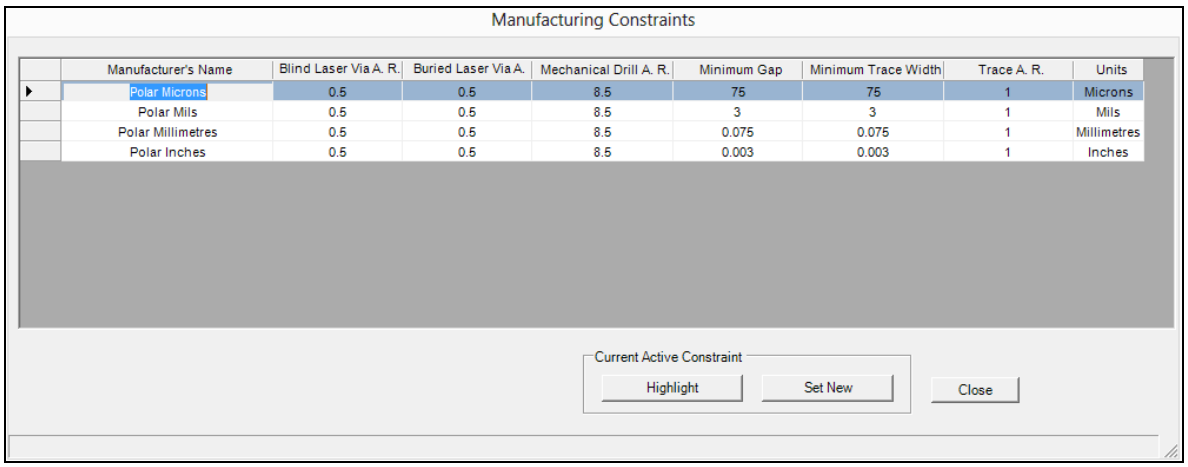
The Rebuild and Calculate Structures tab allows the designer to specify which parameters are included when controlled impedance structures are recalculated after modifying the stack.

Manufacturing Constraints

The Manufacturing Constraints options consist of a collection of manufacturing capabilities, minimum gaps and trace widths, buried and blind via and trace aspect ratios, drill aspect ratios, etc. that can be applied during design rule checking (see figure below).

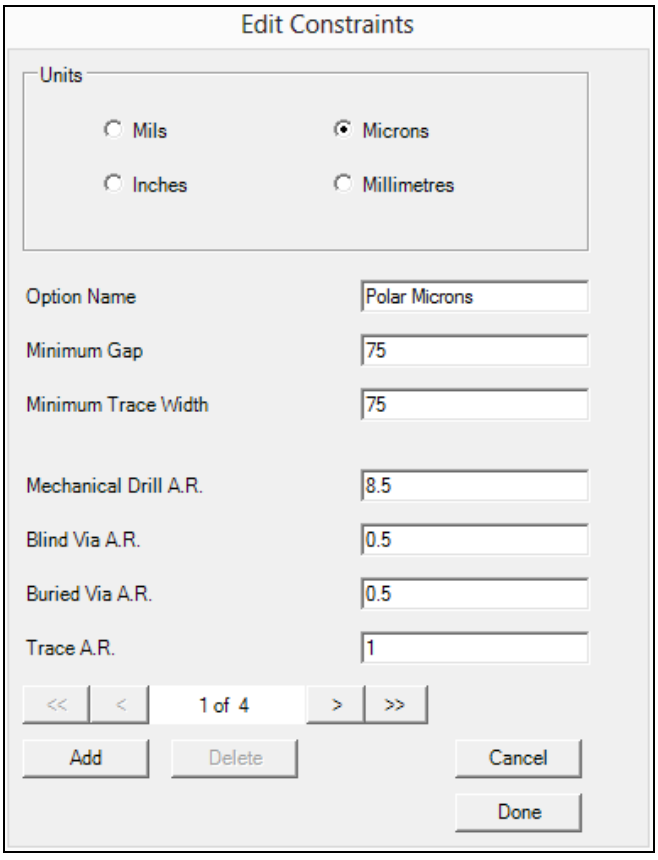


They will normally refer to differing levels of technology offered by one or more PCB manufacturers for a range of prices. The required information (shown in the example below) can normally be obtained from the manufacturer.



Click the Highlight button to highlight the current active constraint; to apply a new constraint select the constraint row and click Set New.

Editing and adding constraints
To modify a constraint or add a new constraint, double click within the constraint row to be edited.

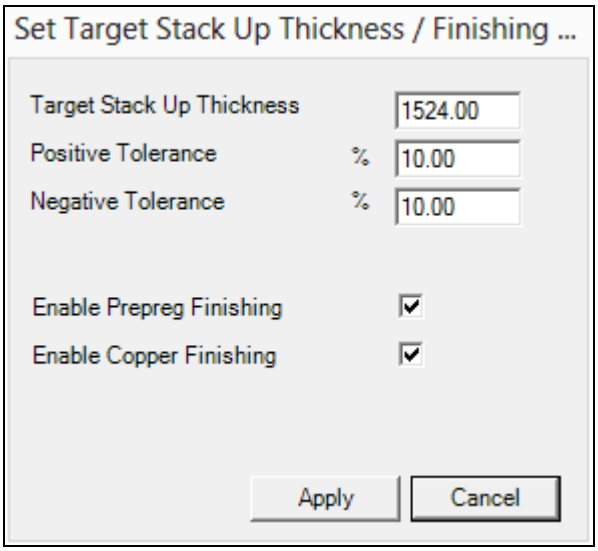


Modify each setting as required; click Done to confirm the settings and close the dialog.

To add a new constraint click the Add button, fill in the settings fields and click Done to finish. The new constraint will be added to the table of current constraints. Click the Delete button to remove the constraint from the list.

Setting the Target Stackup Thickness/Finishing options

Set the Target Stackup Thickness and tolerances via the dialog below.

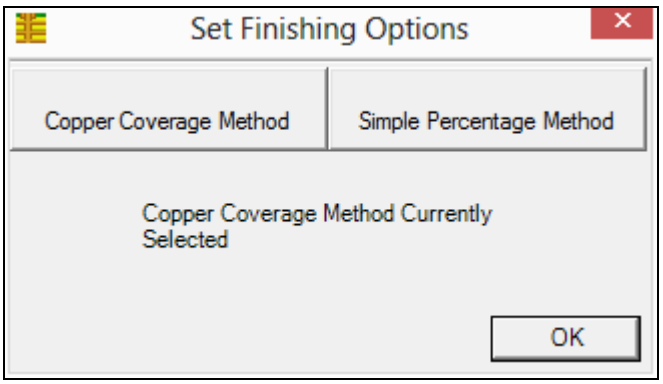


To enable prepreg and/or copper finishing tick the associated check boxes. Click Apply.

Note: Unchecking the Enable Finishing options disables the Apply and Reset Finishing buttons. Note that these buttons are only available in Materials Library Mode – they are disabled in Virtual Material Mode.

Finishing Options

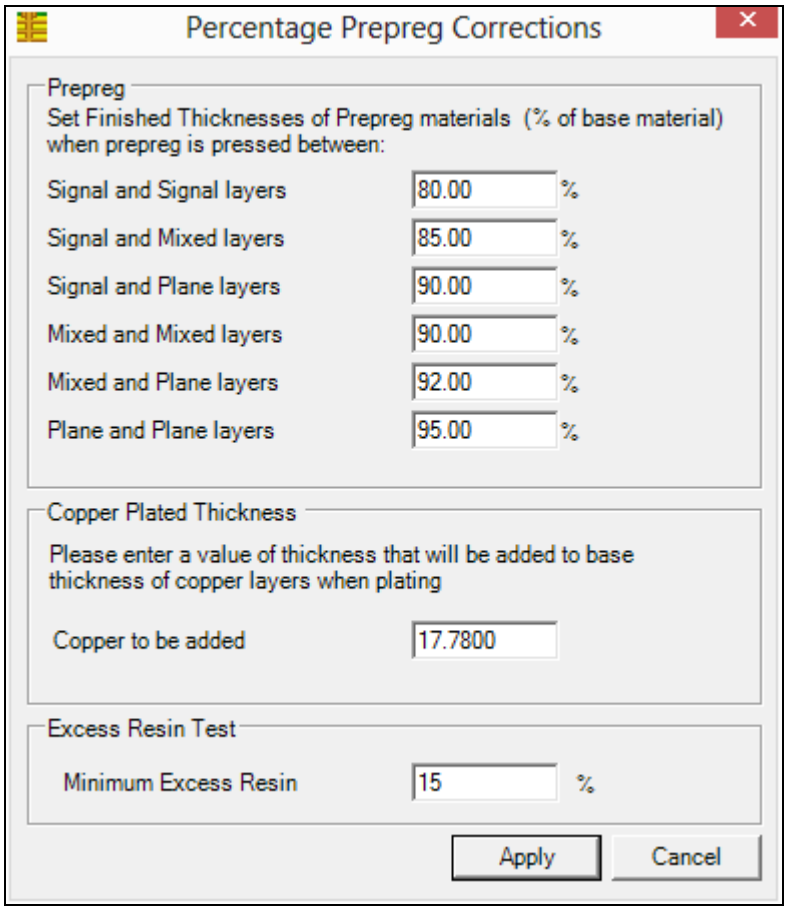
From the Tools menu choose the Finishing Options command to display Set Finishing Corrections dialog. Speedstack offers two methods: Simple Percentage Method and Copper Coverage Method.



Each method requires that the amount of copper to be added where plating is required be set. In addition, where the Excess Resin design rule check is used the minimum acceptable value must be set.

Simple Percentage Method
The Simple Percentage Method allows the user to set the percentage of prepreg base height, which will be used to determine the isolation distance. The percentage is set for each electrical layer type pair.

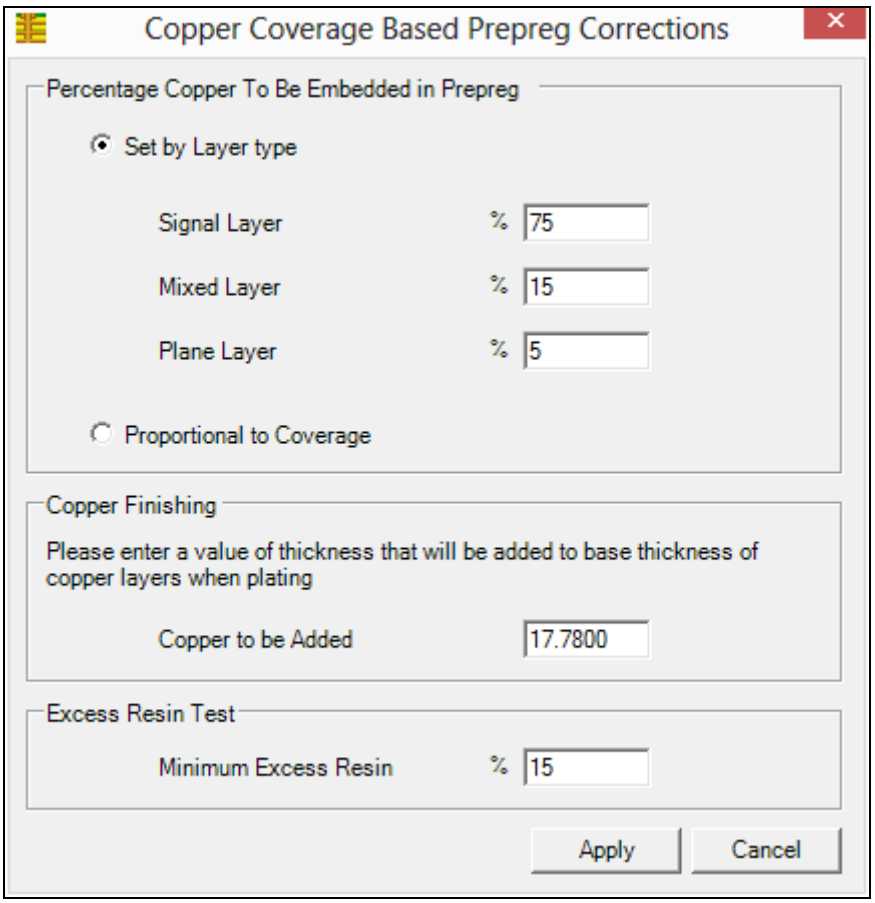
- Signal – Signal
- Signal – Mixed
- Signal – Plane
- Mixed – Mixed
- Mixed – Plane
- Plane – Plane



Copper Coverage method

The Copper Coverage method allows the user to set the amount of copper that will be embedded into the prepreg.

This can be set as a single value for each electrical layer type. Alternatively the amount of copper embedded will be calculated on an electrical layer by layer basis dependent upon the copper coverage for the layer set in the properties window. The greater the copper coverage the smaller the amount of copper that is embedded.



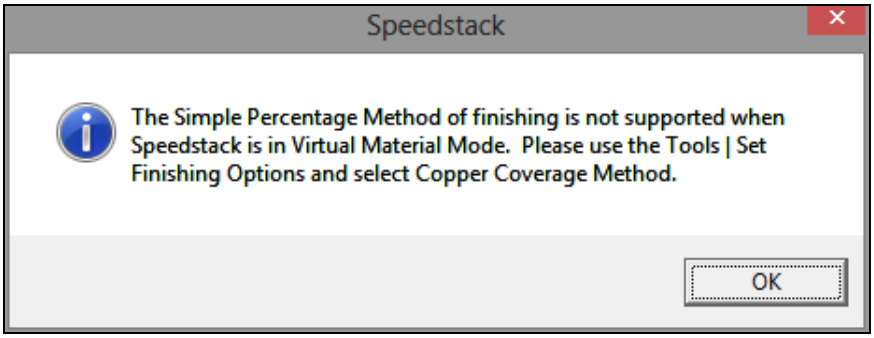
Note: The two methods of finishing are not compatible with each other. The Copper Coverage method requires that the finished thickness of prepregs be entered in the library; that value stays locked in the stack unless the Simple Percentage method is set up; if Reset Finishing is then clicked the finished thickness reverts to the base thickness.

Virtual Material mode

The Virtual Material Mode command toggles between Virtual Material and Material Library modes.

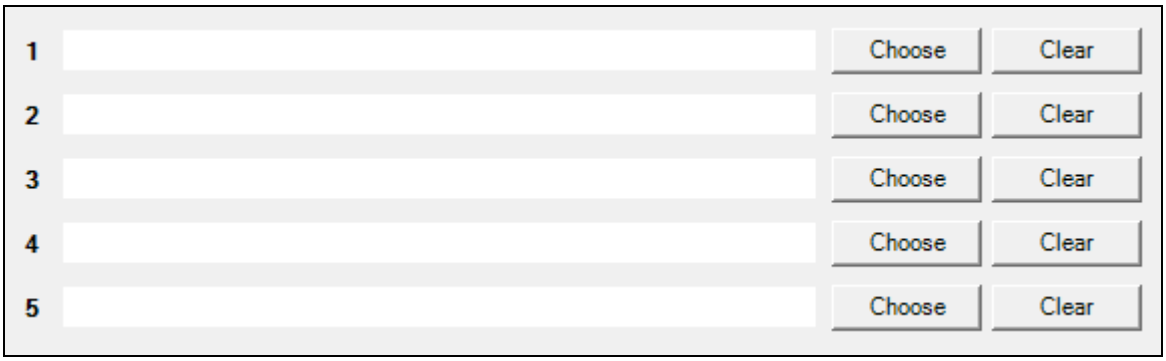
Note: Switching to Virtual Material Mode disables the Apply and Reset Finishing buttons.

Note: Virtual Material mode and the Simple Percentage method of finishing are not compatible. Speedstack displays the message below if the two are selected simultaneously.



Working with external utilities

Speedstack can call an external program / utility / script via the External Utilities menu options. The menu items are configured via Configuration Options|External Utilities.



To specify a program click Choose and navigate to the program and click Open. The program will be added to the External Utility menu.

The Speedstack toolbar

The Speedstack toolbar comprises shortcut links to the most popular commands.

Note: toolbar buttons will be enabled/disabled depending on whether Speedstack is performing stack editing or controlled impedance calculations. Pause the mouse over each tool button to display the tool's screen tip

File operations

Create new stackup

Stackup Wizard

Stack building operations

Symmetrical Mode

Mirroring Mode

Add layer to the stackup

Click to select the layer type. The list of layer types is displayed in the associated sub-menu.

Layers available include:

Foil	Add foil layer to the stackup
Core	Add core layer
RCC	Add resin coated copper layer
Flexible core	Add flexible core layer
Prepreg	Add prepreg layer
Non-Copper Core	Add non-copper core
Soldermask	Add solder mask
Coverlay	Add coverlay layer
Ident	Add screened ident layer
Peelable	Add peelable mask
Adhesive	Add Adhesive
Bondply	Add bond ply adhesive

 Add mechanical/laser drill between layers

Editing the stackup

 Delete selected stackup layer or drill

 Swap selected material

Note: the Copy and Paste buttons below are only enabled for the Stack Editor and DRC tabs – they are disabled for the Controled Impedance and CI Results tabs.

Copying and pasting materials

 Copy material of the selected layer

 Paste material above selected layer

 Paste material below selected layer

Changing plane types

 Set the selected electrical layer as a signal layer

 Set the selected electrical layer as a plane

 Set the selected electrical layer as a mixed signal/plane layer

 Set the selected electrical layer as a hatched plane

Note: the Move Selected Layer buttons below are only enabled for the Stack Editor and DRC tabs – they are disabled for the Controlled Impedance and CI Results tabs

 Move selected layer up one layer

 Move selected layer down one layer

 Display properties dialog for the selected layer or drill

Note: the Apply and Reset Finishing buttons below are only enabled for the Materials Library Mode with the Prepreg and

Copper Finishing Options checked (see Set Target Stack UpThickness/Finishing Options) – they are disabled for the Virtual Materials Mode.

Applying finishing

Apply finished thickness

Reset finished thickness

Changing the stackup view

Display 2-dimensional view

Display 3-dimensional view

Managing the materials library

Display materials library

Virtual Material mode

Exchanging data with the Si8000 or Si9000 Field solver

Copy controlled impedance data to field solver

Paste controlled impedance data from field solver

Re-engineer current stack

Creating and editing stackups (Virtual Material mode)

Speedstack provides the option of switching easily between Material Library and Virtual Material modes allowing the stack designer to build and experiment with stackups (for example to examine the effects on impedance structures of different trace widths or dielectric heights) without requiring real materials to be entered into a materials library.

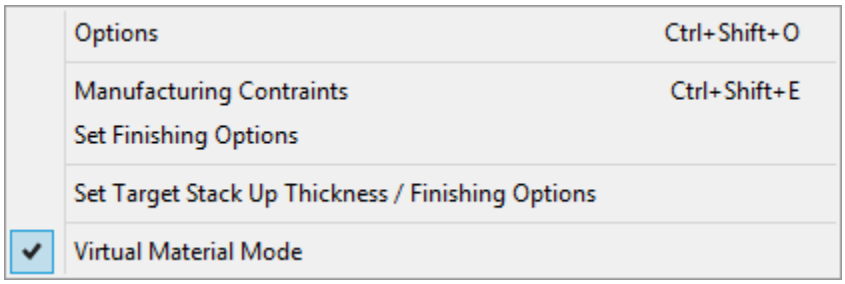
In Virtual Material mode the Stackup Wizard allows rapid entry of stack details, the number of layers, overall board thickness, plane layers, etc., along with solder mask and copper thickness. Speedstack will then build a stack to the specified board thickness by distributing the dielectric regions equally. If a preferred core thickness is specified the software will maintain the dielectric thickness for core regions but then equally distribute prepreg regions to reach the target board thickness.

This section will describe the steps to construct an 8-layer, symmetrical FR-4 stack to the specification below using Speedstack's Virtual material Mode.

Thickness:	60 mil
Signal layers:	1, 3, 6, 8
Plane layers:	2, 4, 5, 7
Er:	4.2
Preferred core thickness:	8 mil
Copper (all layers):	1 oz. / 1.4 mil
LPI Mask:	1 mil
PTH drill passes:	Layers 1 – 8
Laser microvia passes:	Layers 1 – 2, 8 – 7
Impedance structures:	SE 50 Ohm Layer 1, Diff 100 Ohm Layer 1

From the Units menu choose Mils/Thou

From the Tools menu toggle Virtual Material Mode On.



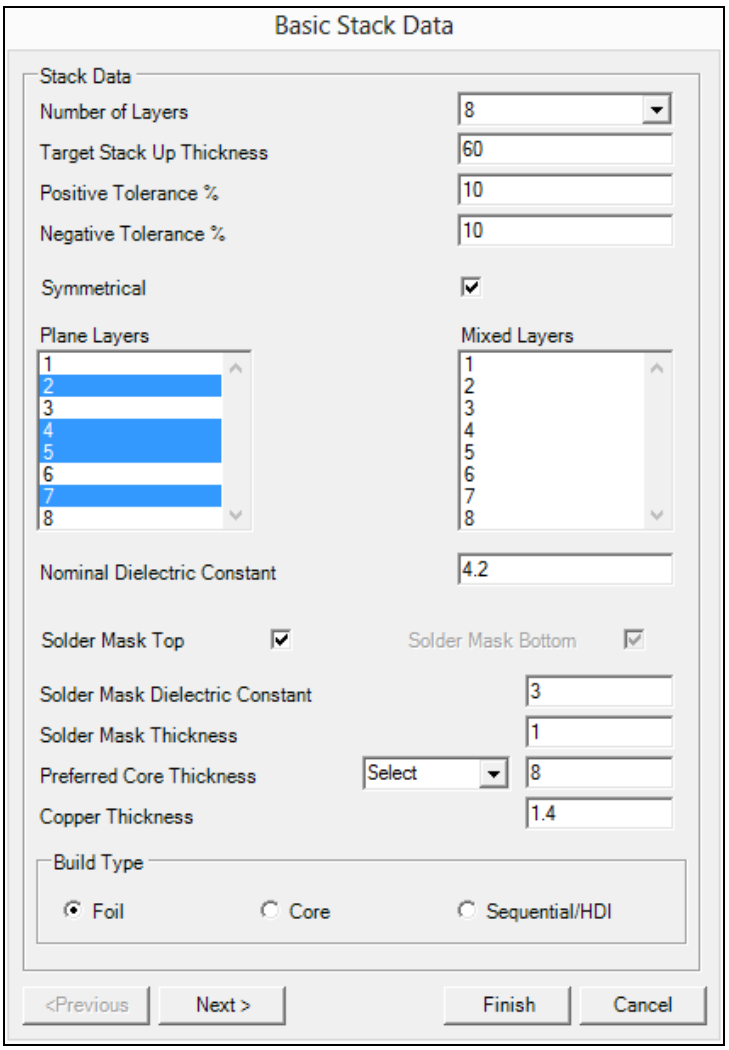
Virtual Material mode is indicated by VM overprinting the Go to Material Library button.

Using the Stackup Wizard

From the File menu chose New|Stackup Wizard.

Setting basic stack data

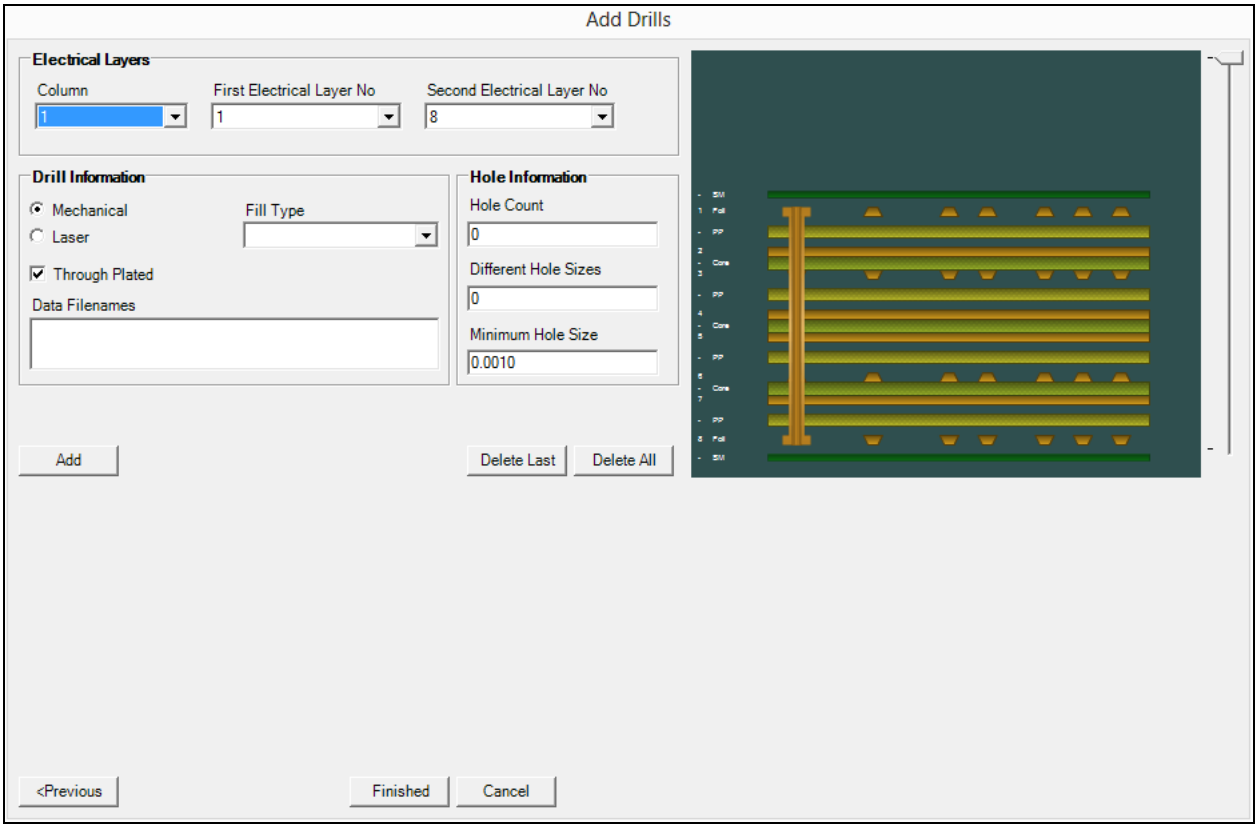
Fill in the dialog as shown below.



Click Next to add drills.

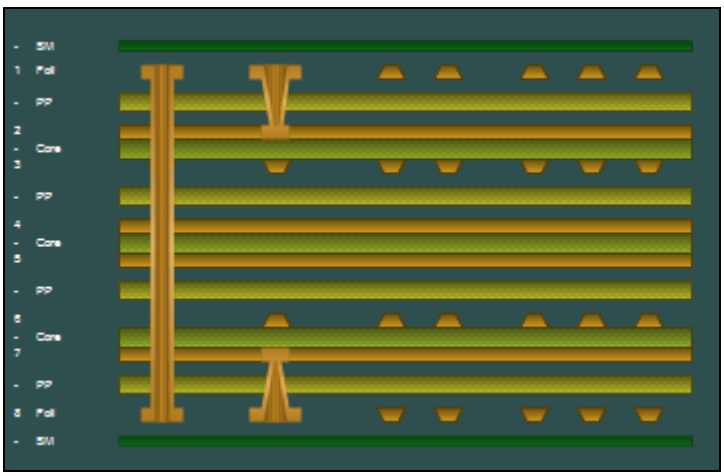
Adding drills

Select Column 1 and specify the First Electrical Layer as Layer 1 and the Second Electrical Layer as Layer 8; choose Mechanical, Through Plated with No Fill and click Add to add the first drill to the stack.



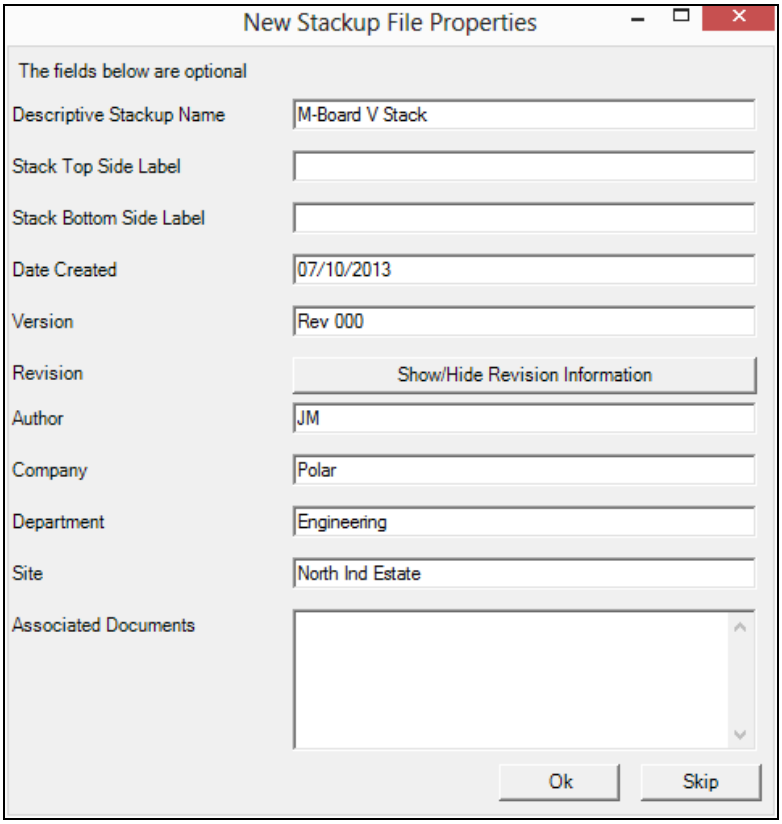
Adding microvias

Choose Column 2, specify the First Electrical Layer as 1 and the Second Electrical layer as 2; choose Laser with No Fill and click Add. Repeat the process to add another microvia to Column 2 between electrical layers 8 and 7 (shown below.)



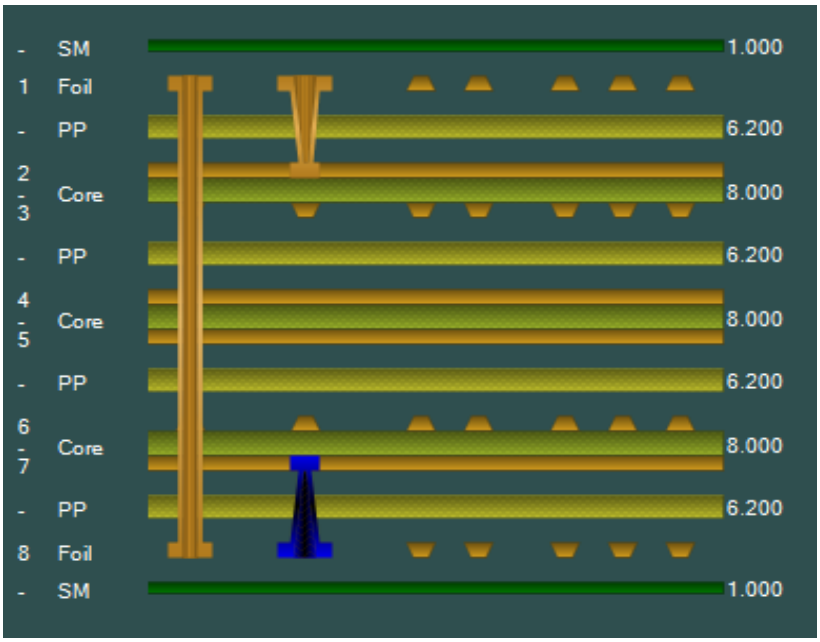
Click Finished.

The Stackup Wizard displays the New Stackup File Properties dialog; enter the (optional) stackup properties.



Click OK to close the dialog and edit the stack. Speedstack builds the stack to achieve the specified board thickness.

Click the 2D button to assist in visualisation while editing the stack.



Use the View menu to zoom in and out of the stack.

The Stackup Editor displays summary information for the whole stack and for items within the stack as they are selected.

Stack Up Information

Field	Value
Electrical Layer Count	8
Copper Thickness	11.2000
Dielectric Thickness	48.8000
Solder Mask Thickness	2.0000
==========	==========
Stack Up Thickness	60.0000
Stack Up Thickness with Solder Mask	62.0000
==========	==========

Selected Item Information : Drill

Field	Value
First Electrical Layer No	8
Second Electrical Layer No	7
Mechanical Drill	False
Laser Drill	True
Fill Type	No Fill
Data Filenames	
Hole Count	0
Different Hole Sizes	0
Minimum Hole Size	0.001
Minimum Allowable Hole Size	15.2000

Editing the stack

With the “virtual” stack in the Stack Editor the stack can be changed as required.

Changing material properties

To change the properties of a material, right click the material in the stack and choose Properties; fill in the text fields with the associated information and click Apply. Most material properties can be changed, including the material descriptions, base and finished thickness, dielectric constants, drill parameters along with the graphical colours.

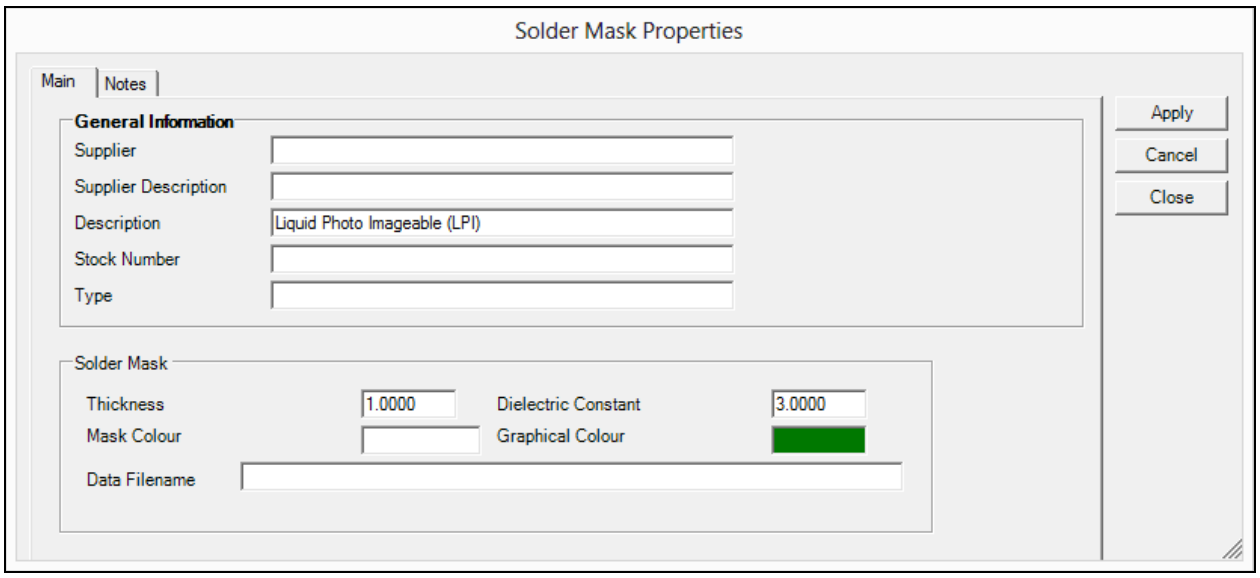
Choosing Symmetrical mode

Symmetrical mode

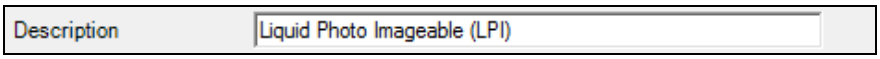
Stackups are often designed symmetrically to prevent warping and twisting – using similar materials in the top and bottom halves of the stack. Clicking the Symmetrical button will toggle the Symmetrical mode on or off. In Symmetrical mode the stack editing functions will process materials in the upper and lower halves of the stack simultaneously.

Changing the material description

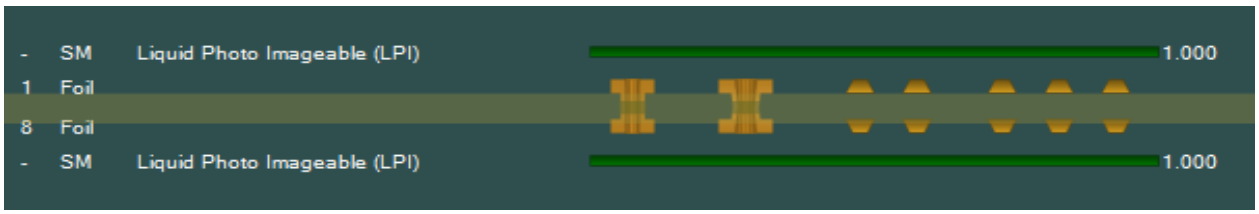
In this example stack, ensure symmetrical mode is selected then right click the solder mask material in the stack to display the Solder Mask Properties dialog.



Change the Solder Mask Description to Liquid Photo Imageable (LPI).

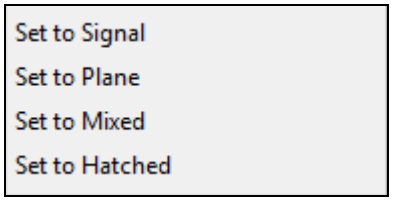


The change on the Description in both solder masks is reflected in the Editor window.



Changing electrical layers

Electrical layer types may be changed from plane to signal, mixed and hatched. Right click the layer to be changed and choose from Signal, Plane, Mixed or Hatched.

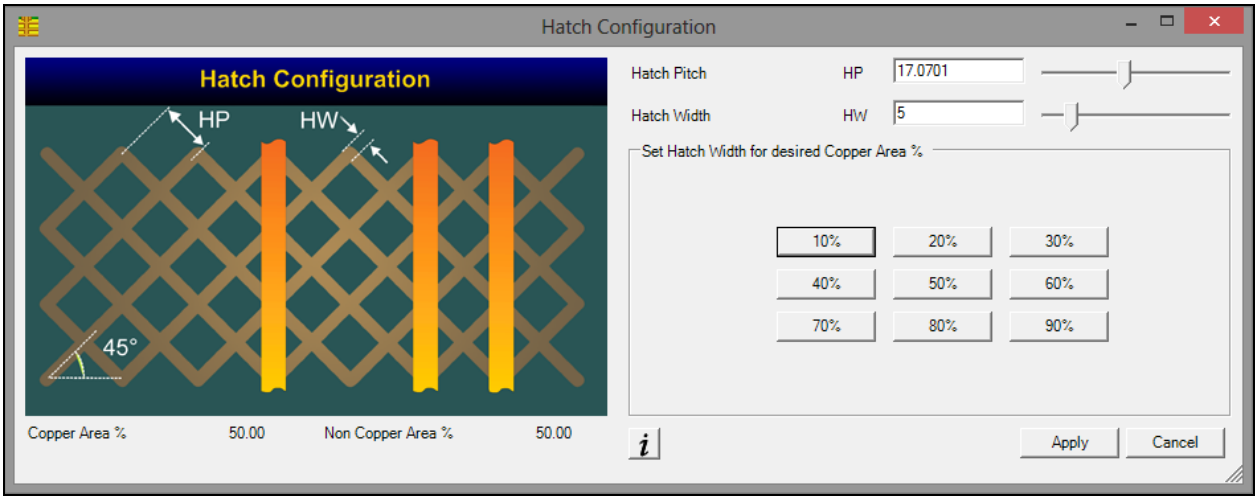


Speedstack will take the designated layer type into consideration when adding controlled impedance structures.

Setting hatched planes

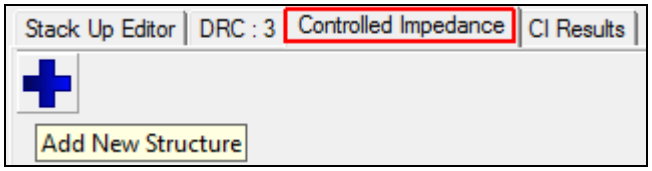
Set Layer to Hatched Plane

With the XFE option Speedstack supports hatched planes, implementing the same crosshatch calculation technique used in the Si8000m / Si9000e. If a crosshatch plane is required click Set Layer to Hatched Plane –use the Hatch Configuration dialog to set hatch pitch and width or set the hatch width by percentage copper area. Click Apply.

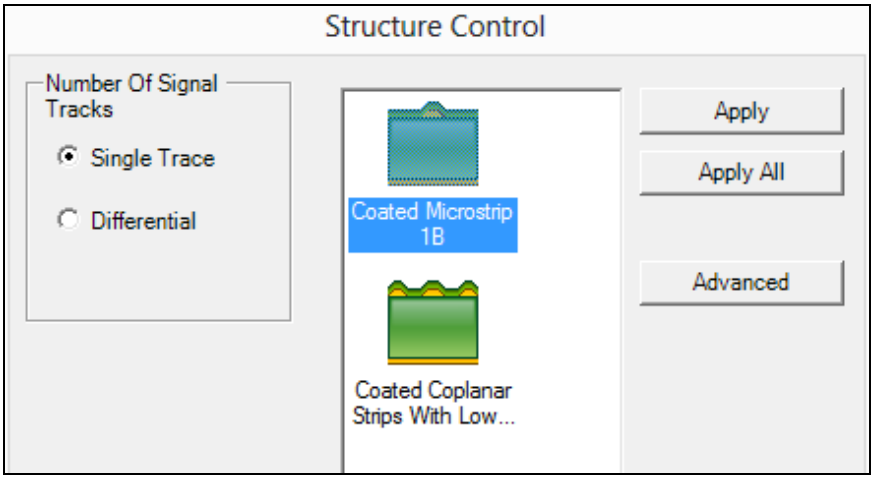


Adding controlled impedance structures

To add controlled impedance structures, click the Controlled Impedance tab, select the copper layer (in this example, Layer 1) and click the Add New Structure button.



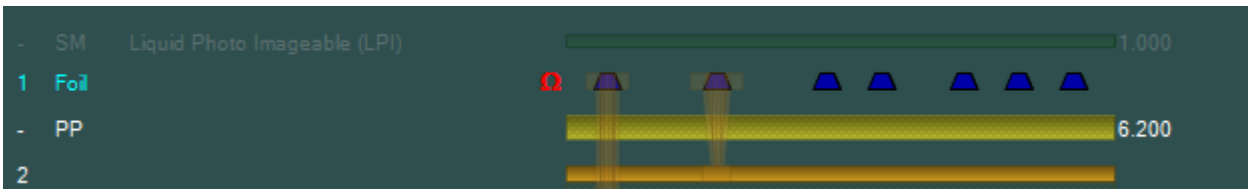
Speedstack suggests structures valid for the layer based on the plane layer types.



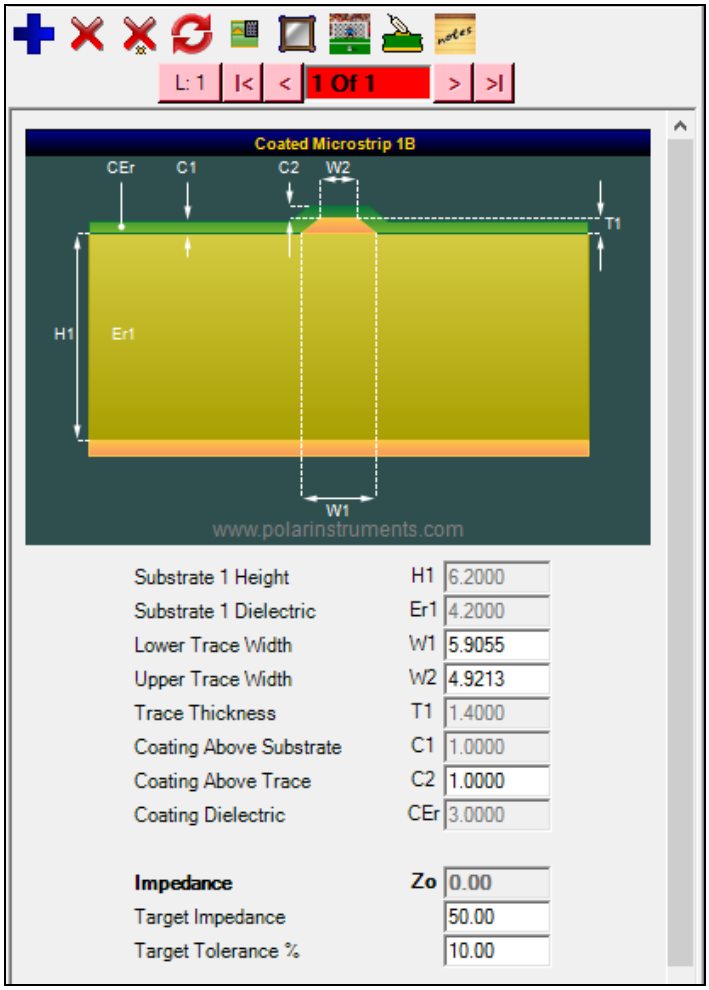
For this example, choose a 50 Ohm single ended coated microstrip; leave the tolerance at 10%; click Apply then Done.

Structure on Layer

The new structure is shown in the stack, highlighting the materials employed by the structure.

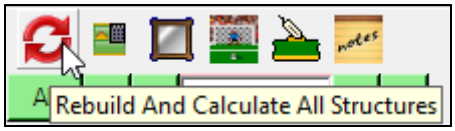


The structure also appears in the Controlled Impedance panel, along with its parameters.

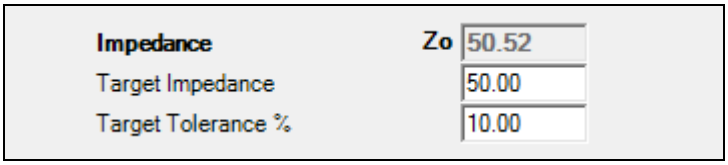


Calculating the structure impedance

Parameters calculated from the stack materials, such as the substrate height and dielectric are read only and shown greyed out; other parameters may be edited. If the editable parameters are known they may be entered directly. For example, modify W1 to read 10.5 and W2 to read 9.5 and click the Rebuild and Calculate All Structures



The impedance is calculated as 50.52 Ohms

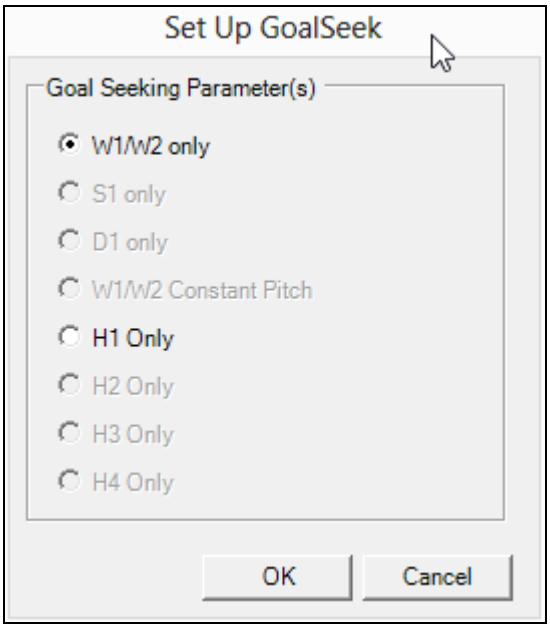


Goal Seeking the target impedance

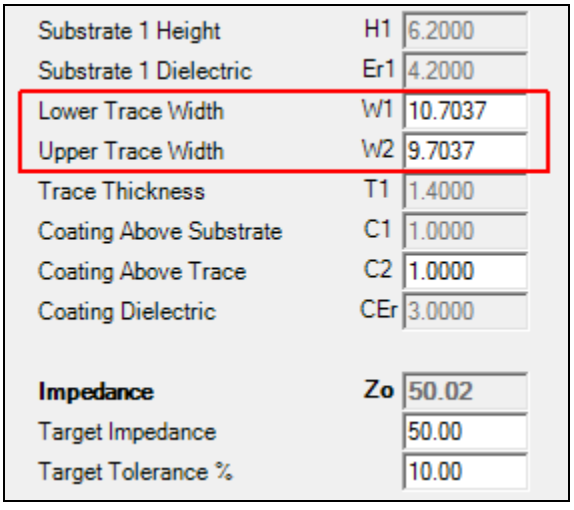
Goal Seek button

Speedstack can adjust one or more structure parameters to achieve a specified target impedance. Leave the Target Impedance at 50 Ohms and click the Goal Seek button

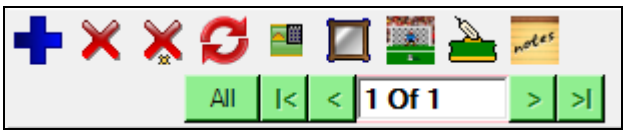
From the Set Up Goal Seek dialog choose W1/W2 only



Click OK – Speedstack adjusts trace width (below) to achieve the target 50 Ohm impedance.



With the impedance in tolerance the navigation buttons display green.



Mirroring structures

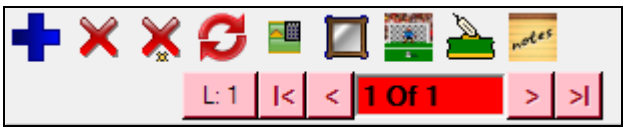
This example stack is symmetrical so structures may be copied to the lower half of the stack (i.e. on the lower outer layer.) Click Mirror Structures if Stack Symmetrical.

The impedance structure on Layer 1 is copied to Layer 8.

Rebuilding the stack

During stack editing changes to the stack (for example, inserting prepreg materials into a layer or altering the existing material thickness) will affect the impedance value of one or more structures. If Speedstack senses that an impedance structure has changed it issues a Rebuild alert.

Click Rebuild and Calculate All Structures – Speedstack recalculates the impedance for the new parameters. If the impedance value is out of tolerance the structure browse control changes colour to red.



Virtual Material mode allows the designer to experiment with material properties to examine the effects on impedance structures of different trace widths or dielectric heights, etc. Materials may be added, moved, copied, pasted or removed and the properties of materials changed – Speedstack will sense the changes and allow the “generic” stack to be rebuilt and recalculated.

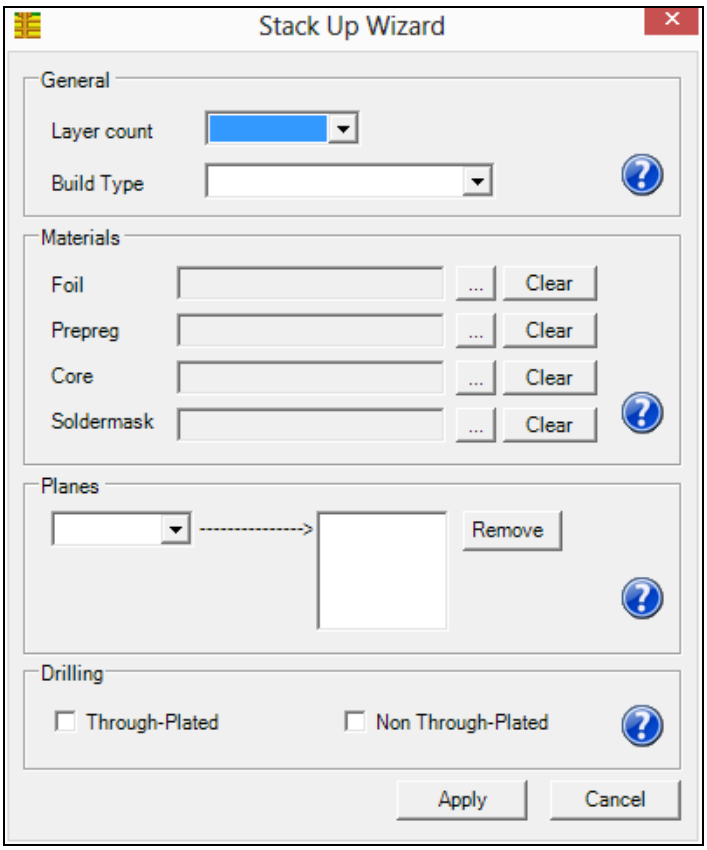
Creating and editing stackups (Material Library mode)

This section describes creating stackups using the Material Library mode. Stackups may be created manually using the Stackup Wizard or using the editing window. Ensure Tools| Virtual Material Mode is toggled Off.

Using the Stackup Wizard

Stackup Wizard button

The Stackup Wizard guides the user through the process of creating complex stackups in only a few steps. Click the Stackup Wizard button or choose Stackup Wizard from the File|New sub menu. The stackup editing window is cleared and the Stackup Wizard displayed.



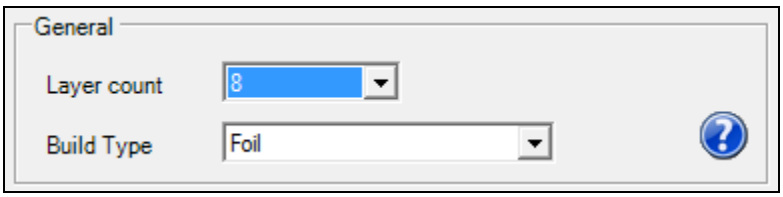
Using the Wizard the user can specify the layer count and build type, stackup materials, planes and drill types in a single operation.

Electrical layer count

Begin by specifying the electrical layer count — up to 64 electrical layers may be specified. Choose the number of layers from the drop down list box.

Build type

Choose the build type (Foil or Core) from the drop down list box. Core builds contain only core materials; most builds will be foil builds — containing internal layers of cores with two outer foils.

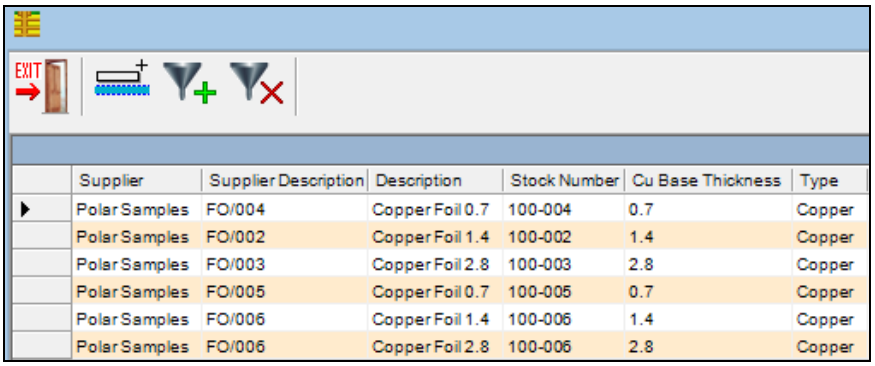


Choosing stackup materials

Note; if Core build type has been specified the Foil material control will be disabled.

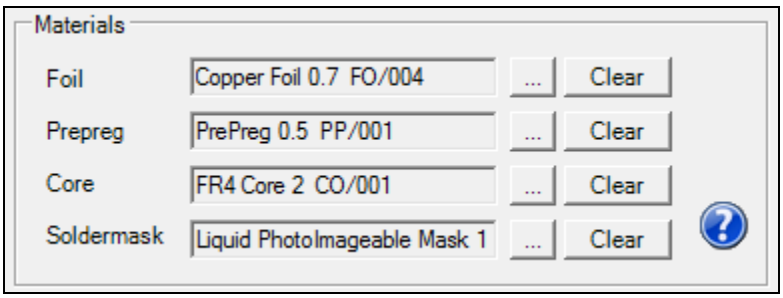
Adding layers

To include a foil layer click the Foil Add Material button; the library of foil materials is displayed. Choose the foil material from the list and click the Add Material Above button; the material is added as a foil layer to the stackup.



Supplier	Supplier Description	Description	Stock Number	Cu Base Thickness	Type
Polar Samples	FO/004	Copper Foil 0.7	100-004	0.7	Copper
Polar Samples	FO/002	Copper Foil 1.4	100-002	1.4	Copper
Polar Samples	FO/003	Copper Foil 2.8	100-003	2.8	Copper
Polar Samples	FO/005	Copper Foil 0.7	100-005	0.7	Copper
Polar Samples	FO/006	Copper Foil 1.4	100-006	1.4	Copper
Polar Samples	FO/006	Copper Foil 2.8	100-006	2.8	Copper

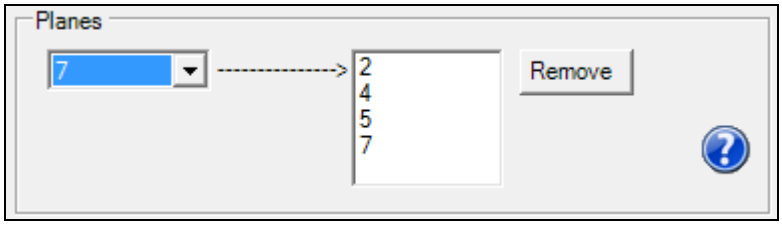
Repeat the procedure for prepreg and core materials and the (optional) solder mask layers. Use the Clear button to remove a layer from the stackup.



Stackup materials selected

Nominating power planes

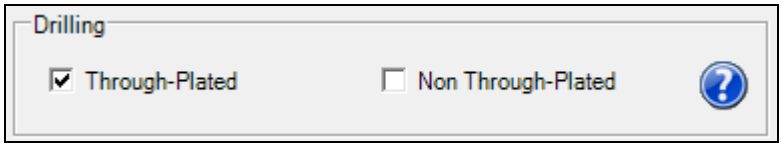
Use the drop down list box to specify that a plane should be a power plane. Select all planes as required. To remove a power plane from the list select the plane number from the list and click Remove.



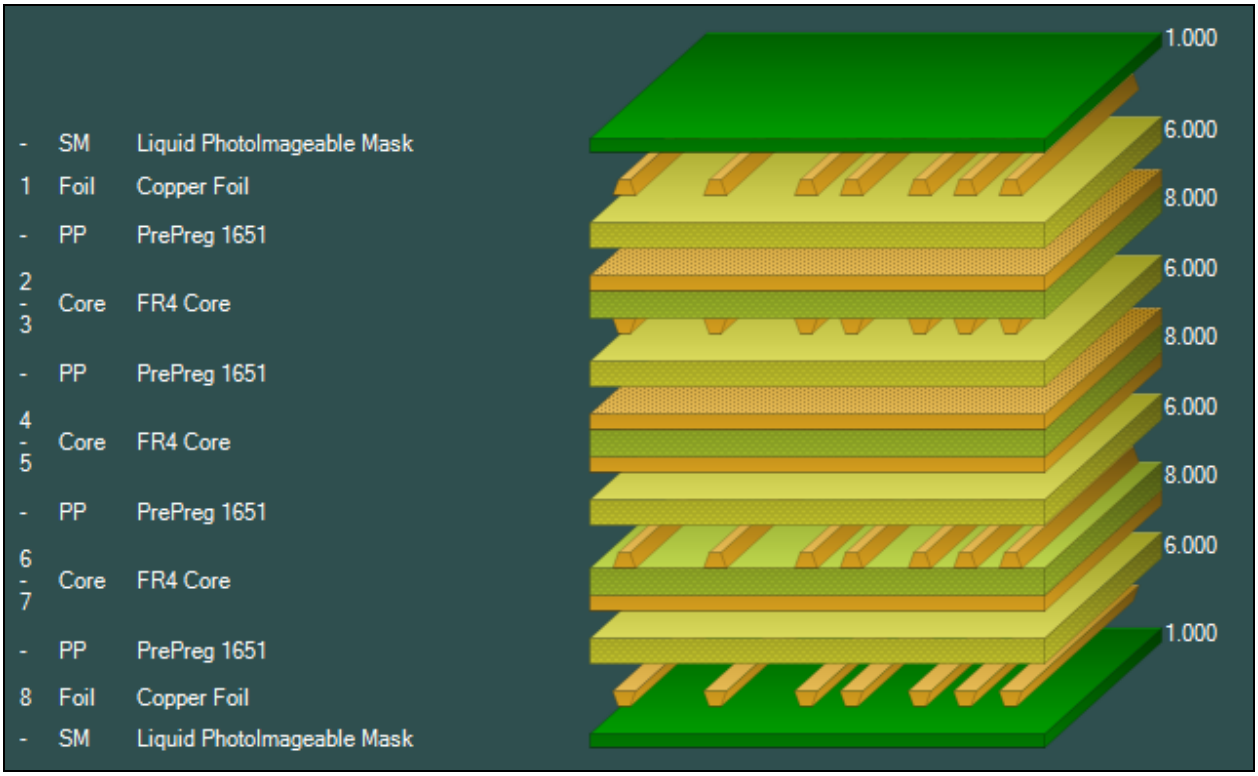
Layers 2,4, 5 and 7 specified as power planes

Adding drill information

To add a drill between electrical layer 1 and the last layer click the Through-Plated and Non-Through-Plated check boxes as required.



With all build options specified click Apply to complete the stackup. The finished stackup appears in the Editor window.

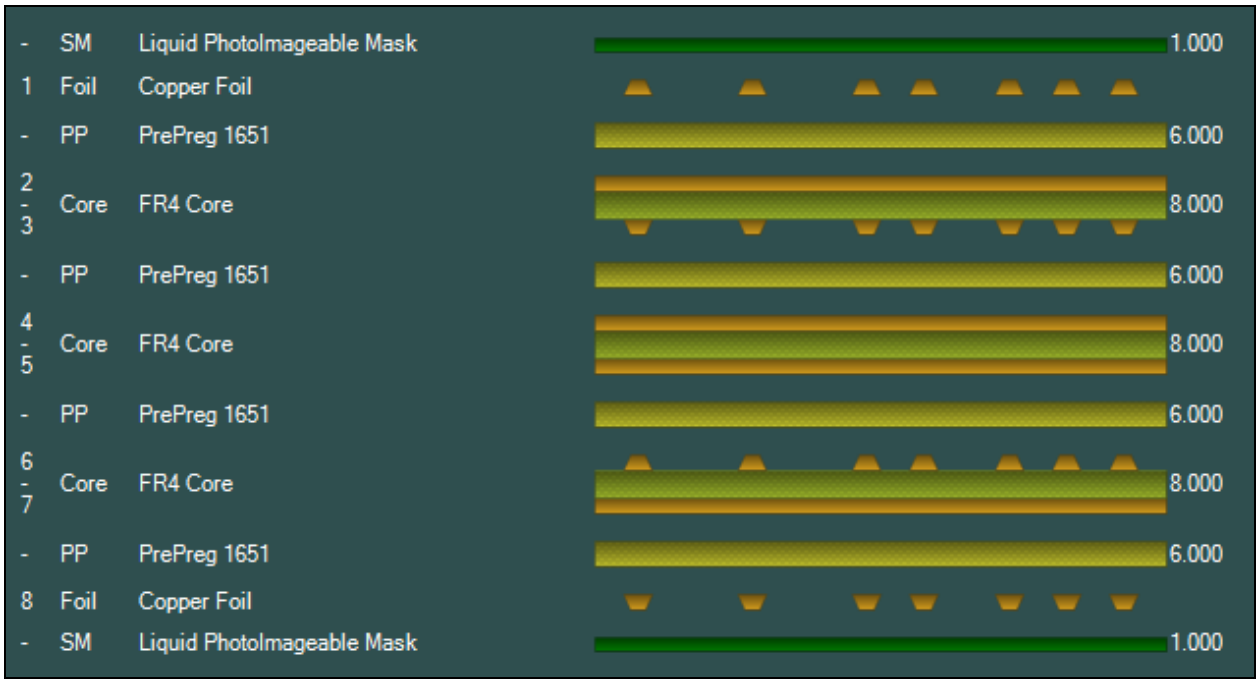


Summary information is shown in the Status Bar.

See 2D View

Changing the Stackup view

For many editing operations changes to the stack may be easier to visualize when shown two-dimensionally. Click the See 2D View button



Filtering Materials

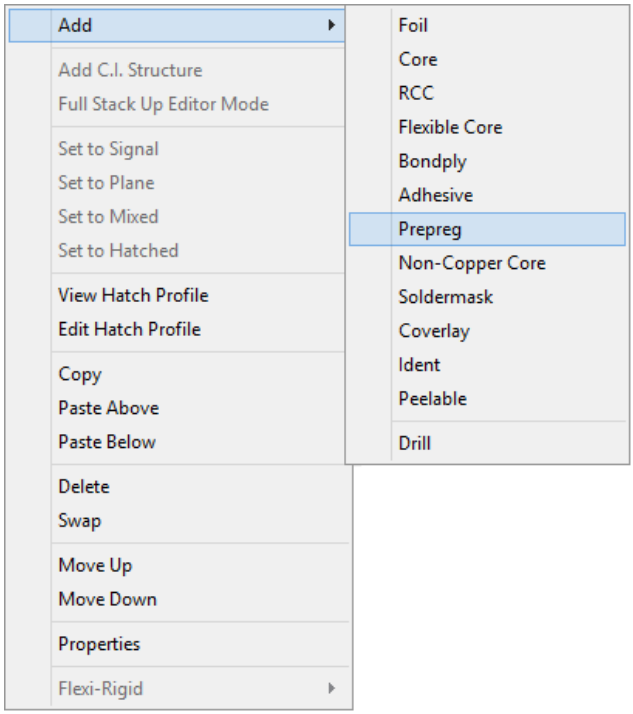
When adding or swapping materials, available materials (foils, prepregs, etc.) are listed in the associated material library dialog. Lists can be filtered for materials matching desired parameters (dielectric thickness, Er, etc.) See *Using Speedstack Materials Libraries*.

Creating stackups manually

Speedstack allows the designer to add or edit stackup layers in any order, from top to bottom, bottom to top or from the centre layer outwards. This example will create a four-layer stackup, starting at the centre core layer and adding layers above and below.

Editing the stack

When editing the stack it will probably be most convenient to right click an object in the stack and select the associated command from the context menu. The menu will reflect the commands available for the selected object — commands that are not appropriate for the object are greyed out.



Alternatively, select the object (copper, prepreg, core, etc.) with the left mouse button and choose the command from the Speedstack toolbar.

Adding layers to the stackup

Go To Materials Library

Items added to the stackup are added from the currently open materials library. Speedstack opens Program Files\Polar\Speedstack\default.mlbx if it exists; if a different library is required, open it via Go To Materials Library.

Note: Speedstack does not ship with the default.mlbx library.

For this discussion open one of the two sample library files, Speedstack Imperial.mlbx or Speedstack Metric.mlbx (stored

in the Program Files\Polar\Speedstack\Samples folder at installation time for a default installation.)

Caution: Consistency of units

When defining dimensions for a stackup (for example, layer thicknesses) ensure that all measurements are defined using the same units (mils, mm, etc.) throughout the structure and its libraries.

Note: the libraries supplied for these examples are preloaded with sample data only.

Click the File|New command to clear the stackup screen and notes and information text areas.

Click the File|Save Stackup or Save Project command to save the stackup or project. Users are recommended to save stackups or projects frequently during the stackup creation process to avoid data loss. Stackup files, project files and library files should be backed up to a secure location.

Adding a core layer

Click the Add Layer Material button and choose Core…the Core library is displayed

The Core library contains full details of the core material, including base and finished thicknesses, dielectric constant, and upper and lower copper thicknesses.

Supplier Description	Description	Stock Number	Dielectric Base Thickness	Dielectric Finished Thickness	Dielectric Constant	Upper Cu Base Thickness	Lower Cu Base Thickne
CO/001	FR4 Core 2	400-001	2	2	4.2	0.7	0.7
CO/002	FR4 Core 2	400-002	2	2	4.2	1.4	1.4
CO/003	FR4 Core 2	400-003	2	2	4.2	2.8	2.8
CO/004	FR4 Core 3	400-004	3	3	4.2	0.7	0.7
CO/005	FR4 Core 3	400-005	3	3	4.2	1.4	1.4

Click on any of the column buttons to sort the library list by the selected column.

Add Material above

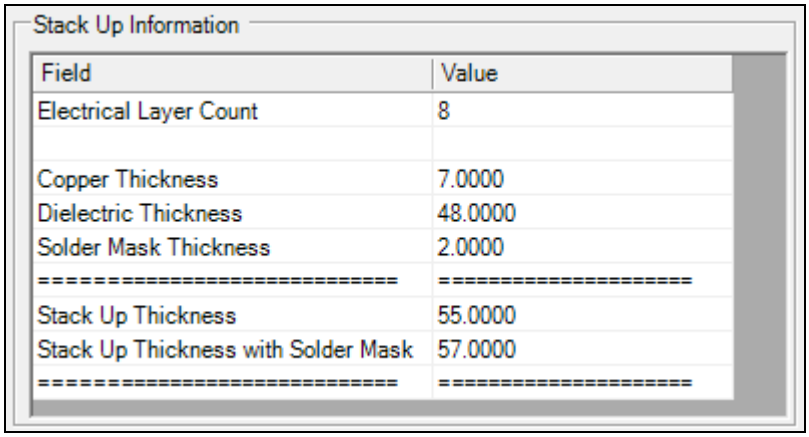
Choose a core type from the list of cores and click the Add Material Above button. The core is added to the stackup screen. When editing a stack this button adds a core above the selected layer.

Stackup core layer

Add Material below

Layers may also be added below the selected layer. The Add Material below button adds a core below the selected layer.

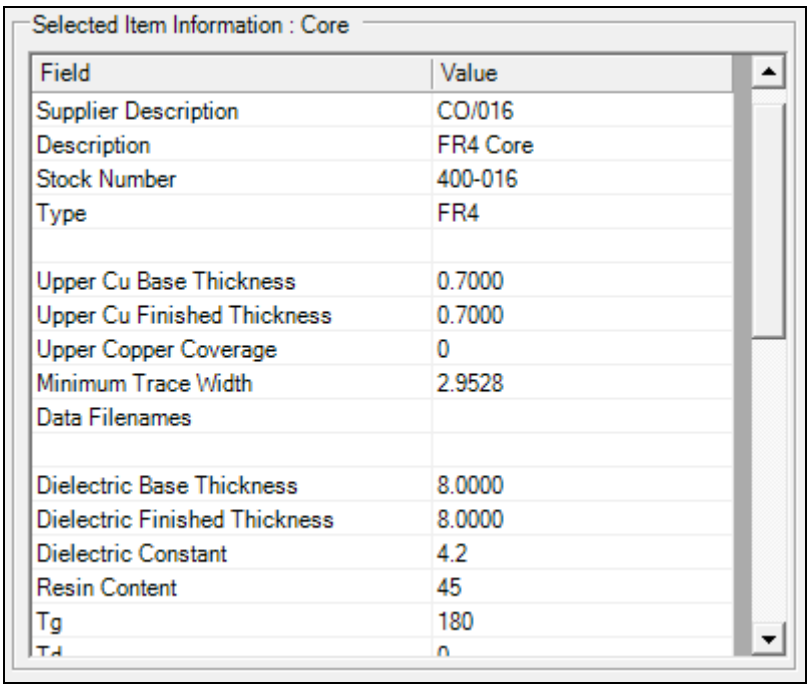
As each layer is added the stackup information table is updated to reflect the current status of the stackup.



Stackup information table

Note: The Stackup Information is printed in red when the stack thickness is outside its tolerance.

With the core selected, the Selected Item table displays the properties of the core.



Core layer information

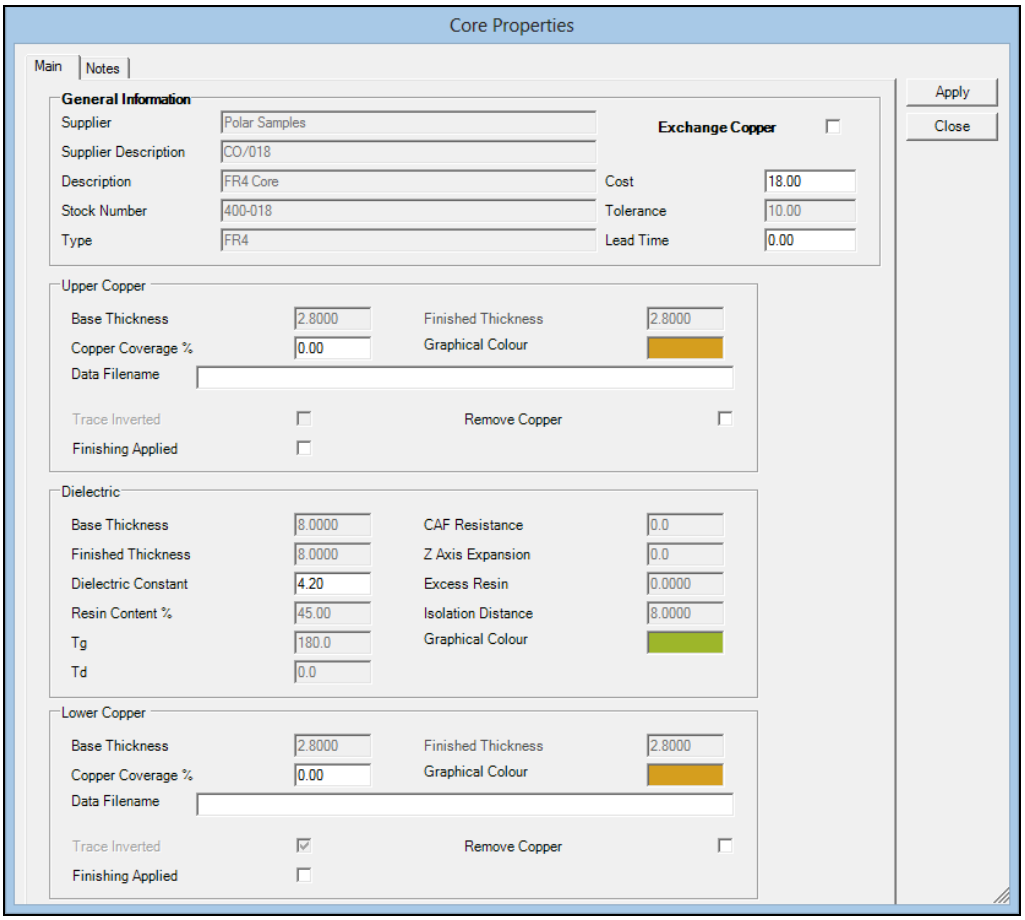
To observe the properties of any material, click the material in the stack and read off the properties in the Selected Item Information panel.

Editing the selected layer properties

To change the properties of the selected object (for example, to modify the dielectric constant or the value for the finished thickness of the dielectric), right click the object in the stackup and choose Properties from the shortcut menu; in this example the Core Properties dialog is displayed.

Note that the Enable Finishing setting in the Tools|Set Stackup Thickness/Finishing Options dialog must be unchecked to enable the Finishing Thickness to be specified manually.

Change the value to the corrected value and click Apply.



Adding data file names

If available, add the data file name(s) to the upper and lower copper layers and click Apply.

Close the dialog when all changes are completed.

Changes will be reflected in the Stackup Information table.

Changing a layer function

In this example both the signal layers above and below the core dielectric are changed to planes.


Set Layer to Plane

Click the lower signal layer and click the Set Layer Plane button. Repeat for the upper signal layer.

The changes are reflected in the stackup window

Exchanging layers

To change just the core dielectric (leaving the copper layers unaffected), right click the core material (for example the FR4 in the graphic above) and choose Swap from the context menu or left click the core material and click the Swap Selected Material button. Choose the new core type from the library and click the Swap button. The layer properties will change to reflect the new material and changes appear in the Stackup Information table.

Swap Selected Material

Adding prepreg layers

With the core selected, click the Add Material button and choose Prepreg…; the Add Prepreg library is displayed.

Add Material

Supplier Description	Description	Stock Number	Dielectric Base Thickness	Dielectric Finished Thickne	Dielectric Constant	Resin Content	Tg
PP/001	PrePreg 1080	300-001	3	3	4.2	60	180
PP/002	PrePreg 3080	300-002	3	3	4.2	60	180
PP/003	PrePreg 3113	300-003	4	4	4.2	53	180
PP/004	PrePreg 1651	300-004	6	6	4.2	47	180
PP/005	PrePreg 7628	300-005	7.9	7.9	4.2	45	180
PP/006	PrePreg 106	300-006	2	2	4.2	60	180

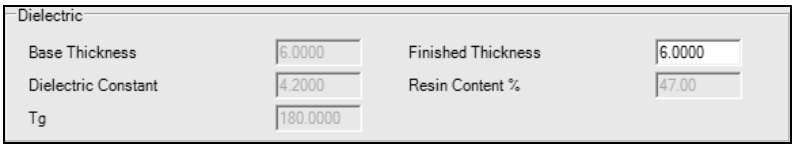
The Prepreg library contains details of the prepreg material, including the prepreg's base and finished thickness and dielectric constant.

Choose the Prepreg material from the database and click the Add Material Above button.

Add Material Above

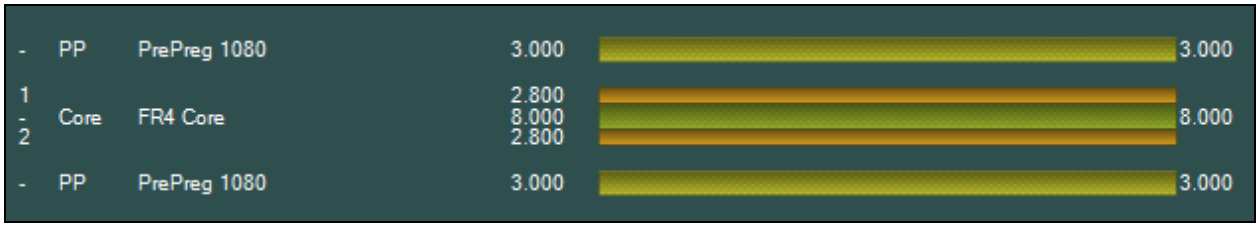
The prepreg layer is added above the core.

To change the properties of the prepreg material right-click the layer and choose Properties from the short cut menu. For example, the value for Finished Thickness can be modified to reflect the effects of the pressing process.



Select the Core material and click Add Material|Prepreg to display the prepreg library and click the Add Below button. The layer of prepreg is added below the core.

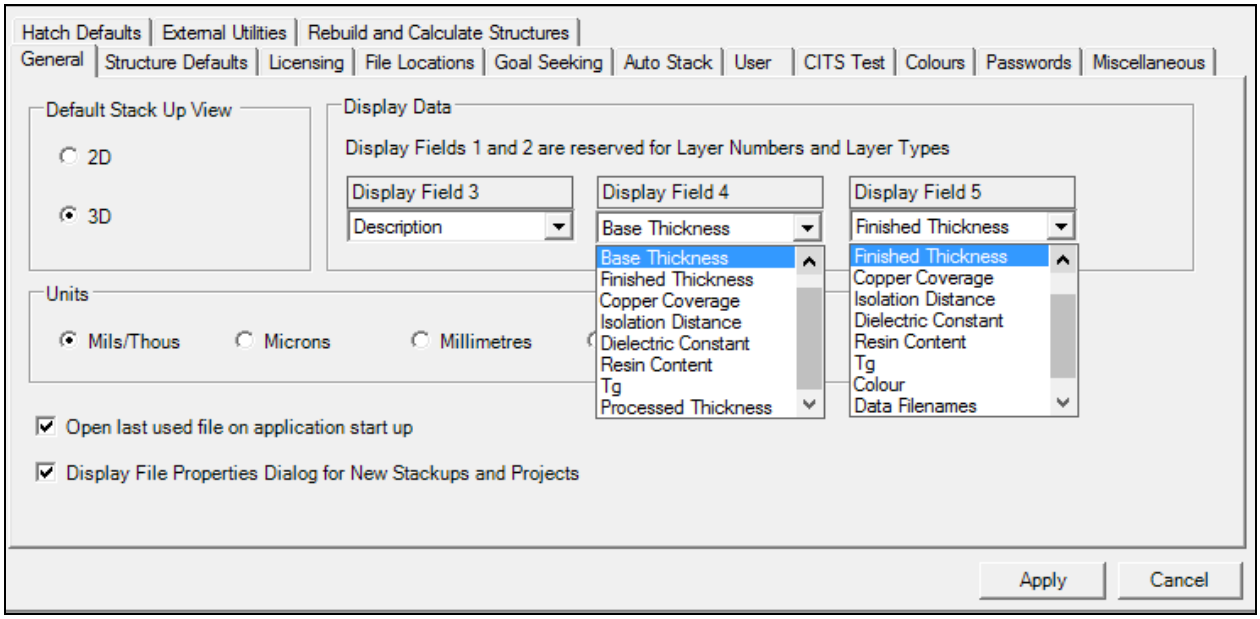
Add Prepreg Below



Modify the properties as necessary.

Choosing the Display Data fields

The Speedstack Stack Editor provides a range of useful data fields for optional display alongside each material. Base and Finish (Display Field 4) refer to thicknesses and weights and appear to the left of the stackup graphic.



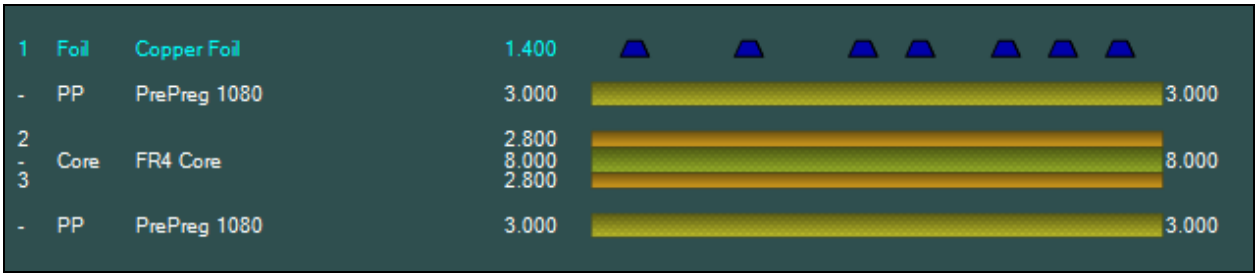
Display Field 5 appears to the right of the stackup graphic. Choose the data of interest from the drop down lists.
Note: Processed Thickness is the Finished Thickness for copper layers and Isolation Thickness for dielectric layers.

Adding a foil layer

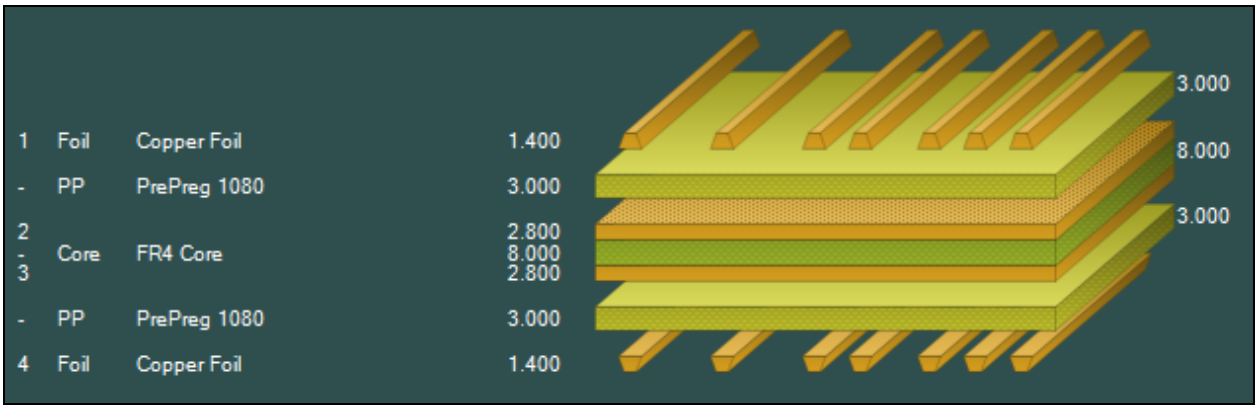
Select the upper layer of prepreg and click the Add Layer Material button and choose Foil to display the copper foil library.

Supplier Description	Description	Stock Number	Cu Base Thickness	Type	Cost	Lead Time
FO/001	Copper Foil	100-001	0.7	Copper	1	0
FO/002	Copper Foil	100-002	1.4	Copper	2	0
FO/003	Copper Foil	100-003	2.8	Copper	3	0

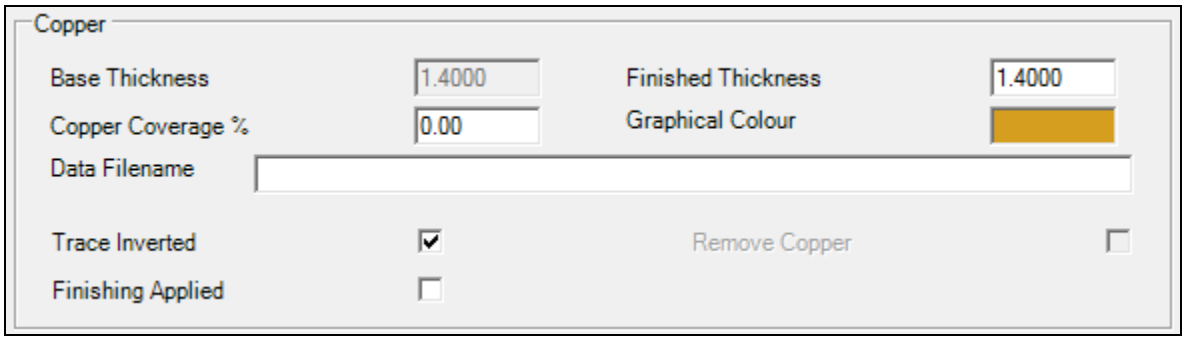
Choose the foil type and click Add Above, the copper foil layer is added above the selected prepreg layer.



Repeat the procedure for the lower prepreg layer: select the lower prepreg layer and add a layer of copper foil below the layer (shown below as layer 4 in the 3D view).



To alter the foil properties, right-click the foil layer and choose Properties. Using the Properties dialog the user can, for example, specify that the trace is shown inverted.



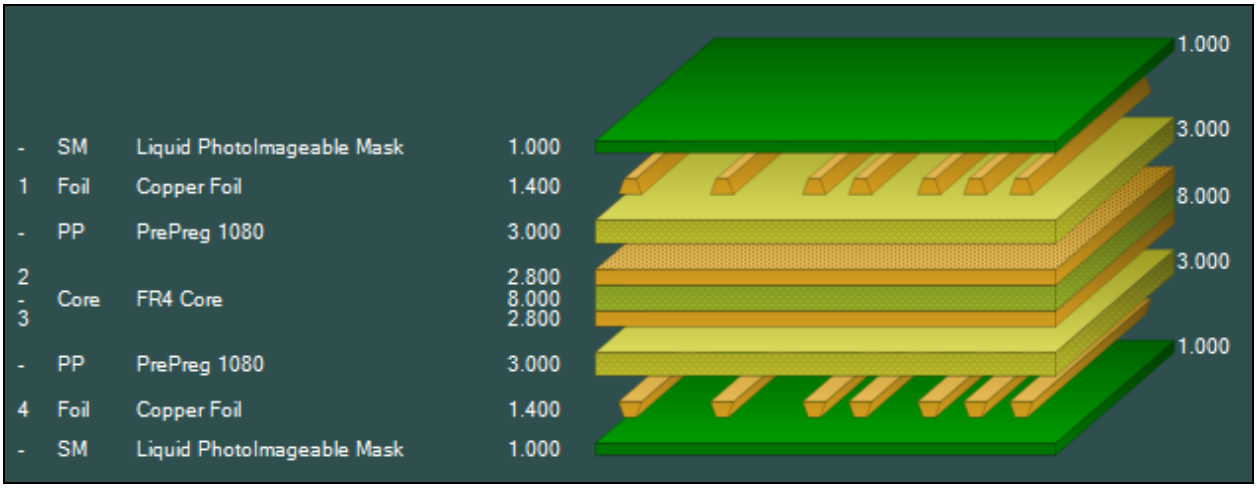
Note that the stackup is being built symmetrically about the centre layer.

Adding solder mask layers

With the upper layer of foil selected, click the Add Layer Material button and choose Soldermask to add a layer of LPI solder mask above the foil.

Supplier Description	Description	Stock Number	Mask Thickness	Dielectric Constant	Colour	Type	Cost
SM/001	Liquid PhotoImageable Mask	500-001	1	4	Green	SolderMask	0.5
SM/002	Liquid PhotoImageable Mask	500-002	1	4	Green	SolderMask	0.6
SM/003	Liquid PhotoImageable Mask	500-003	1	4	Blue	SolderMask	0.6
SM/004	Liquid PhotoImageable Mask	500-004	1	4	Red	SolderMask	1

Repeat the process for the solder mask material below the lower foil layer.

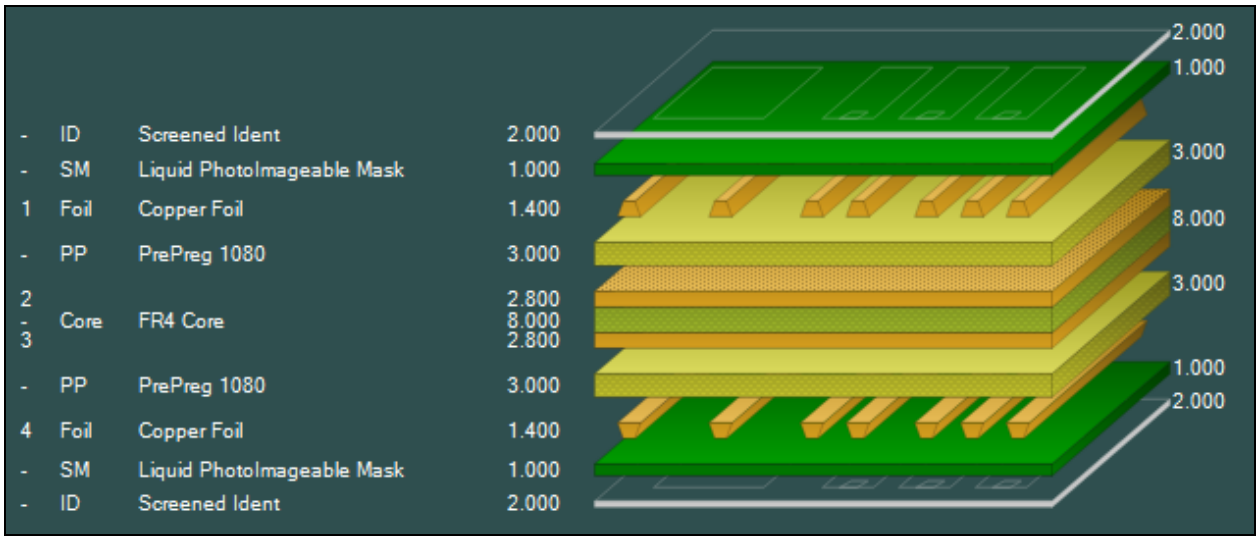


Adding the Ident layers

Select the lower LPI Soldermask layer and click the Add Layer Material button and choose Ident to add a layer of Screened Ident below the layer. The sample Ident library includes ink thickness and colour

Supplier Description	Description	Stock Number	Ink Thickness	Colour	Type	Cost
ID/001	Screened Ident	600-001	2	White	Ident	0.1
ID/002	Screened Ident	600-002	2	Yellow	Ident	0.1
ID/003	Screened Ident	600-003	2	Black	Ident	0.1

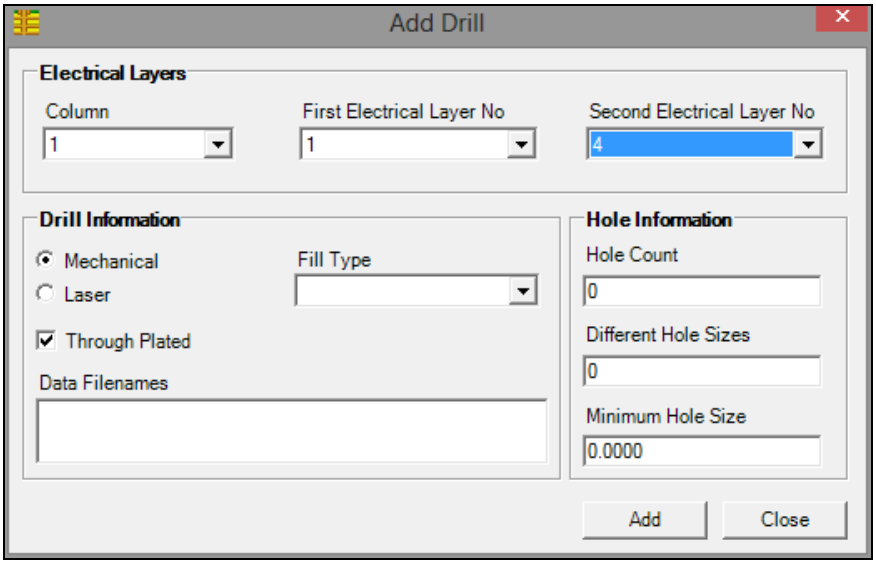
Repeat for the upper layer.



Adding a drill

AddDrill

To add a drill between layers click the Add Drill button; the Add Drill dialog is displayed.



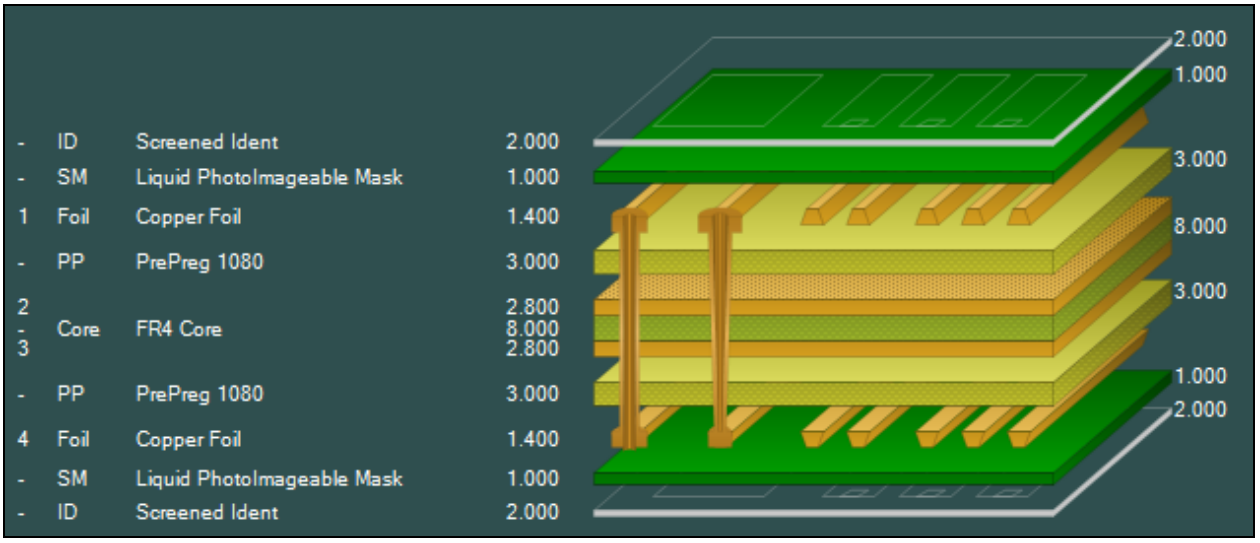
Select the column in which to place the drill.

Choose the first and second electrical layer numbers (layers 1 and 4 in the example).

Specify the drill type, mechanical or laser and whether through plated. Note that with laser drills the order of drill layers is important, e.g. layer 1 and 4 is different from layer 4 and 1. Optionally, add the NC drill data filenames.

Optionally, add the hole count, number of different hole sizes and the minimum hole size. Click Add and close the dialog. The drill information is added to the stackup. The example below contains through plated and laser drill information.

The finished stackup is shown below



Deleting a layer

To remove a layer from the stackup select the layer and click the Delete button.

Delete Selected Material

Copying a layer

Copy Selected Material

With layers defined it will often be found more convenient to copy an existing layer and paste it into the stackup than to create a new layer “from scratch”. Select the layer to be copied and click the Copy Selected Material button. Click the layer nearest the destination location and choose Paste Above or Paste Below as appropriate

Note: when modifying the stackup it may be necessary to redefine the drill information to reflect the changes.

Moving materials

Move Selected Material Up

Move Selected Material Down

To move materials within the stackup use the Move Selected Material Up and Move Selected Material Down buttons.

When a material is moved it is exchanged with the layer above or below, respectively.

Applying finishing

Apply Finishing

Reset Finishing

To apply the finished thickness factor throughout the board, click the Apply Finishing button with no material selected.

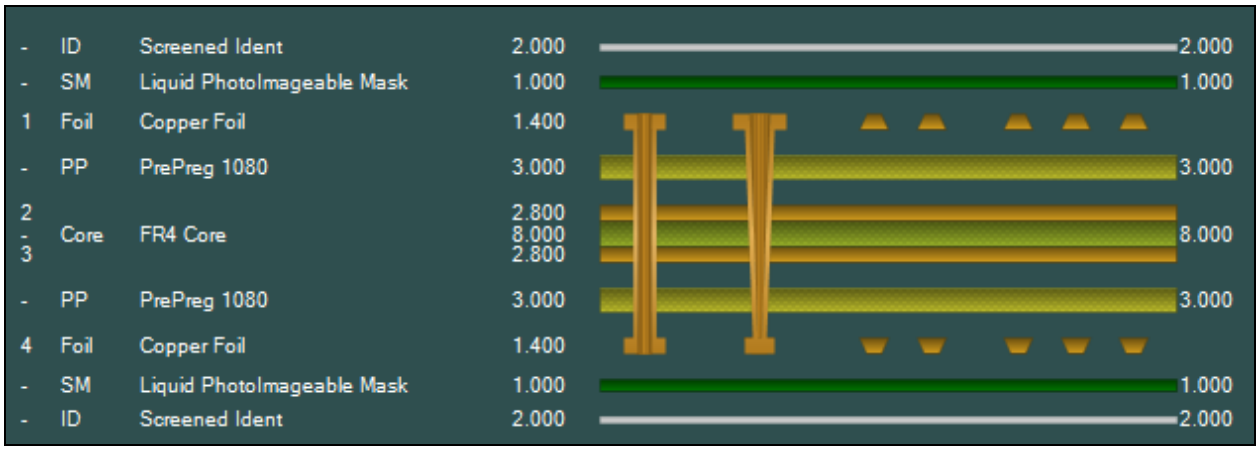
To reset the finished thickness back to the original base thickness of the materials throughout the board, click the Reset Finishing button with no material selected.

Note: when applying or resetting finishing, if a material is selected it will be necessary to specify whether finishing is to be applied to the selected material only or the whole stack.

Displaying the stackup in 2-dimensional view

See 2D View

To change the view of the stackup from its default 3-dimensional aspect, click the See 2D View button. The stackup is displayed in 2-dimensional view.



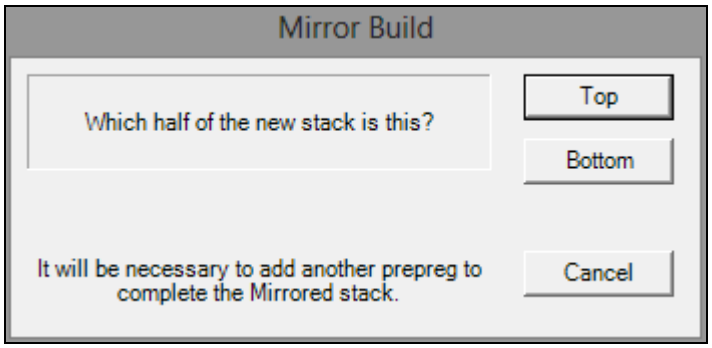
See 3D View

Click the View 3D button to restore the 3 dimensional view.

Mirror Build

Mirror Build allows the designer to consider the stack in two halves, designing and building, for example, just the top half and mirroring the structure into the lower half.

Build the top half of the stack, including any controlled impedance structures and click the Mirror Build button; specify whether the current set of layers is the upper or lower half of the stack. To maintain symmetry, Speedstack will add a layer of material as appropriate to the stack;



the stack is reflected symmetrically into the lower half.

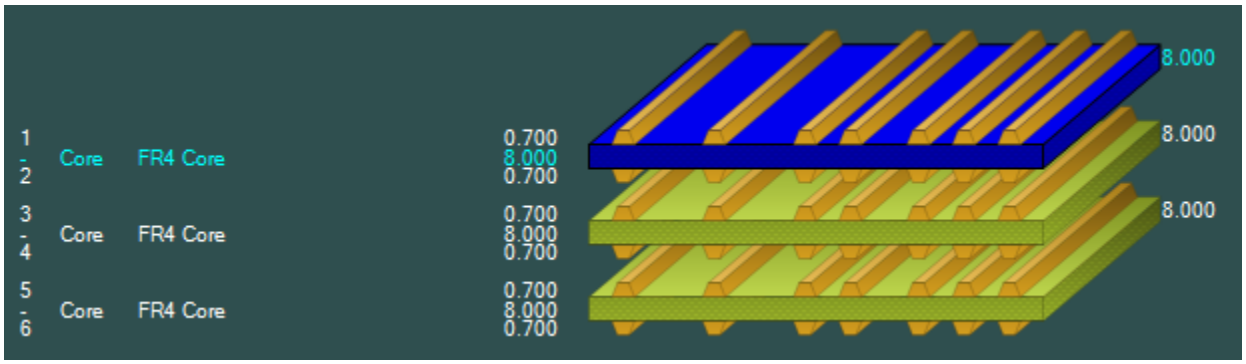
Symmetrical Build

In Symmetrical Build mode the Speedstack maintains stack symmetry as the stack designer creates or edits a stack. Changes in one half of the stack are reflected in the opposite half of the stack to ensure a symmetrical stack.

This example considers an 8-layer stack – beginning with three cores and then using Symmetrical Build.

Creating a new stack

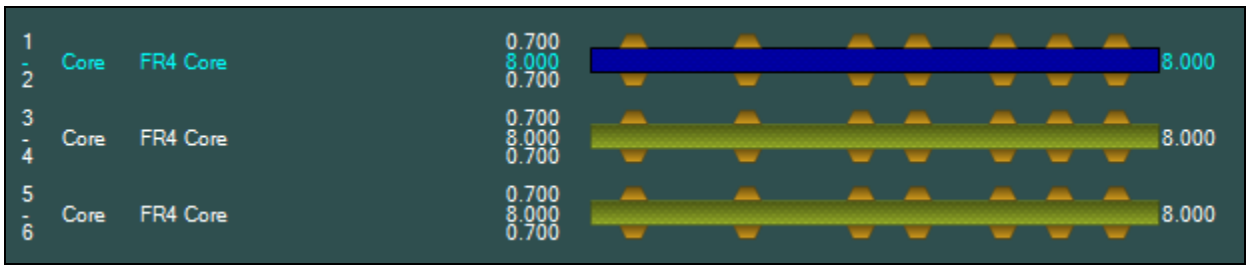
Create a new empty stackup and add three cores.



When constructing complex structures it will often be found easier to use the two dimensional aspect.

View 2D button

To change the view of the stackup from its default 3-dimensional aspect, click the See 2D View button. The stackup is displayed in 2-dimensional aspect.



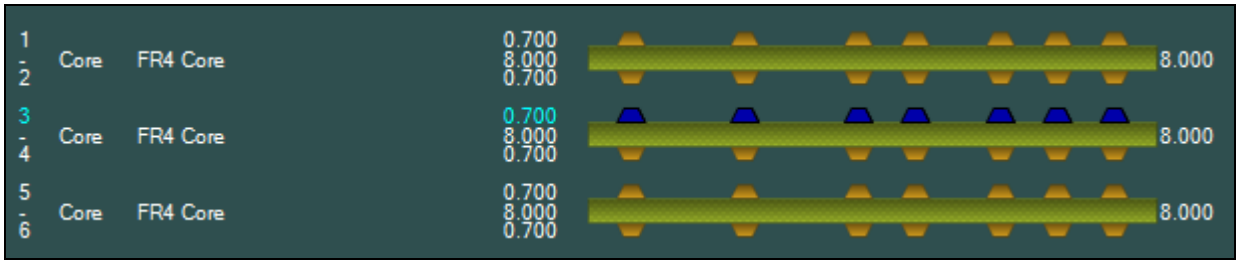
Adding a prepreg layer in Symmetrical Mode

In this example it is necessary to add prepreg layers between cores to achieve the required dimensions.

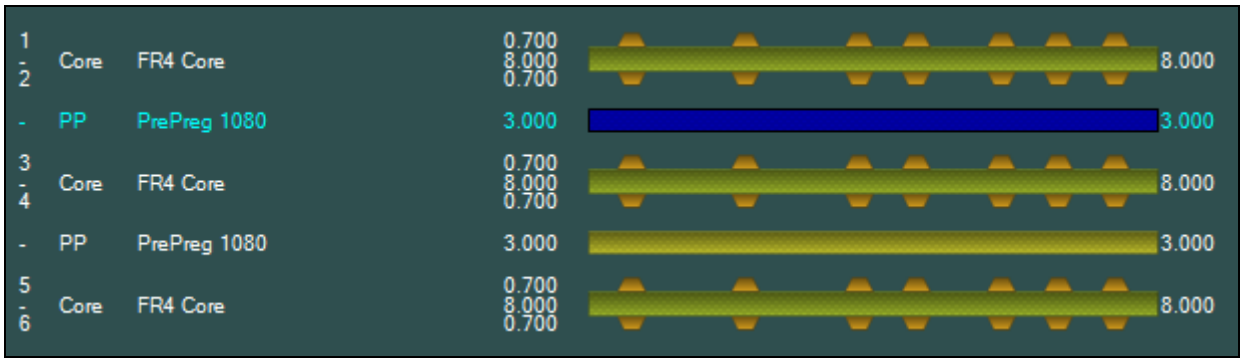
Symmetrical mode button

Switch to Symmetrical Mode and work in the top half of the stack – in Symmetrical Mode as layers are added to the top half of the stackup the Speedstack will add layers to the lower half of the stackup to maintain stack symmetry.

To add a layer of prepreg between Layers 2 and 3 select Layer 3 (the selected layer is shown highlighted in the figure below.)

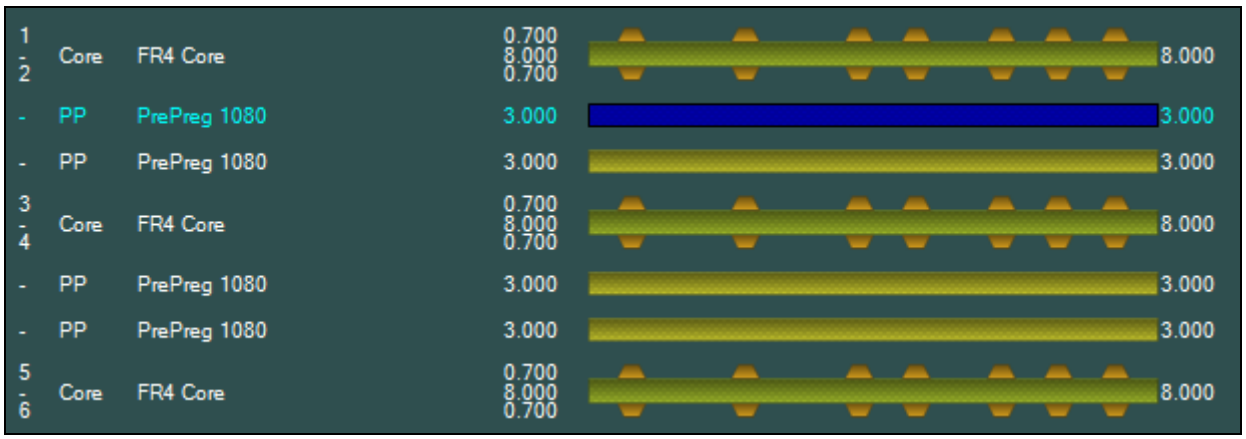


Click the Add Material button and add a layer of prepreg above Layer 3 (shown highlighted in the figure below); the prepreg layer is automatically reflected in the lower half of the structure.

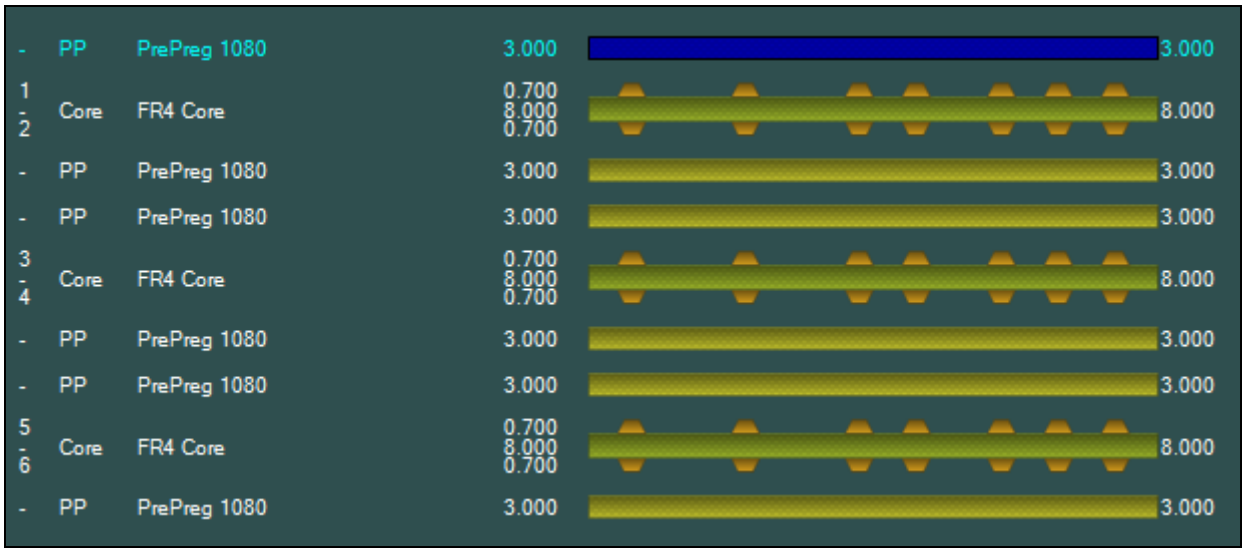


Adding a second prepreg layer

Now add a second layer of prepreg above the layer just added; the new prepreg layer is reflected in the structure below

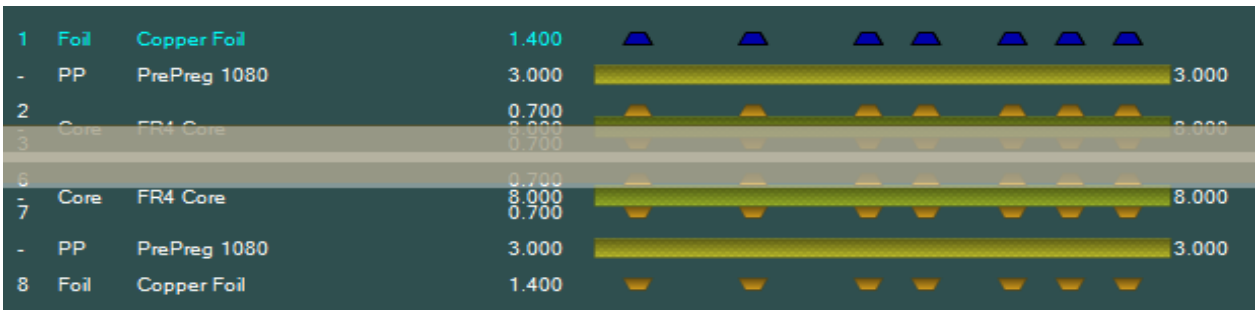


Next add a layer of prepreg above layer L1 in the upper half of the stackup; Speedstack automatically maintains stack balance by adding the corresponding layer below L6.

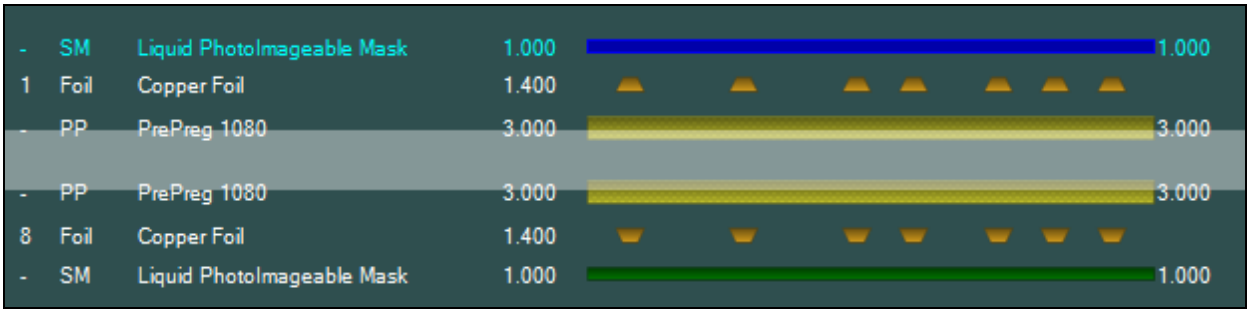


Adding foil, LPI Mask and Ident layers

Next, add a foil layer (L1 below) which is mirrored as L8; as part of the process Speedstack inverts layer L8.

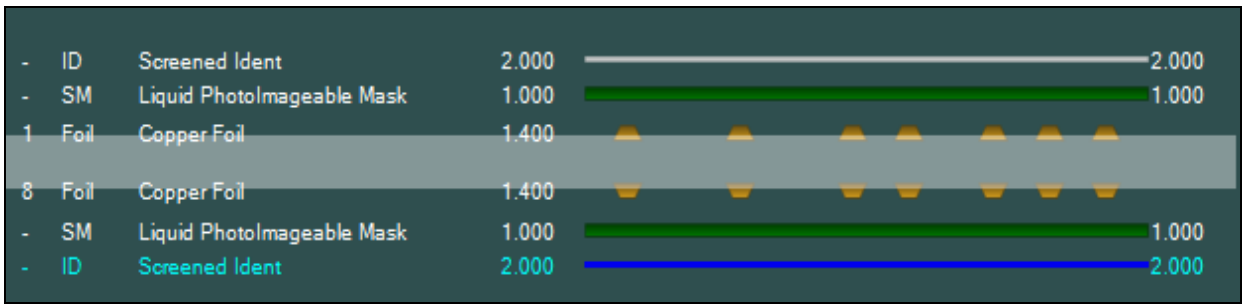


Next, LPI solder mask is applied to the top side of the stackup and reflected on the bottom side.



Ident layers (which are not considered components of electrical symmetry) will not be automatically reflected by Speedstack as they are added and must be applied separately to each side of the board.

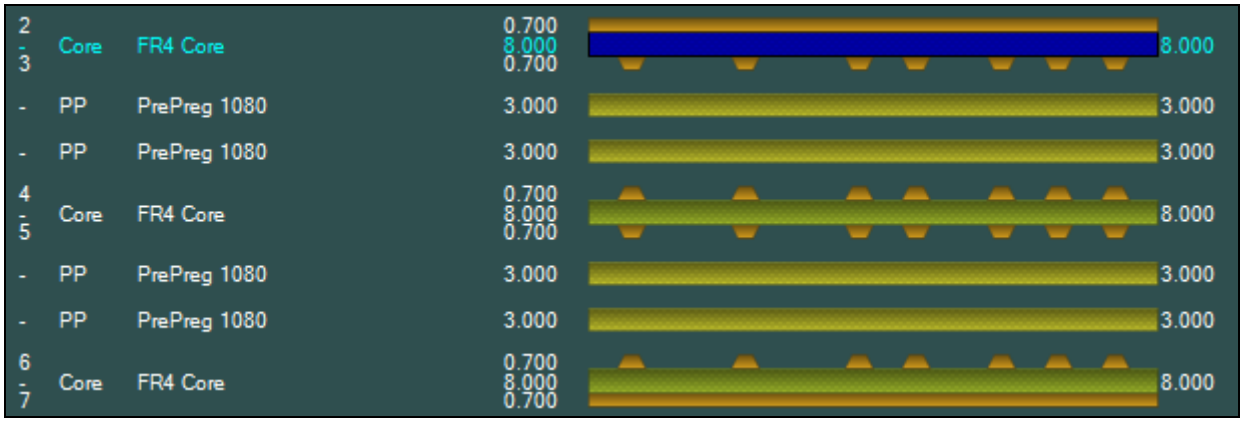
Select the upper solder mask and add an Ident material above; select the lower solder mask and add an Ident material below.



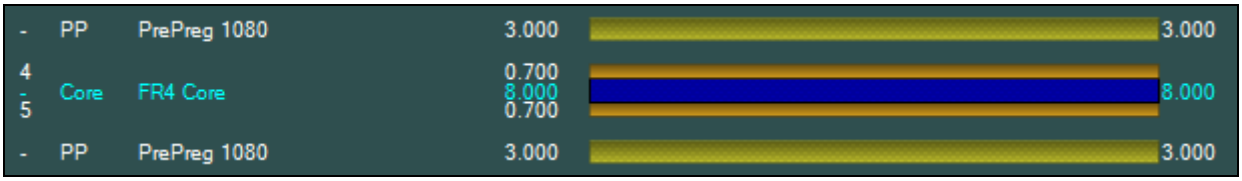
Assigning ground planes

Set Layer To Plane

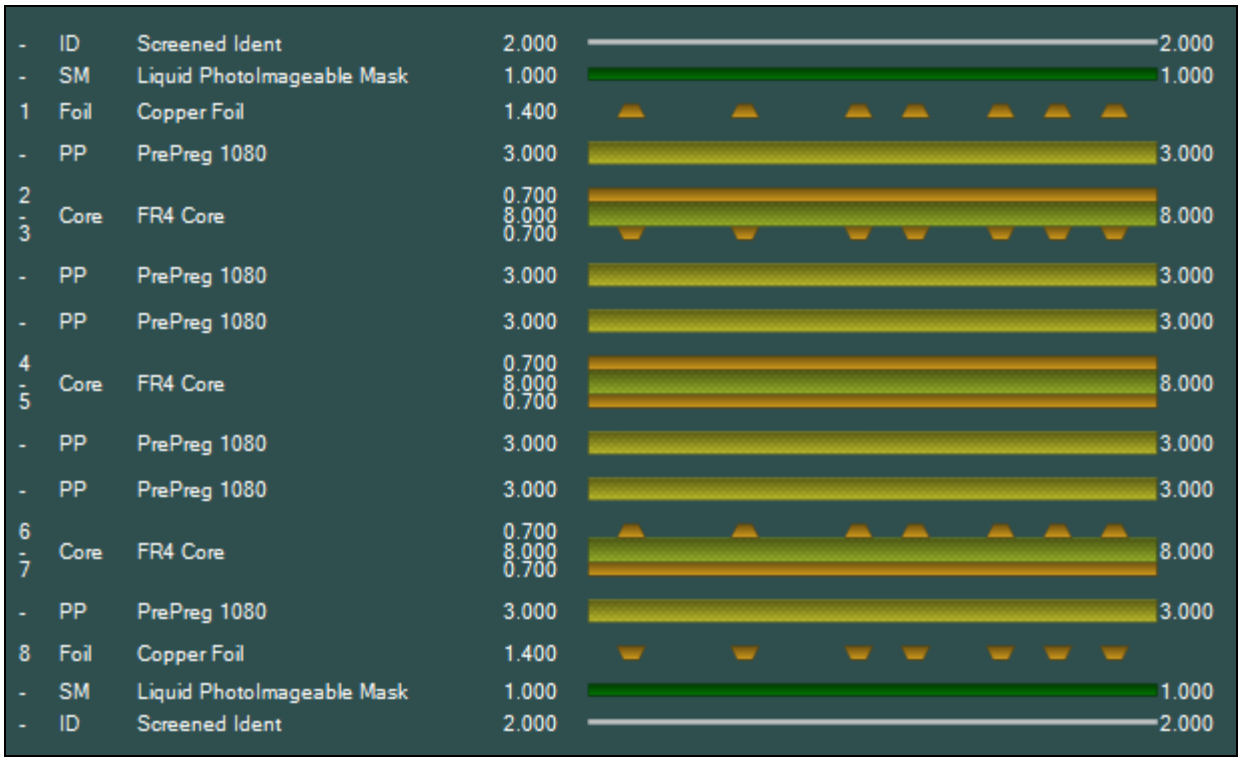
With all the material in place, assign ground planes; begin with layer L2 – it's reflected in layer L7. Right click the copper (L2) in the top core and choose Set Layer to Plane.



Repeat the process for the other ground plane layers; layer L4 is designated a ground plane, the change is reflected in L5 in the lower half of the stack.



The completed stack is shown below



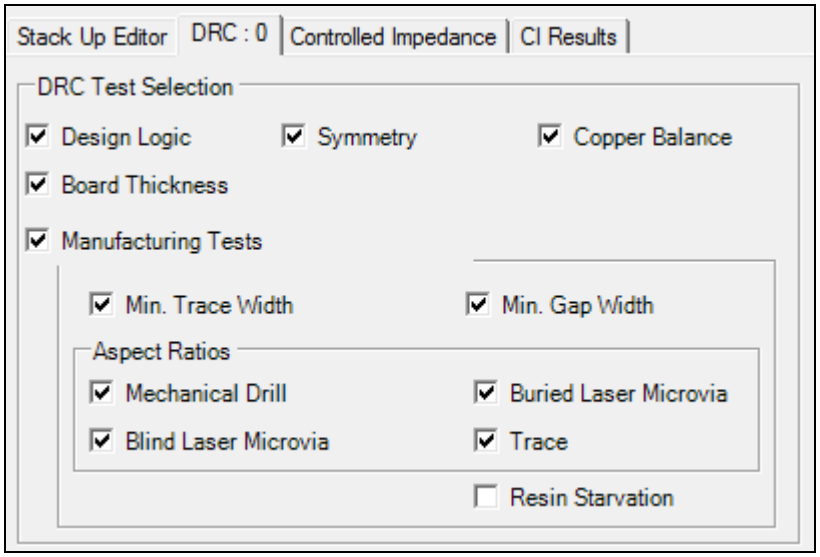
Design Rule Checking

Speedstack includes facilities to check for errors in stackup design, such as layers placed in invalid order or asymmetrical structures. The condition of the design rule checkboxes is carried over from session to session.

The Design Rule Checker (DRC) displays results in the DRC dialog. As each design rule is broken the Speedstack increments the error count on the DRC tab.

Viewing design rule errors

Click the DRC tab to view errors.



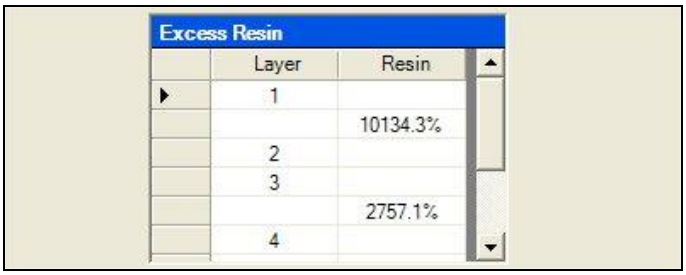
The Design Rule Checker checks include checking for:

- Two adjacent copper layers
- Resin coated copper on internal layer
- External prepreg layers
- Internal solder mask material
- Internal ident material
- Internal peelable mask
- Symmetry – different material types
- Copper not balanced
- Board thickness (if the board is outside tolerance the Stack Information in the Stack editor is displayed in red)

Manufacturing tests

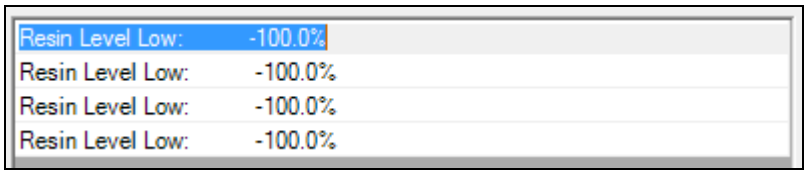
- Minimum trace width (the test is carried out when calculating controlled impedance)
- Minimum trace separation (the test is carried out when calculating controlled impedance)
- Drill aspect ratios for plated holes
- Track aspect ratio
- Excess resin test

If the Excess Resin check box is ticked values are shown as below; scroll through the layers as required

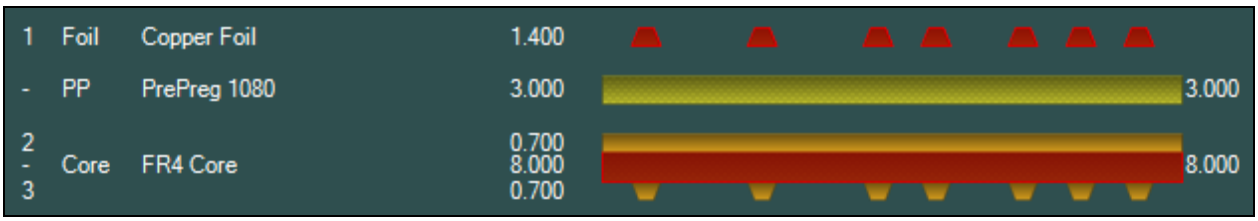


Users can choose to display all errors or to select from a combination of Design Errors, Symmetry errors and Copper balance errors, etc.; check the boxes as required.

Click on the errors shown in the list to highlight the errors in the stackup screen.



Errors are highlighted in red.



Correcting design rule errors

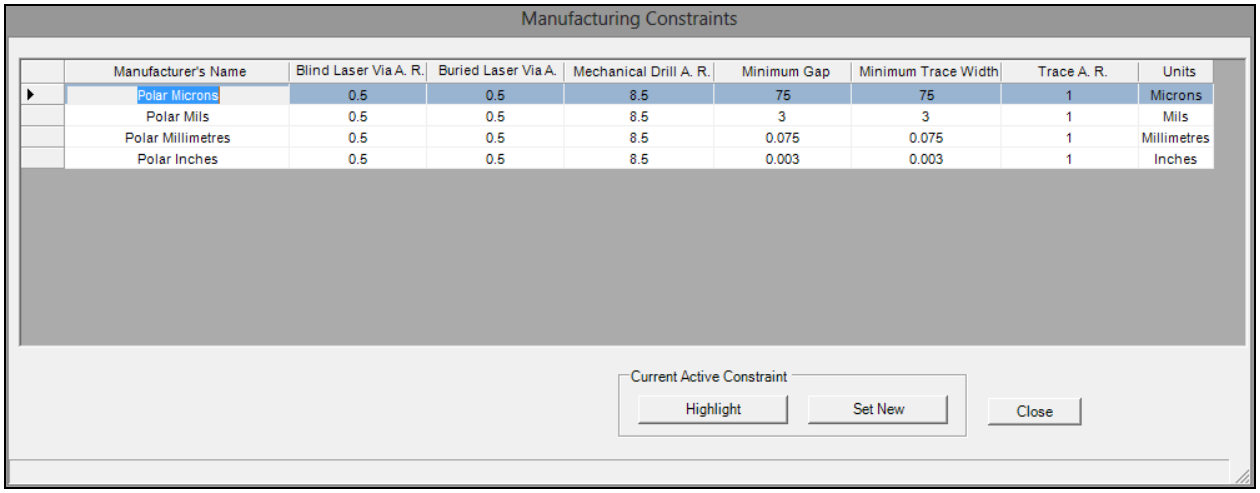
Users are strongly recommended to work through and correct errors in the order in which the errors are listed. Note that clearing each error may clear other errors in the process.

Manufacturing tests should be fixed before sending the PCB for manufacture. Hole sizes should be adjusted to comply. Failures with track and gap should be corrected, possibly by changing prepreg thickness and/or dielectric constants.

A collection of manufacturing constraints can be defined and the required one selected.

Creating and using manufacturing constraints

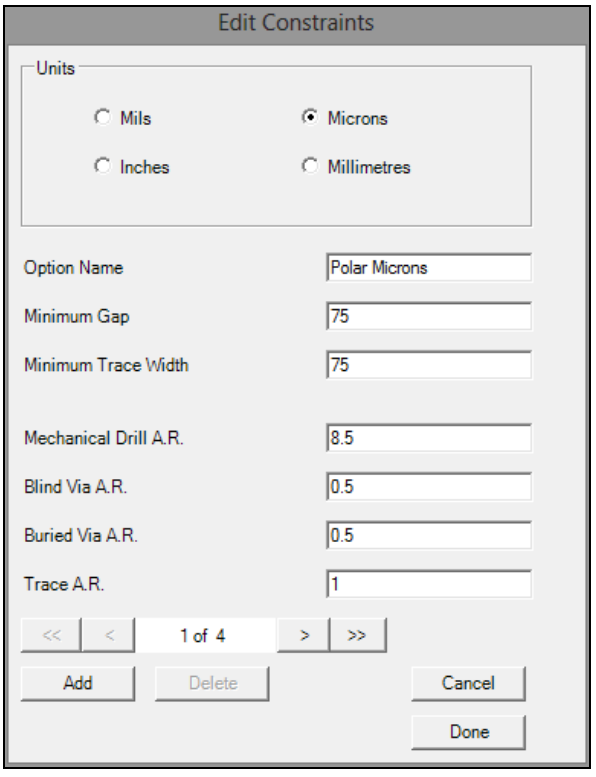
From the Tools menu, select Manufacturing Constraints: the Manufacturing Constraints window opens, displaying any manufacturing constraints added.



By default there will always be at least one. It is important to always have one constraint set active.

Editing constraints

Double-click on a constraint row will bring up the Edit Constraints dialog; use the dialog to add, delete or edit constraints (gaps, trace widths, aspect ratios, etc.)



To edit a constraint set, use the navigation buttons to select the set to be modified, change the values as required and then press Done.

To delete a constraint set, use the navigation buttons to select the set, then press Delete.

To add a new constraint set, press the Add button, this will add a new (empty) constraint row, enter the name and constraint values and press Done.

Adding controlled impedance structures

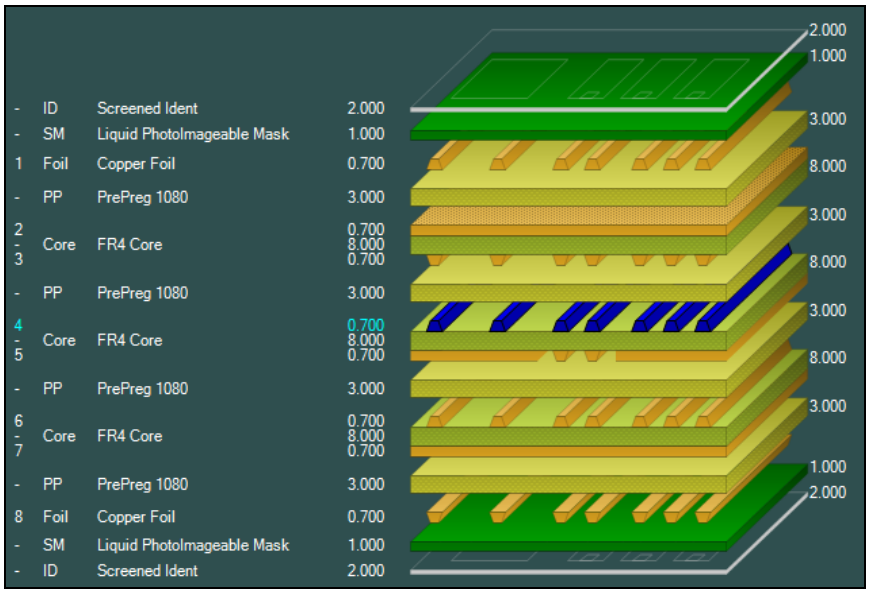
Note: before controlled impedance structures are added the stack must be fully defined (at least in terms of coppers). Attempting to add or delete coppers, or changing layer types will result in all controlled impedance structures being removed.

Speedstack incorporates the facility to add controlled impedance structures to a layer in the stackup. Speedstack is integrated with the Polar Instruments Si8000m/9000e controlled impedance field solvers so impedance values for a structure may be calculated at the click of a button.

Structure parameters may be copied to the field solver for processing (for example by the Si8000m/9000e Goal Seeking function) and calculated values pasted back into Speedstack for insertion into the stackup.

Adding a controlled impedance structure

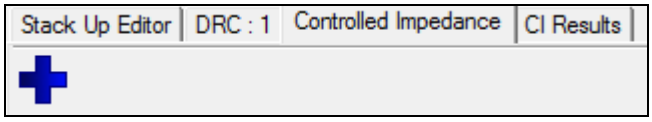
For the example stack below, add a controlled impedance structure to signal layer 4.



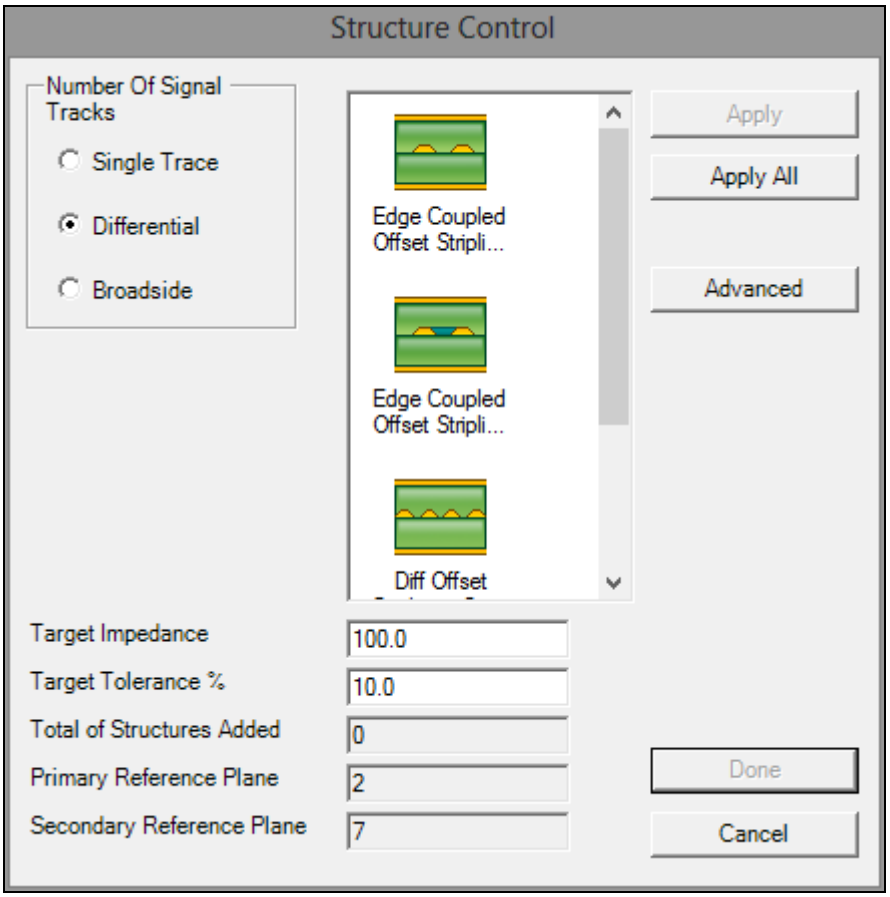
Sample stackup (showing signal layer 4 selected)

Note that in this example Layer 5 is a mixed signal/plane layer. Potential reference planes for Signal Layer 4 are therefore Plane Layer 2, mixed Signal/Plane Layer 5 and Plane Layer 7.

With Layer 4 selected, click the Controlled Impedance tab. The Add Structure button is displayed.



Click the Add Structure button; the Structure Control dialog is displayed containing the controlled impedance structures applicable to the selected layer in the stack. Choose values for the target impedance and tolerance. If necessary, resize the Structure Control dialog to view all structures.



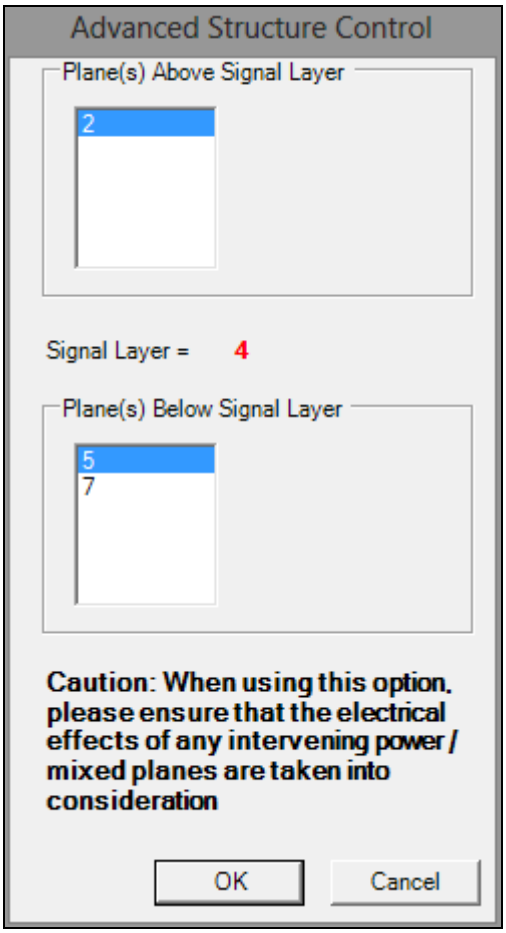
Click the Single Trace, Differential or Broadside option button as appropriate (in this case, choose Single Trace|Offset Stripline 1B1A with a 50 Ohm impedance.)

Note: Broadside only appears as an option where the signal trace is between two reference planes and Differential is selected.

Specify the values for Target Impedance and Tolerance.

Choosing reference planes

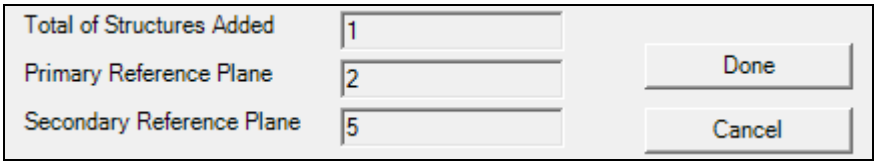
As there are multiple reference planes available (layers 2, 5 and 7, it will be necessary to specify which planes to use for this structure. Click Advanced.



Choose a reference plane from the list of available planes. In the example structure plane layer 2, mixed plane 5 and plane layer 7 are available for reference.

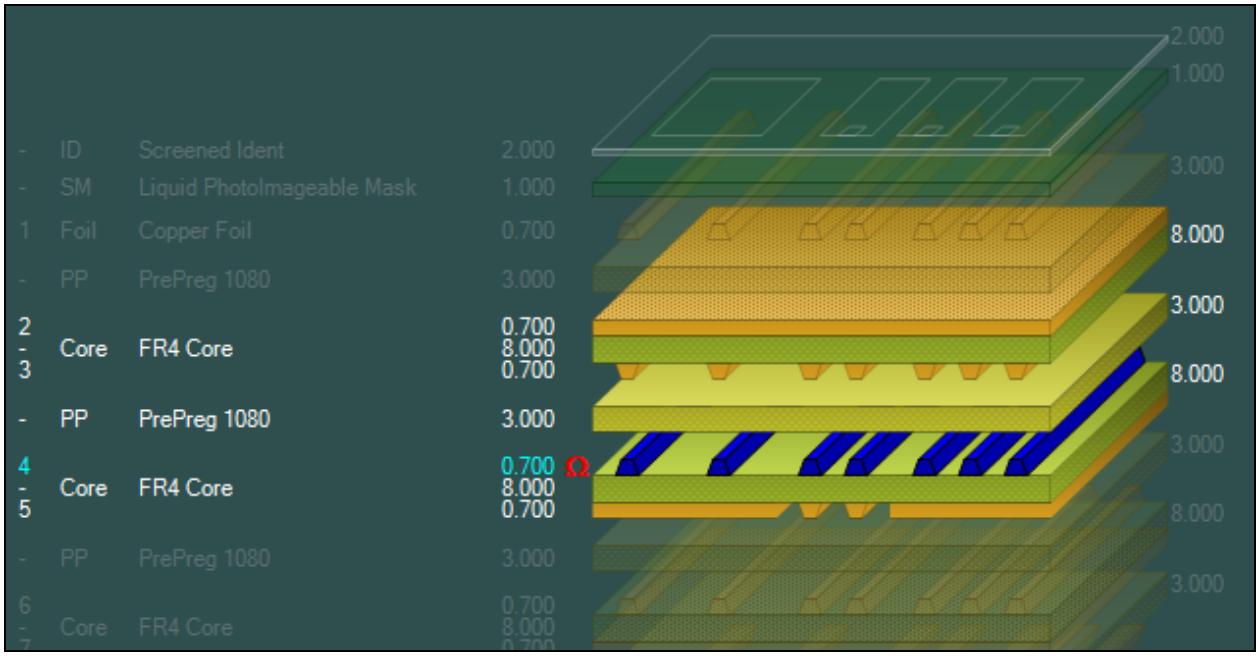
Note: if plane layer 7 is chosen as reference, it will be necessary to take into account the electrical effects of mixed signal/layer plane 5.

In this example choose mixed signal/plane layer 5. Press OK to confirm. The chosen reference planes are shown below.



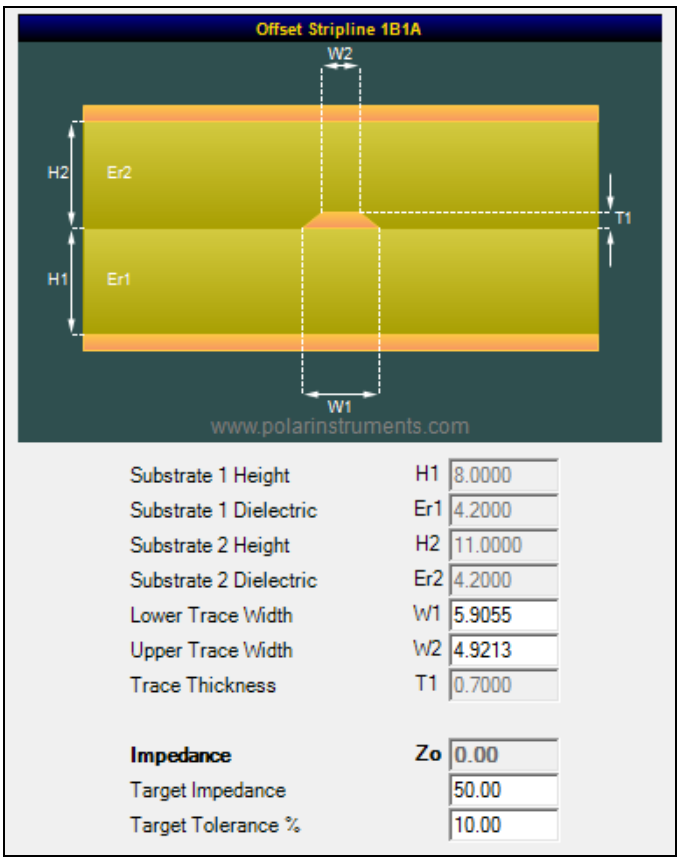
Repeat for all structures to be added. Click Apply for each structure then click Done to finish. In this example, choose a single structure.

Layers with controlled impedance structures are indicated by a red Ohms symbol.



The stackup window changes to reflect the selected signal layer and its associated reference planes.

The applied structure is displayed in the Controlled Impedance pane.



The window displays the parameters of the controlled impedance structure. Fields shown "greyed out" are values derived from the choice of materials in the stackup.

For this structure, enter appropriate values for lower and upper trace widths.

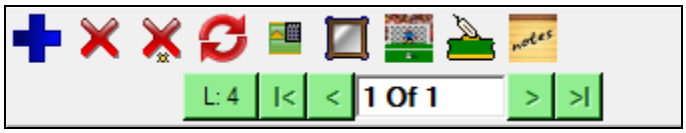
Calculate Displayed Structure

Click the Calculate Displayed Structure button to display the impedance value of the structure with the current parameters. The parameters may then be varied to alter the value of the final impedance. In the example above the user can vary the trace width in order to approach the value of the target impedance; other parameters are changed by modifying the stackup dimensions (for example, core thickness H1.)

Hint: clicking Apply All in the Structure Control dialog adds a single instance of all structures matching the stackup layer and the chosen criteria; the user can then choose the structure producing the value nearest the target impedance and delete the structures that are not needed.

Controlled impedance toolbar

Controlled impedance operations are performed via the Controlled Impedance toolbar.



 Add controlled impedance structure to current layer

 Delete structure from current layer

 Clear all structures from current layer

 Refresh and calculate impedance

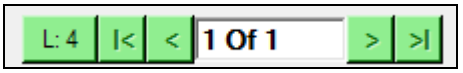
 Calculate structure

 Mirror structures

 Goal seek

 Set CITS test

 Free hand notes



Display layer and navigate through structures

Changing parameter values

Clicking the Calculate function yields a value for impedance. The user can now vary parameters (for example, the dielectric height) to yield a value for impedance closer to the target impedance.

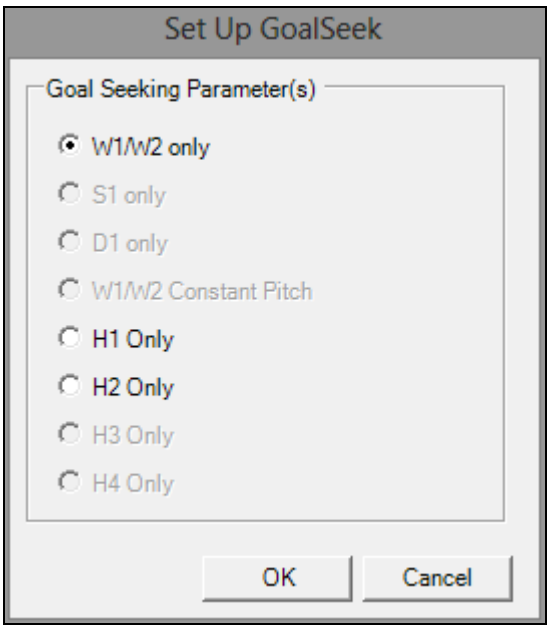
For this example, select the core layers; click the Swap Selected Material button and choose a different core (ensure the same dimensional units are used throughout the structure) and click the Refresh and Calculate Impedance button. The impedance is recalculated to its new value.

To achieve an impedance acceptably close to the target impedance, use the goal seeking function of the Si8000m to alter other parameters (in this case, change the upper and lower trace widths).

Goal seeking with Speedstack

Speedstack provides the facility to solve for horizontal parameters (e.g. trace width and separation, ground strip separation, etc.) to produce the target impedance (or calculate that the target impedance is unachievable with the current values).

Click the Goal Seek button to display the Set Up GoalSeek dialog; the options available will depend on the controlled impedance structure.



Click OK; the Speedstack attempts to arrive at the target impedance by iteratively modifying the specified parameters. It may be necessary to add or delete prepregs to achieve the target impedance.

Goal seeking with the Si8000m/9000e

Speedstack Stackup Builder is fully integrated with the Si8000m/Si9000e Controlled Impedance Field Solvers. Users can transfer Stackup layer dimensions to the Field Solver, solve for stackup parameters to produce the target impedance (or calculate that the target impedance is unachievable with the current values) then transfer the solved dimensions back to Speedstack.

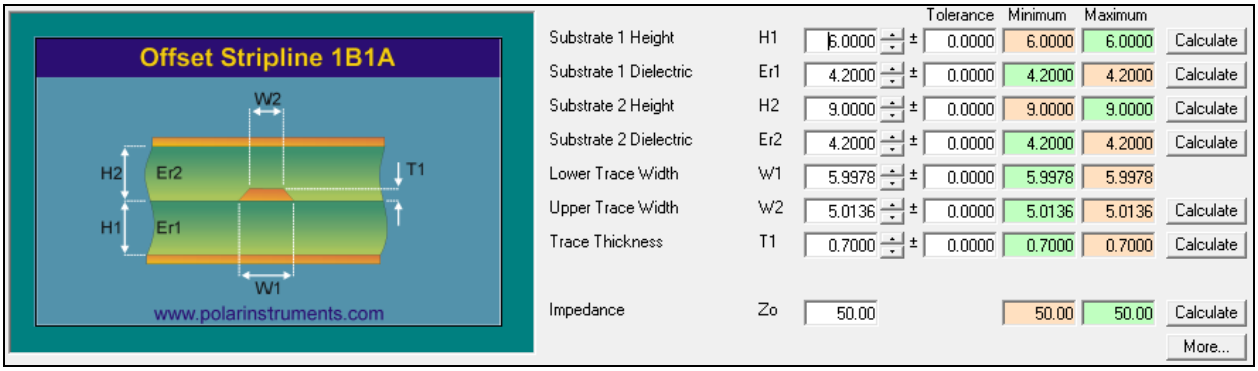
Ensure the Field Solver is running and that its units match the Speedstack units.

To Field Solver

With the stackup parameters displayed in the Controlled Impedance window, click To Field Solver to transfer the current Speedstack parameters to the Si8000m/Si9000e.

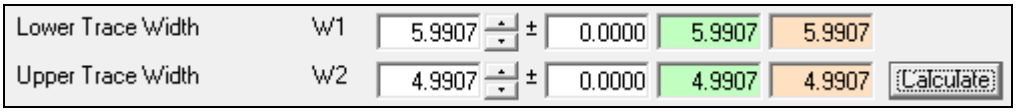
Paste from Speedstack

Switch to the field solver and click the Paste from Speedstack button to load the parameters into the associated field solver fields. The field solver reflects the structure and parameters of that selected in Speedstack.



For the data shown above seek a final value for impedance of 50 Ohms; H1, Er1 and T1 are fixed, so goal seek on W1,W2.

Click the Upper Trace Width (W2) Calculate button to goal seek on trace width. The field solver returns new values for trace width to produce 50 Ohms final impedance.



Click the Copy to Speedstack button, switch to Speedstack and click the From Field Solver button to display the solved parameters for the target impedance.

Copy to Speedstack

From Field Solver

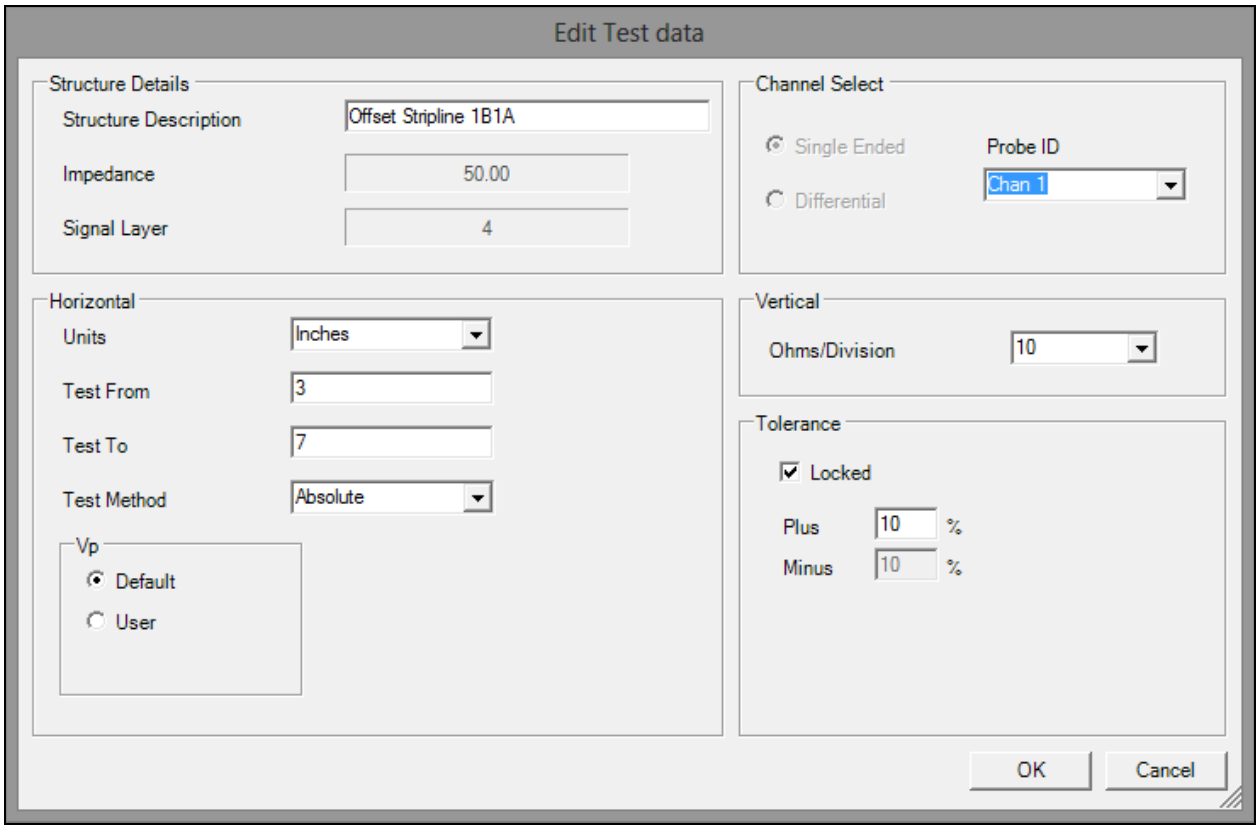
Note: it may be necessary to round some dimensions (for example, the dielectric heights) to the nearest practical values and recalculate the impedance.

CITS test files

Speedstack can create CITS test file data for each controlled impedance structure in the stack.

Set CITS Test

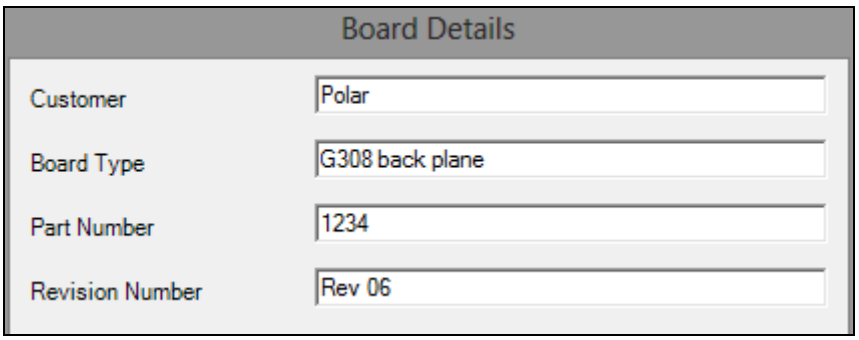
Select each structure and click Set CITS Test to display the Edit Test data dialog; specify the CITS test parameters for each structure to be tested and click OK.



For details on editing and choosing parameters for CITS test files consult the associated CITS User Guide.

Exporting the CITS test file

With the test data specified for each structure, from the File menu choose Export To|Export CITS File. Add descriptive Board Details and notes as required.



Click Make File and navigate to a suitable folder and save the CITS (.cif) test file.

Working with flex-rigid stackups

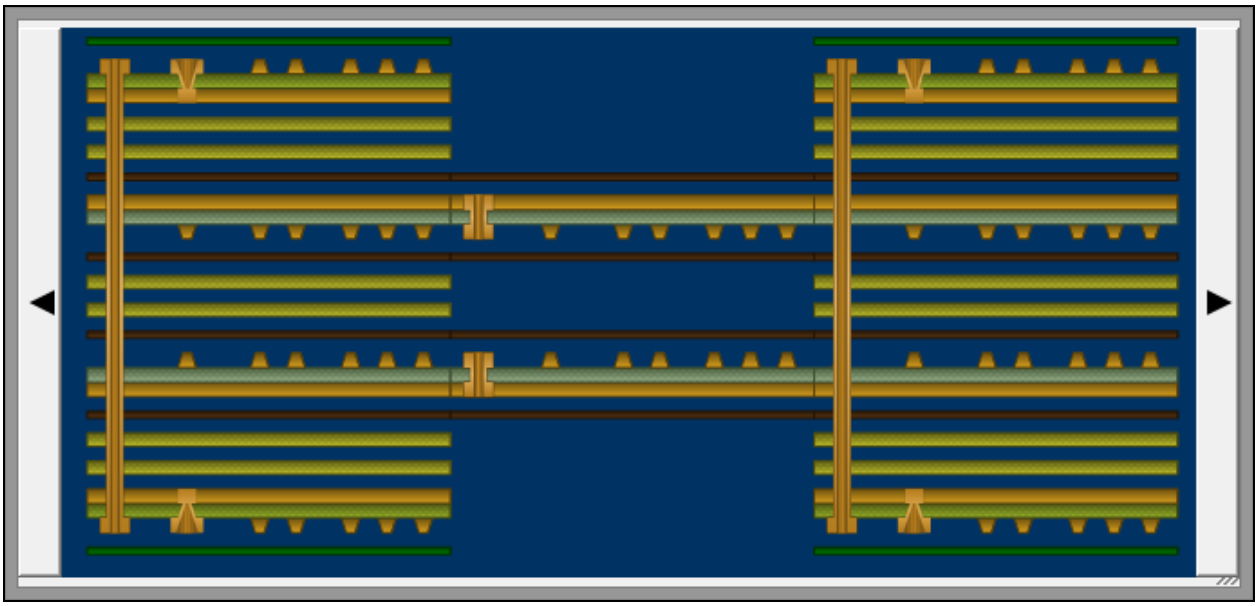
Speedstack Flex

Speedstack Flex allows PCB fabricators and OEM engineers quickly to create and document accurate and efficient flex-rigid PCB layer stackups.

Easy graphical stackup display

The Speedstack Flex Navigator enables the board designer to link and document as many cross sections as necessary in order to fully document a flex-rigid build up.

Speedstack Flex supports documentation of common flex-rigid constructions, including *doublets* where stacked pairs of flex link two rigid sections of the flex-rigid construction together (see graphic below.)



Speedstack's Navigator works from a master stack comprising the full set of materials used in the final stackup and documents each rigid and flex-rigid section with as many "sub-stacks" as needed for the design. There are no limits to the number of sub-stacks or layer count of the total build.

A range of materials including flexible adhesives, bondply and FlexiCore can be enabled or disabled for each layer, and impedance structures can be added to each sub-stack.

Mesh / Crosshatch ground planes

When used with Polar's Si8000m and Si9000e field solvers, Speedstack Flex permits modelling and documenting

mesh/crosshatch ground planes from within the Speedstack Flex environment. Mesh geometry and structure data can be easily shared between Si8000m and Si9000e.

Internal Coverlays
Advanced rules allow impedance structures to be added when coverlays exist internally within a stack. When a coverlay is beyond the outer copper it will behave like a coating, when internal it will behave like a bondply or prepreg.

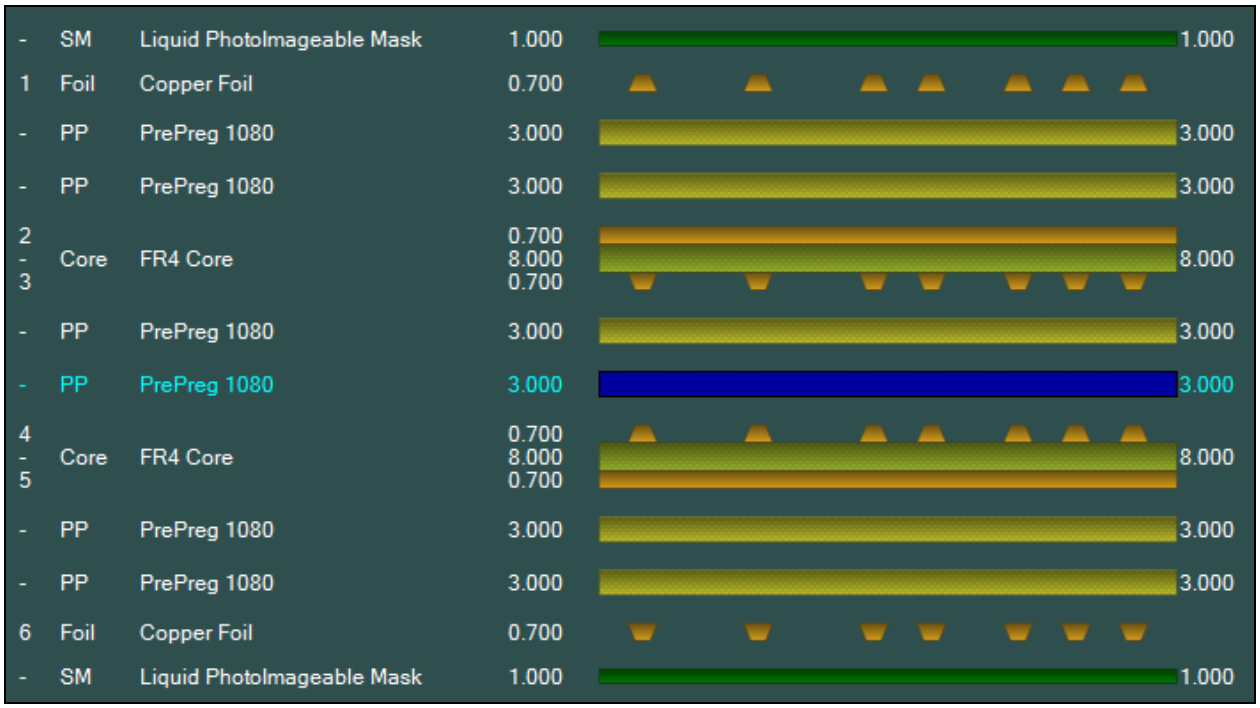
Definable colours per material
Speedstack Flex can set and store individual material colours via the material Properties dialog. This will help ensure that special build requirements are obvious during fabrication. This will be found useful for documenting plated layers or highlighting specific material usage such as no-flow prepregs and flexible cores.

Enabling Speedstack Flex/HDI

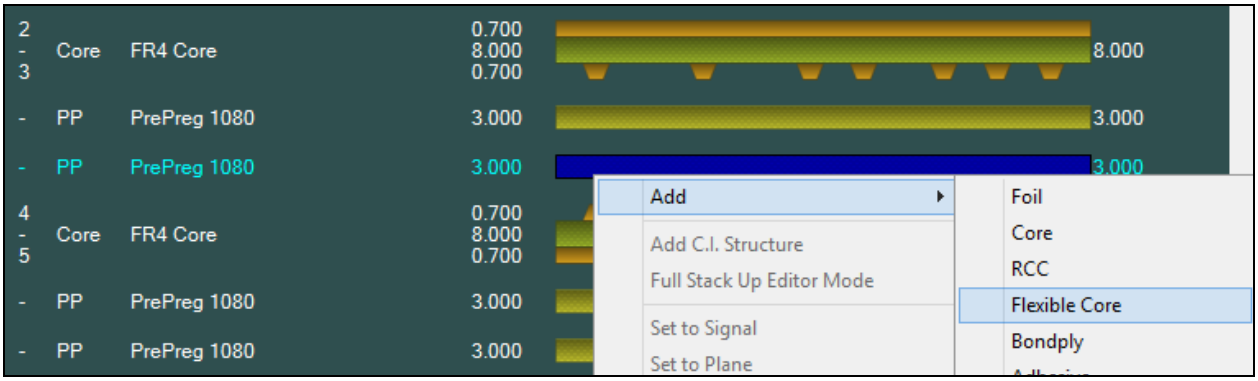
To enable Speedstack Flex/HDI select Tools|Options and ensure the Licensing pane purchasable option Speedstack Flex/HDI License check box is ticked.

Adding a flexible core

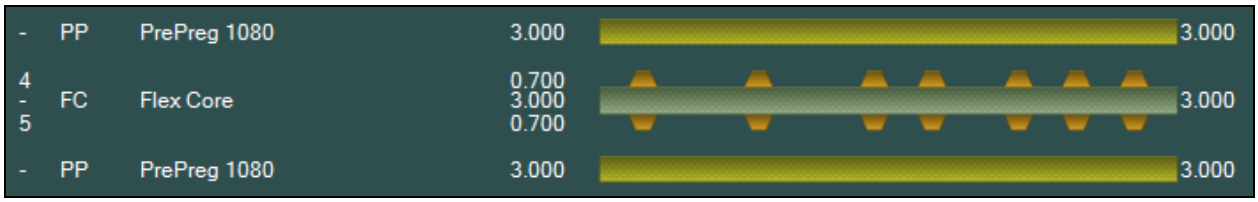
Create and save a symmetrical 6-layer stackup as shown in the sample stack below



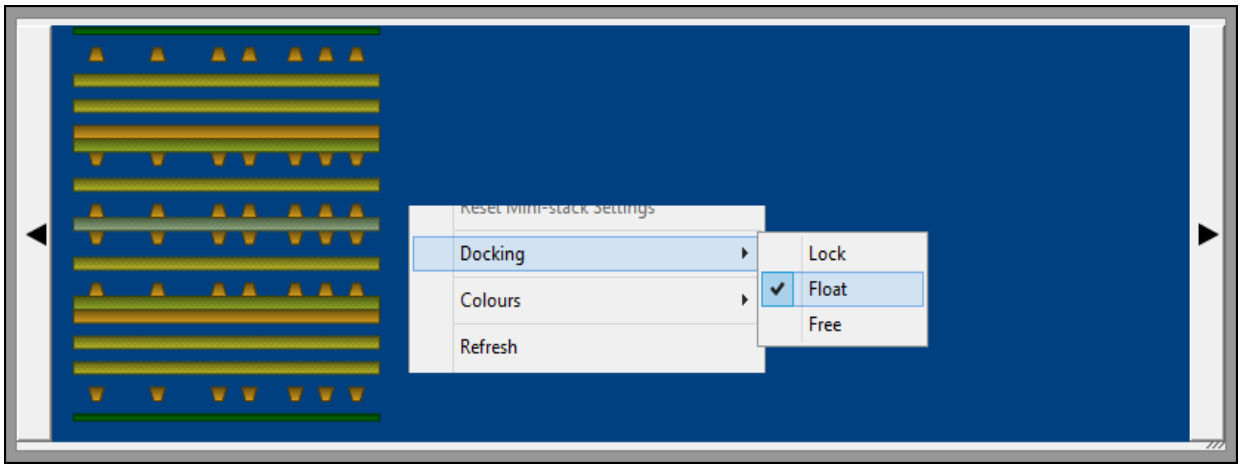
Ensure Symmetrical mode is off, right click the prepreg above Layer 4 copper and add a flexible core:



The flexible core is added as the new layers 4 and 5.

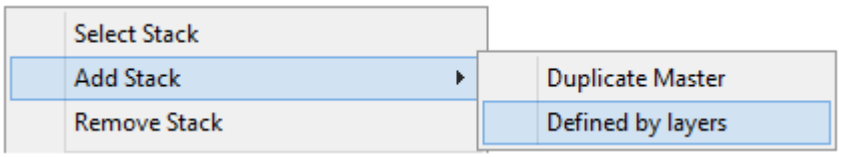


Using the Navigator
Press F4 to display the Navigator

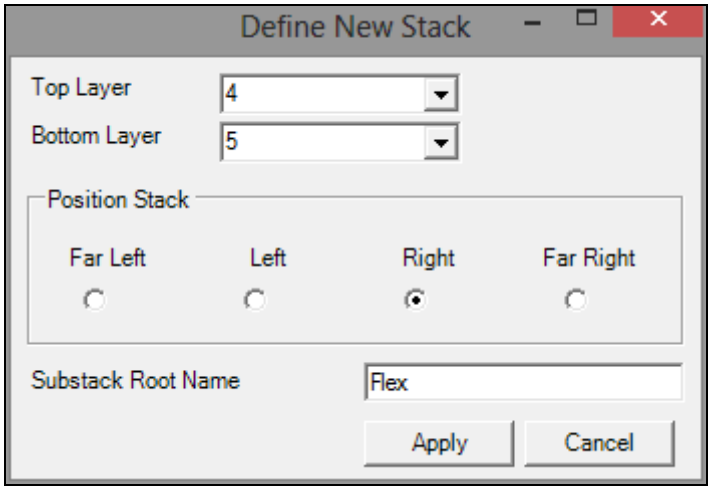


Right click the Navigator and choose Docking|Float to allow the Navigator window to be resized. The Navigator will move with Speedstack's Stack Editor. Choose Free to allow the Navigator to move independently of the Stack Editor.

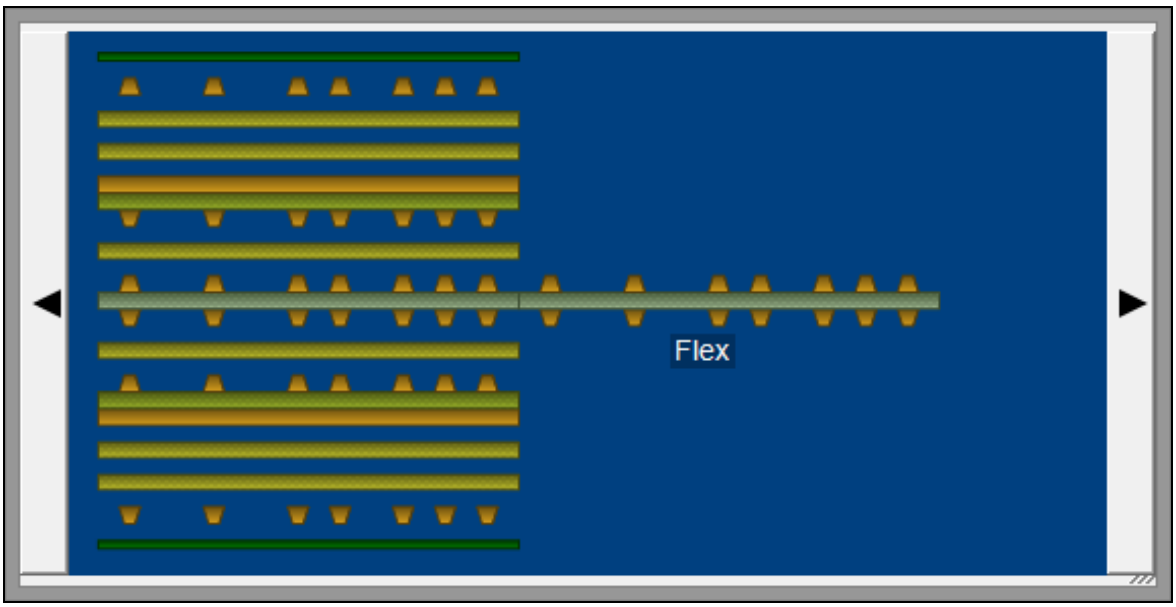
Adding stacks
Select the stack in the Navigator window and click Add Stack and choose Defined by Layers



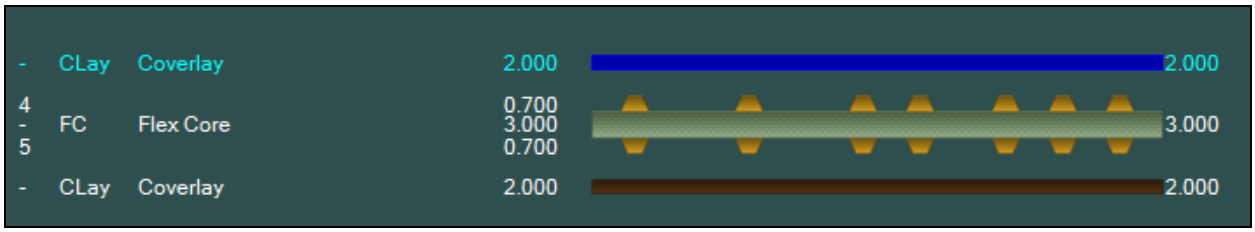
From the drop-down list choose Layer 4 as the Top Layer and Layer 5 as the Bottom Layer as shown below and enter Flex as the Substack Root Name.



The new stack is added to the Navigator. Each sub-stack can be renamed individually as required.

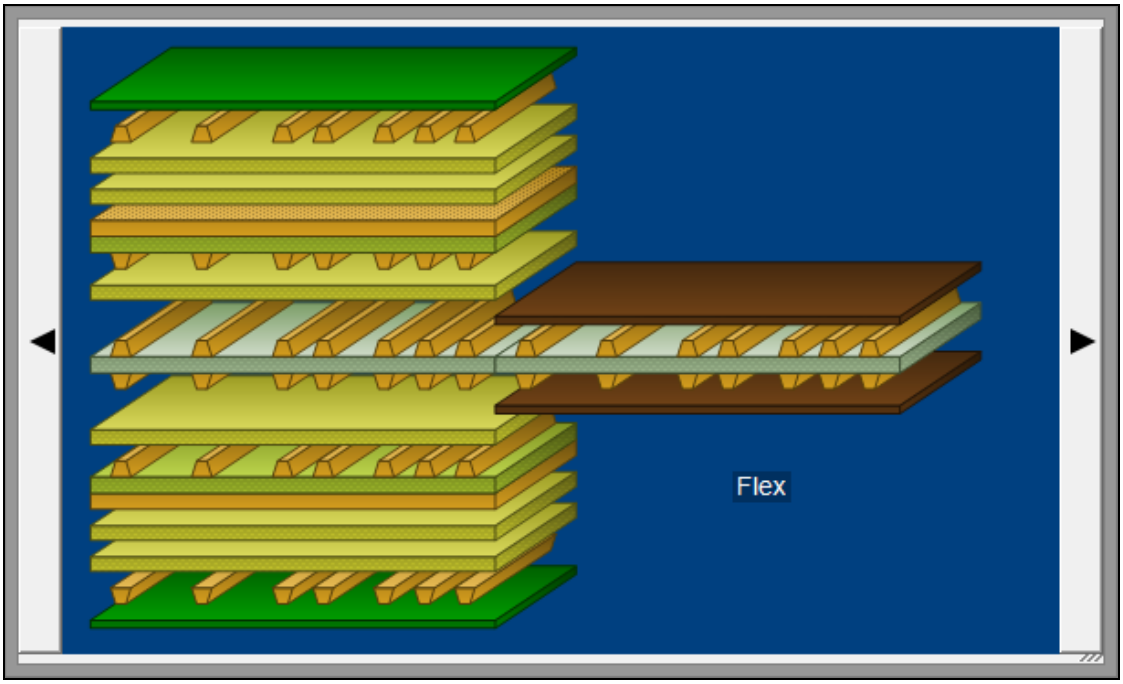


Click the new stack – the selected stack is reflected in the Stack Editor and listed in the status bar. Select Symmetrical mode, in the Stack Editor click the new core and add a coverlay above.



The coverlays are added symmetrically about the core. Changes made in the Stack Editor are reflected in the

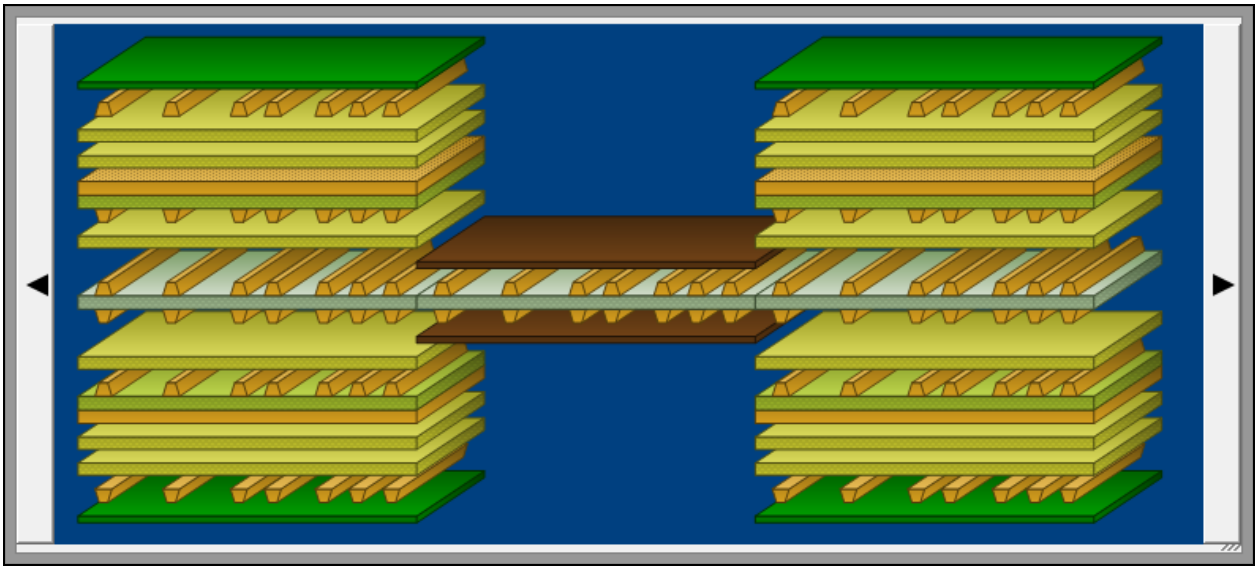
Navigator. Click into the Navigator – use the mouse wheel to resize. The Navigator can display in 2D or 3D views.



The new stack with its added materials appears in the Navigator; clicking each stack in the Navigator displays it in the Stack Editor and allows editing as described earlier to add controlled impedance structures, change layer types, add non-copper layers, etc.

Adding a new stack

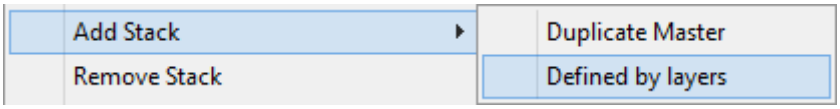
Right click the Navigator and choose Add Stack|Duplicate Master, rename the new stack and click OK.

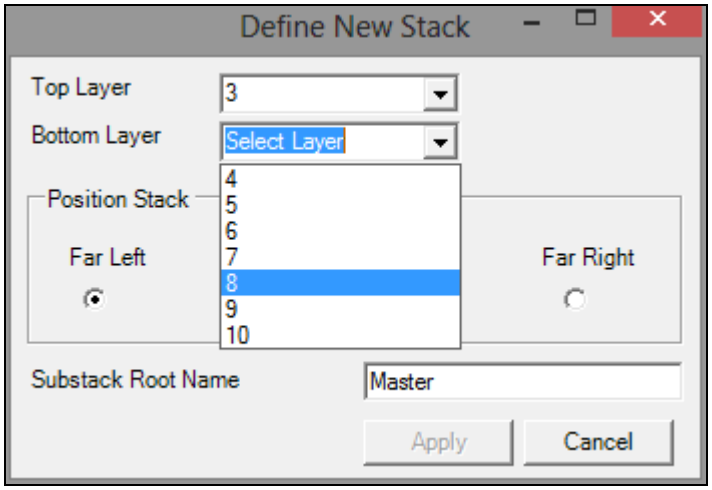


The new stack is added to the Navigator. Click on each stack to display it in the Stack Editor and then edit as required.

Defining new stacks

New stacks may be added defined by layers of the master stack. Choose Add Stack|Defined by Layers:

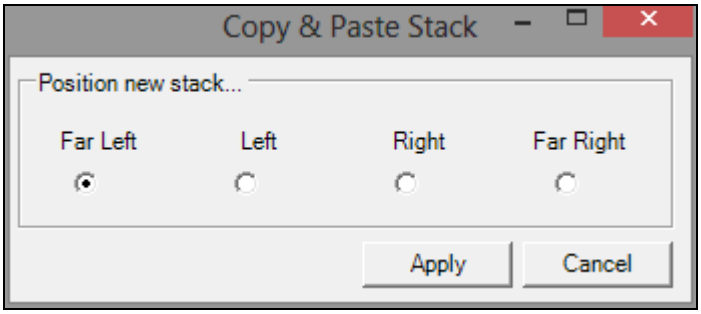




Choose the starting and finishing layers and specify a position for the new stack, choose a descriptive sub-stack root name and click Apply.

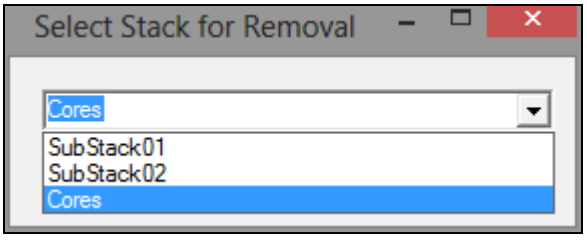
Copying and pasting stacks

To copy a stack in the Navigator select the stack, choose Copy and Paste Stack, then from the dialog below choose the position of the new stack



Removing stacks

To remove a stack right click the Navigator, choose Remove Stack and select the stack to be removed.



Working with HDI builds

Speedstack HDI

For HDI PCB fabricators, Speedstack HDI provides the flexibility to quickly calculate the possible impact of substituting alternative materials to improve manufacturability and reduce cost while maintaining the specified parameters and performance of the board.

Easy graphical stackup display
The HDI navigator provides a rapid guide through the sequential sub-stack lamination sequence and presents the complete assembly in a parsed graphical display that shows each phase of the multi-step lamination sequence of an HDI PCB. User-definable settings within the navigator allow engineers to display layers in transparent, invisible or 3D mode.

Sub-stack reordering
Speedstack HDI makes re-ordering and renaming sub-stacks quick and easy with the Speedflex Navigator; sub-stacks can be simply moved left or right within the Navigator window.

HDI builds

Use the Speedstack Navigator to document HDI press/drill cycles. Speedstack can document press cycles based on foil locations or drill start and end layers.

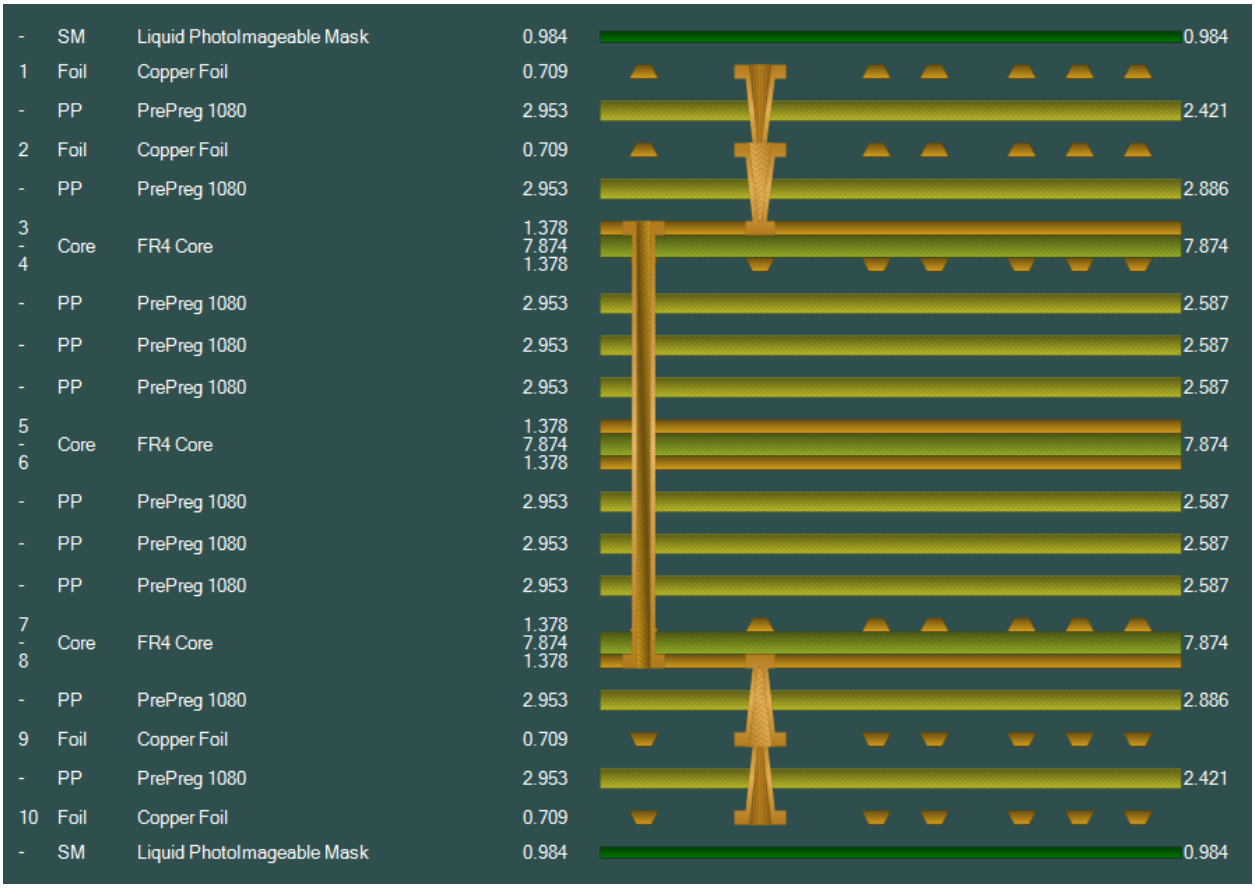
Sequential plan
The Sequential plan command creates sub-stacks that represent each press cycle in a sequential lamination from the Master stack based on foil locations.

Drill plan
Using Drill Plan, Speedstack determines the sub-stacks by the start / end layers of the drills.

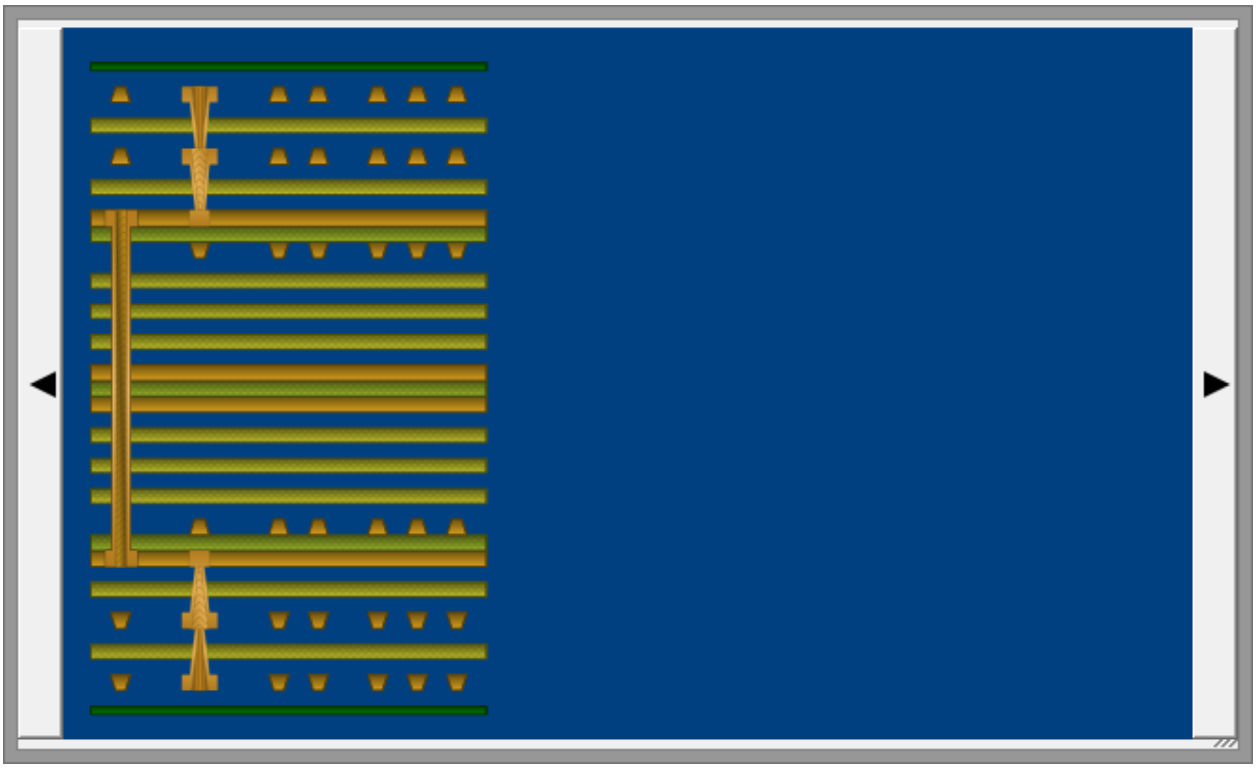
Creating the target stack with the Stack Editor

Consider the target stack below – it will require three press cycles. Build and document the stack in the Stack Editor.

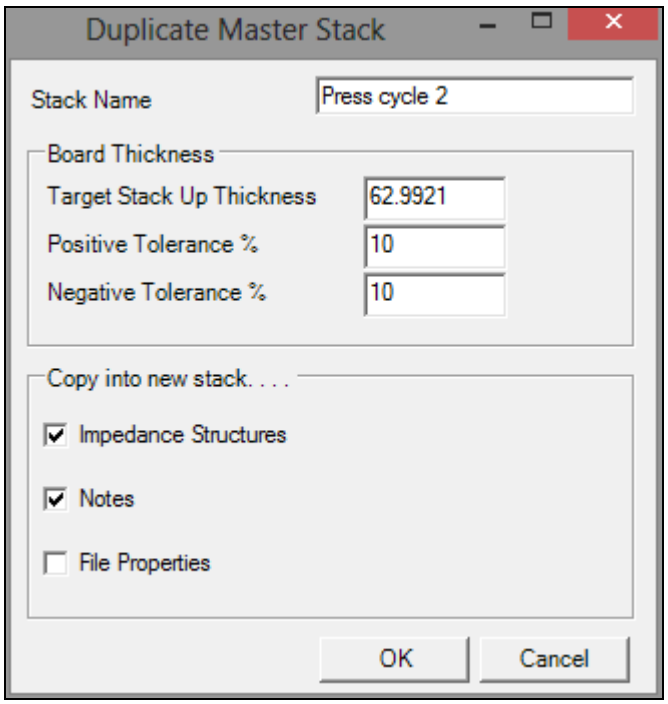
Switch to 2D View.

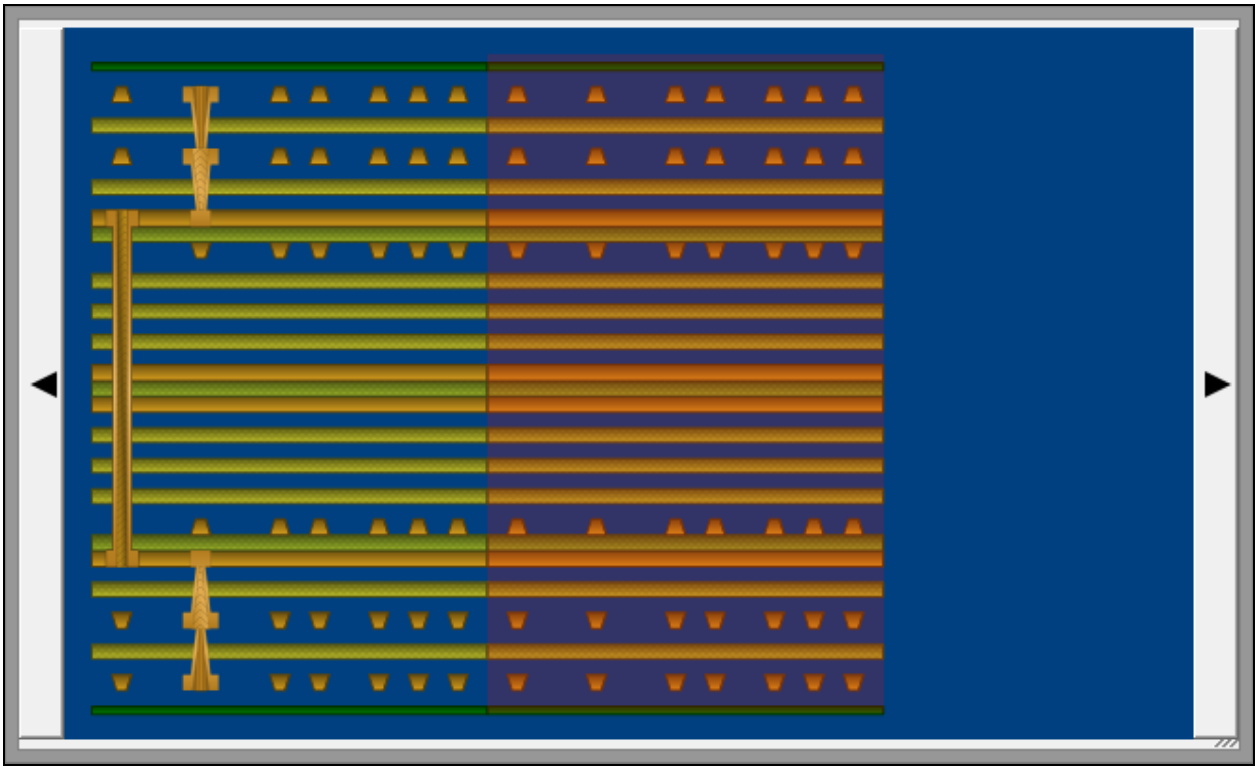


With the target stack completed use the Navigator's Add Stack to document each press cycle, building up the stack in the Navigator. Press F4 to start the Navigator and display the master stack.



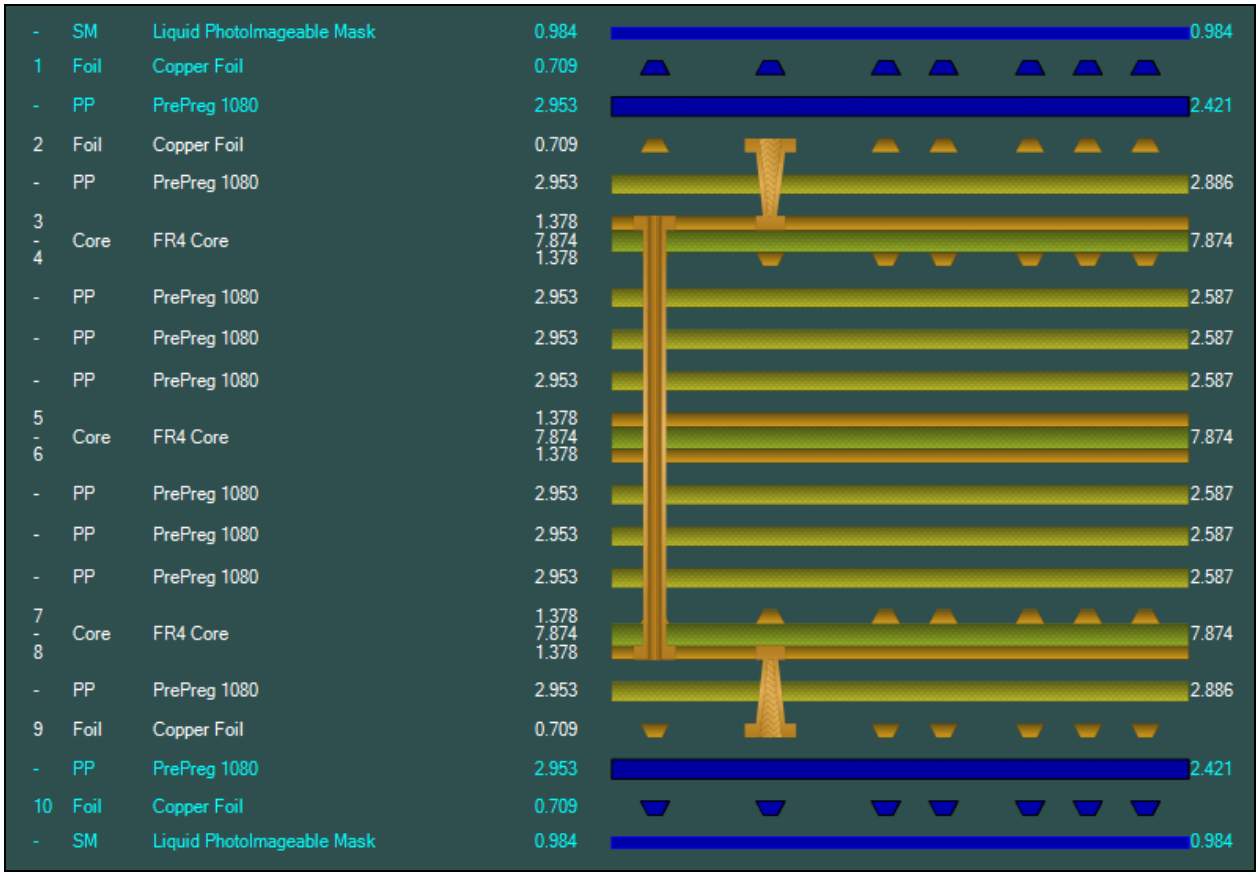
Click Add Stack to copy the stack and name the new sub-stack Press cycle 2.



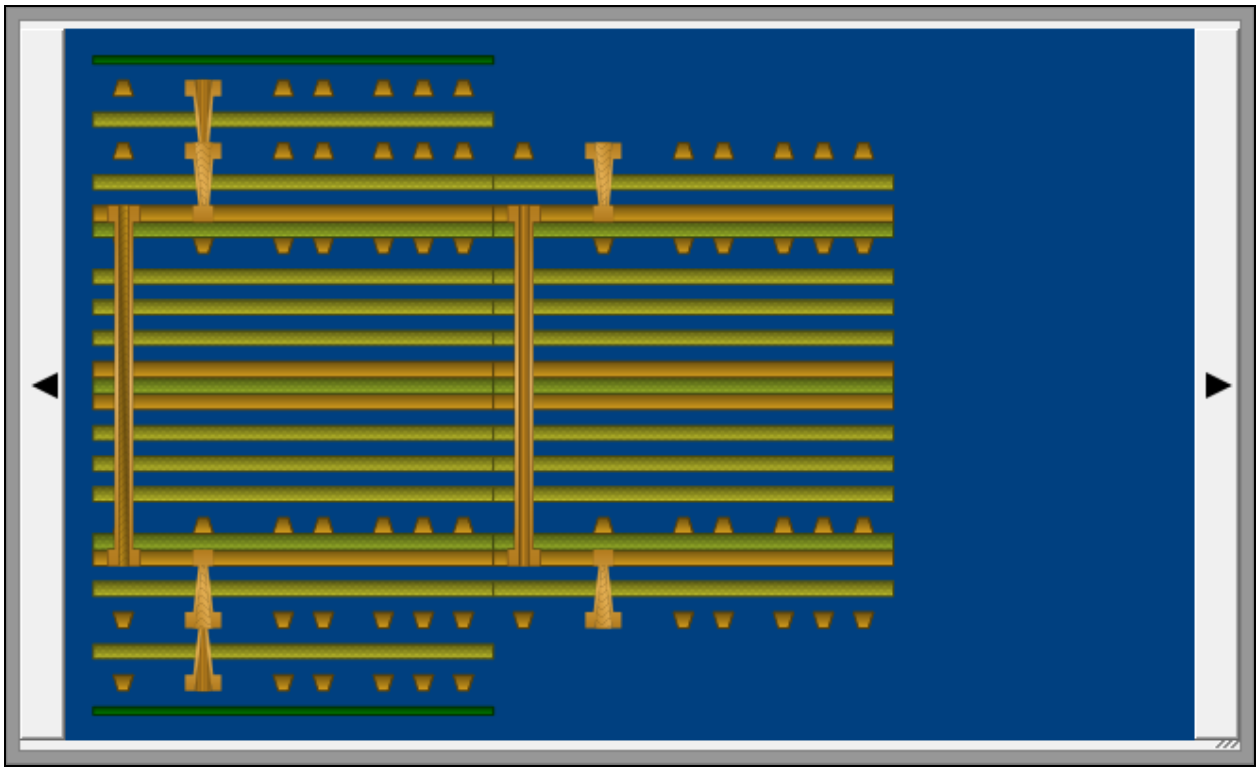


The new sub-stack is copied into the navigator window

Click the sub-stack to display it in the Stack Editor. In the Stack Editor add the drills and disable the materials that are added in the final press cycle.

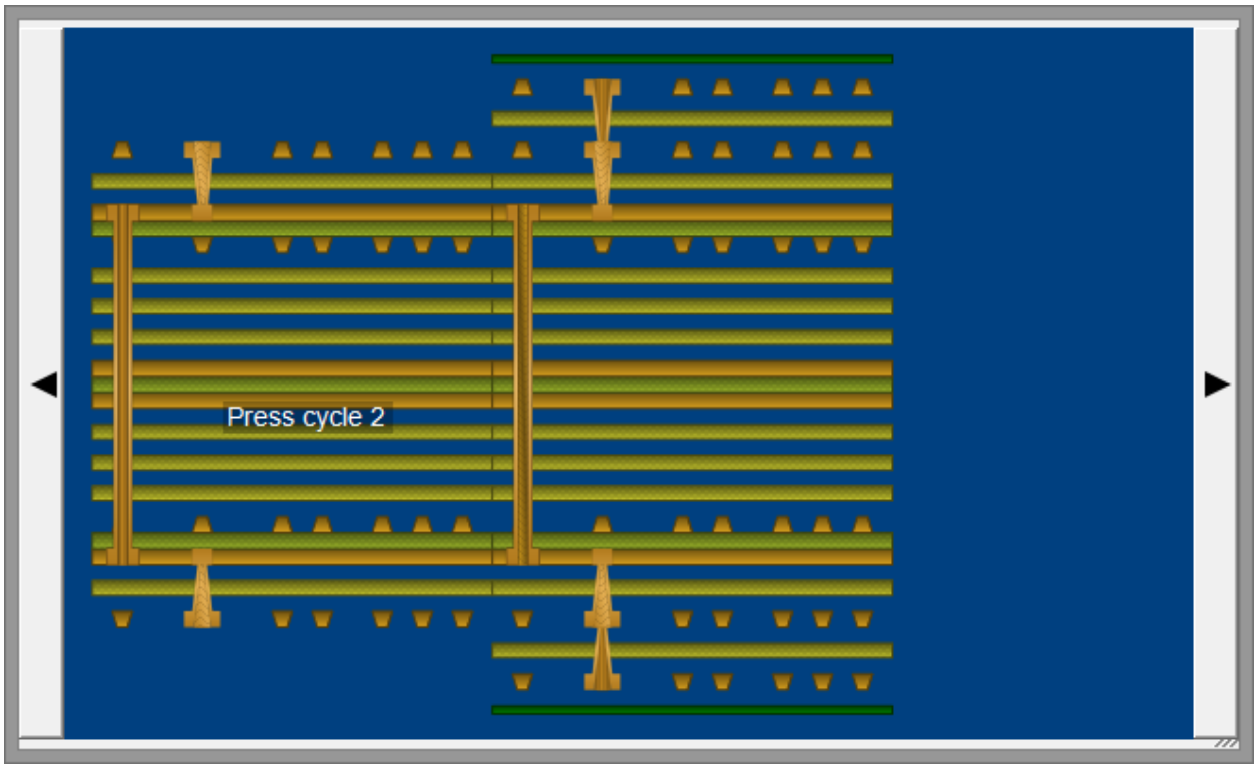


The Navigator displays the second press cycle alongside the master stack.

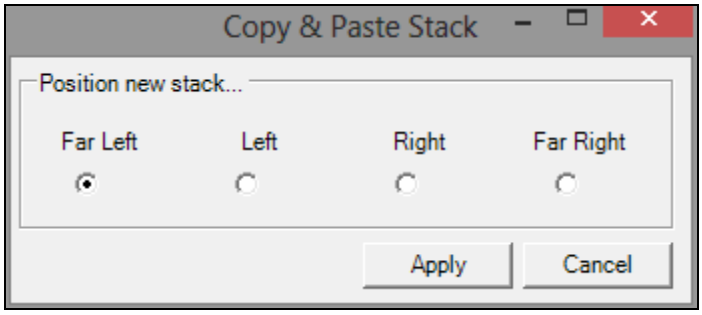


The sub-stack can be displayed either to the right or left of the master stack. Right click the sub-stack and from the context menu choose Move Left.

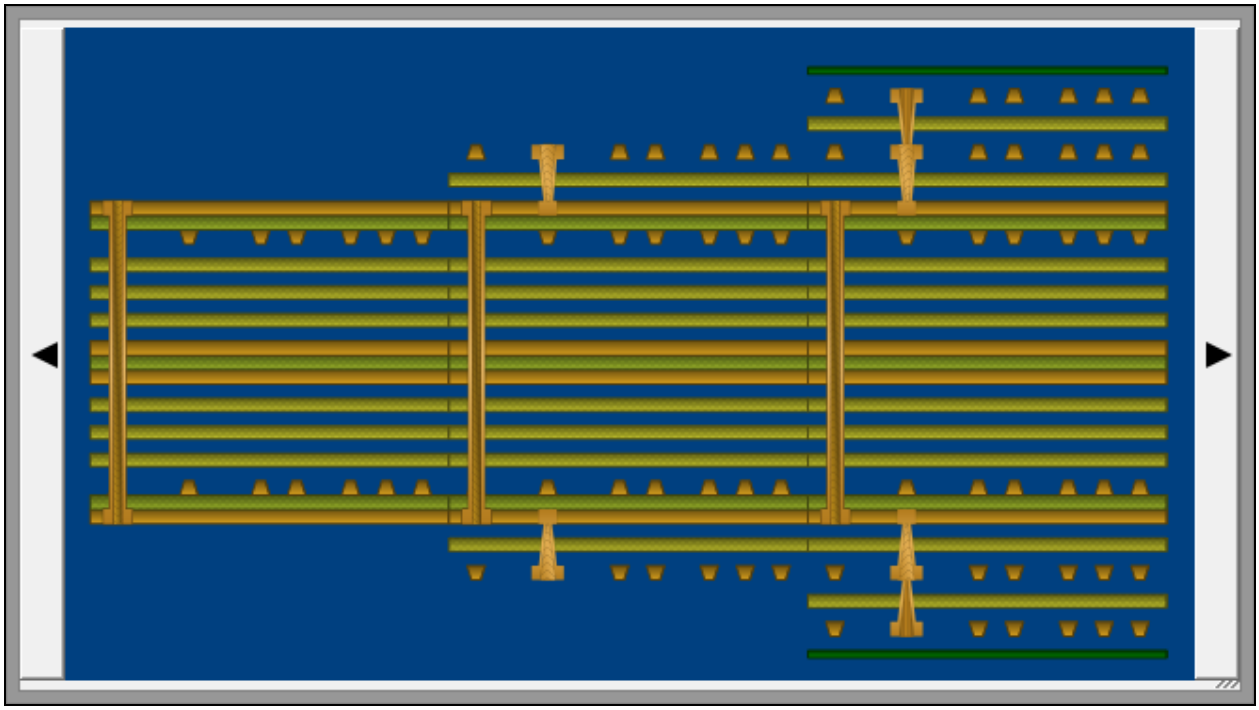
Sub-stack Press cycle 2 is shown to the left of the master.



To add the first press cycle right click the sub-stack and choose Copy and Paste Stack and position the new sub-stack to the far left.



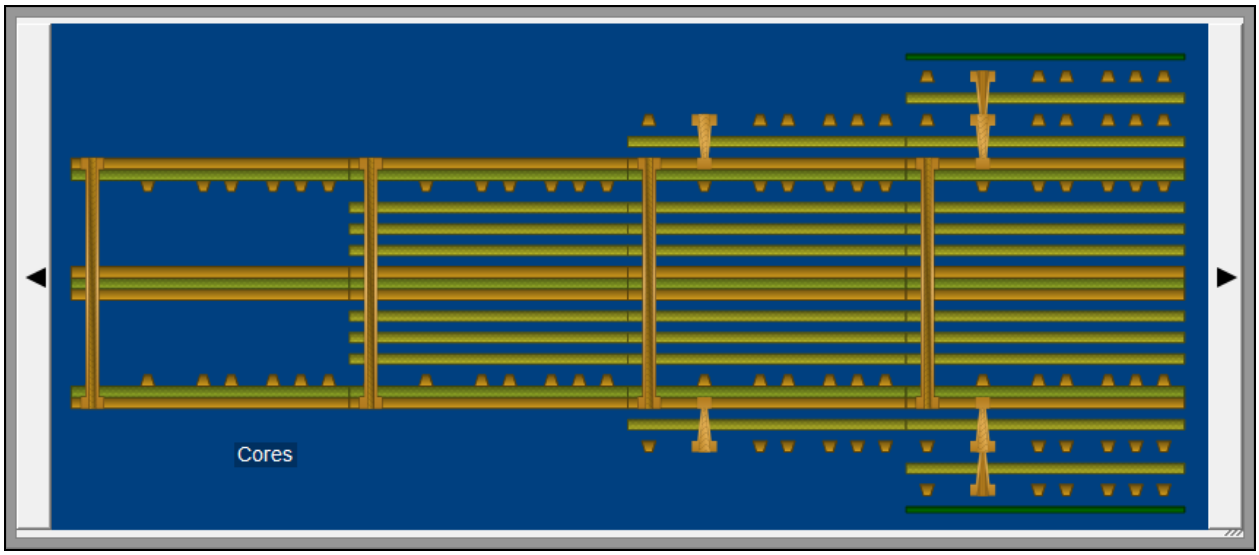
Modify the new sub-stack in the Stack Editor as previously described and display the completed stack in the Navigator.



Each press cycle appears as a separate stack in the Navigator.

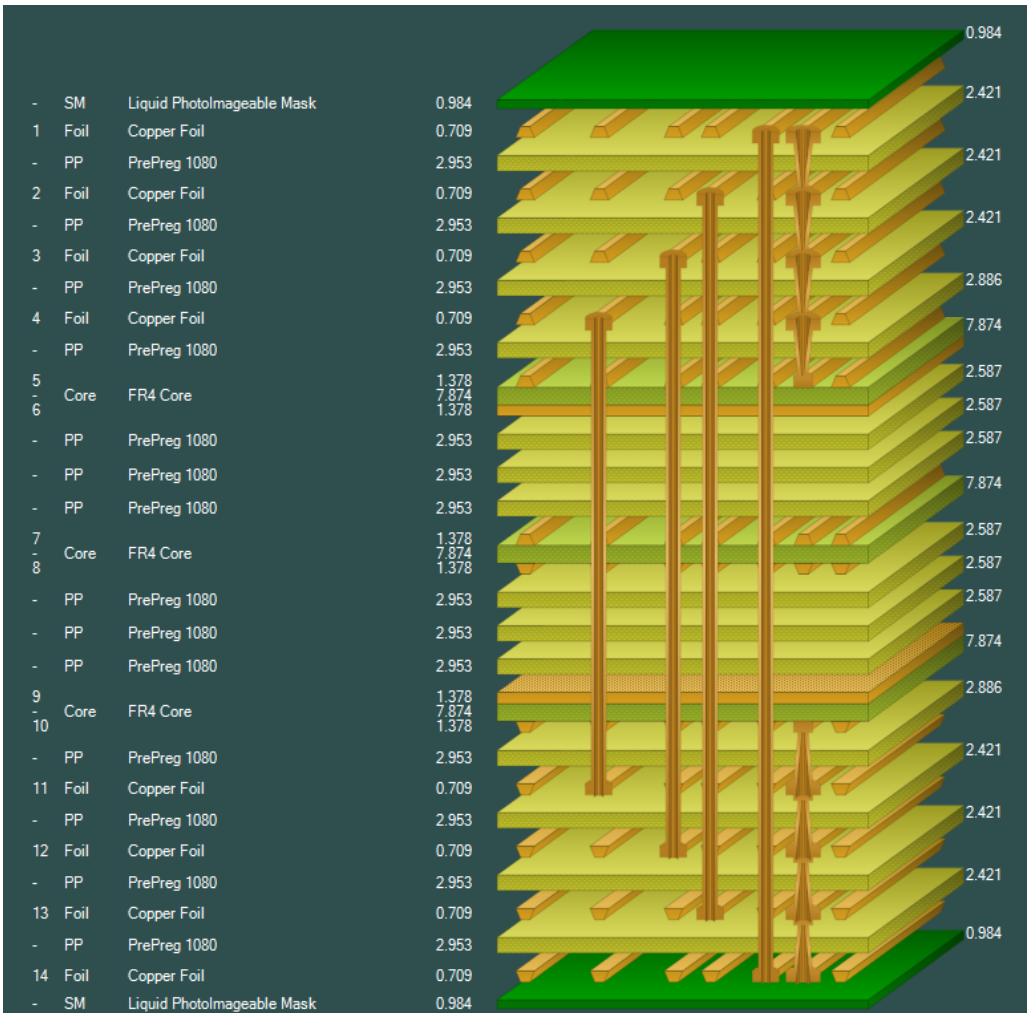
In the fabrication process the manufacturer will process all the core materials first, prior to bonding where each core is interleaved with prepreg materials. It is sometimes useful, therefore, to see all the core materials on a single sub-stack.

Right click the Navigator window and choose HDI Build|Expose Cores to display the core layers.



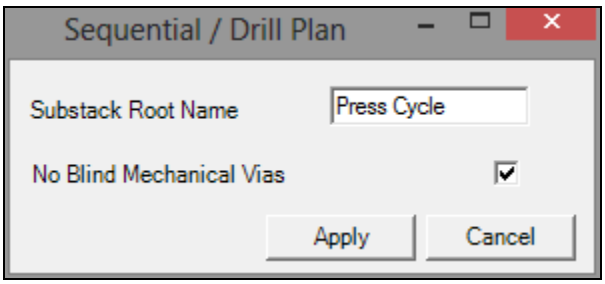
Using the Sequential Plan

Sequential Plan creates sub-stacks that represents each press cycle in a sequential lamination from Master stack based on foil locations. Consider the 14-layer stack below – this stack will need several press cycles to manufacture.

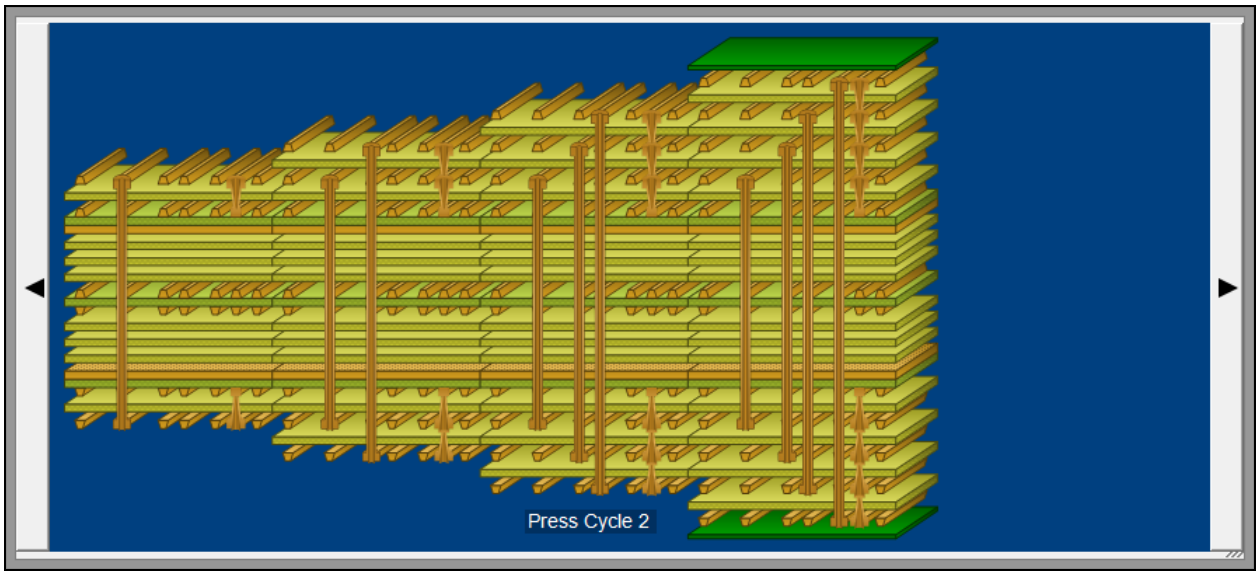


Opening the Navigator will display the completed master stack (shown below) in the Navigator window.

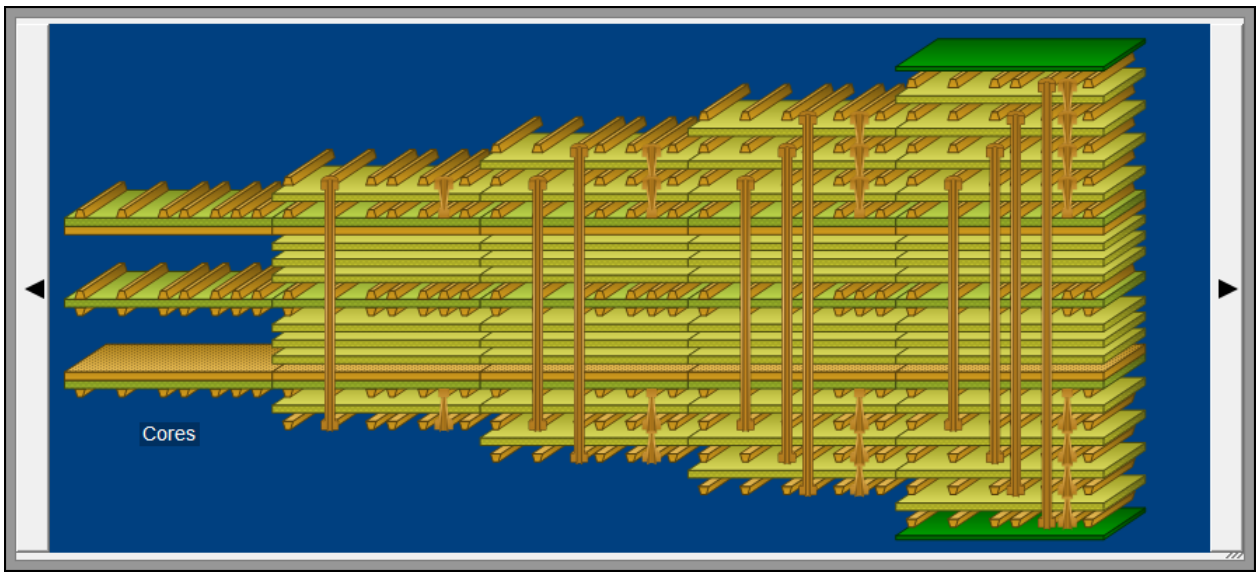
Right click the Navigator window and choose HDI Build |Sequential Plan and name the sub-stacks:



Click Apply – the Navigator displays the 4 press cycles

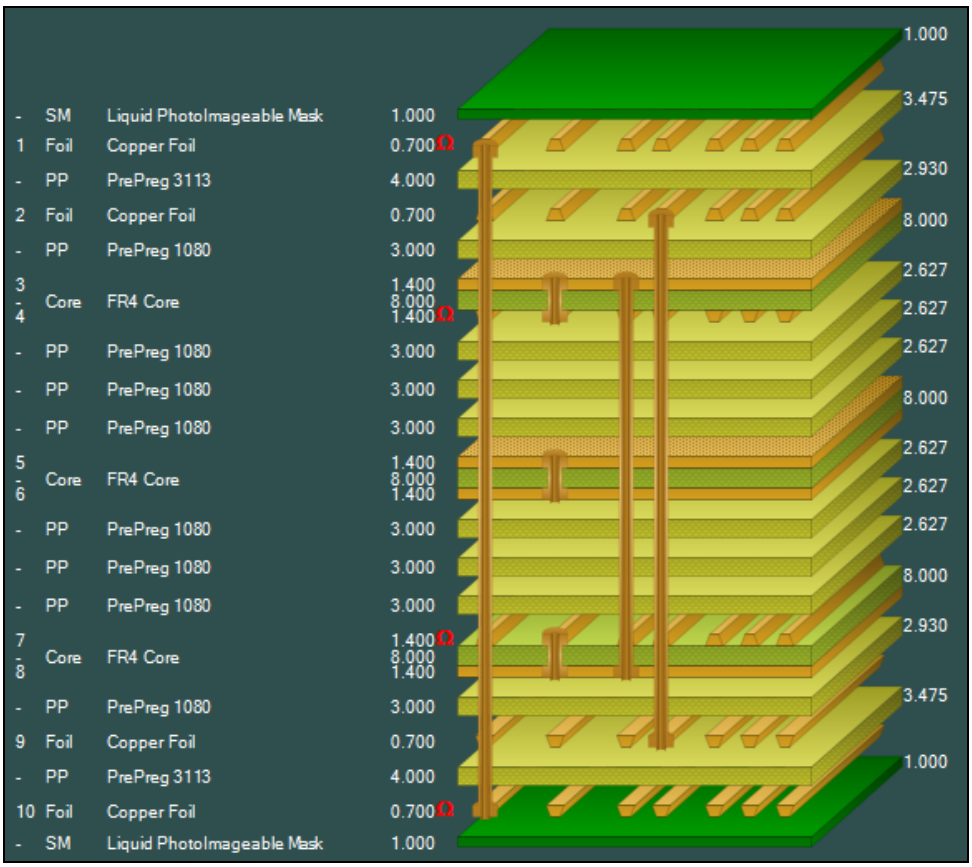


Choose HDI Build|Expose Cores – the cores are displayed in the Navigator window alongside the press cycles.

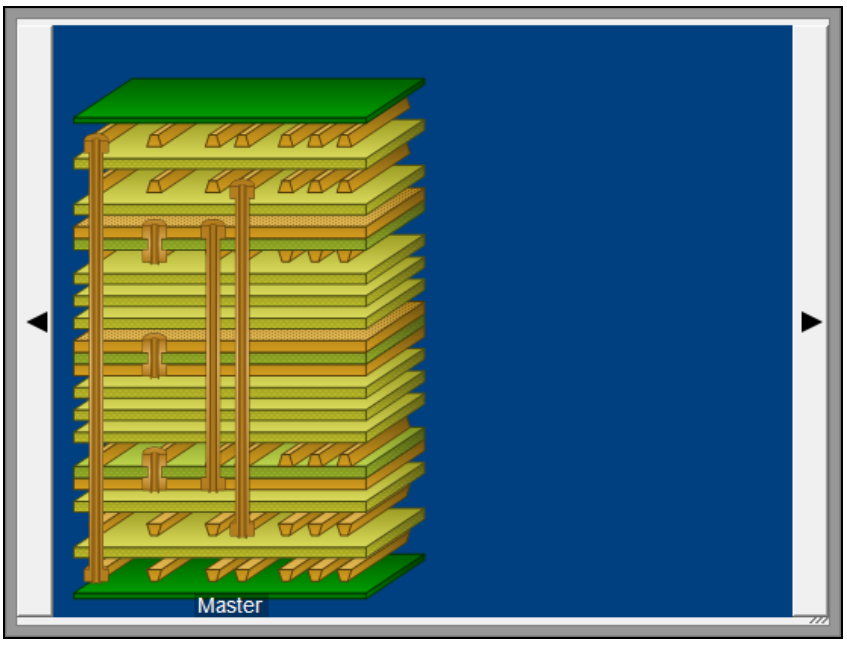


Using the Drill Plan

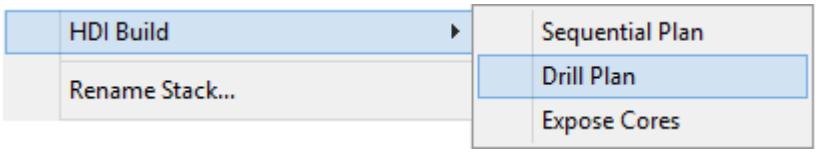
The HDI Build|Drill Plan creates sub-stacks that represents each press cycle from the Master stack based on drill start-end layers. Consider the stackup below – a 10 layer sequential lamination construction.



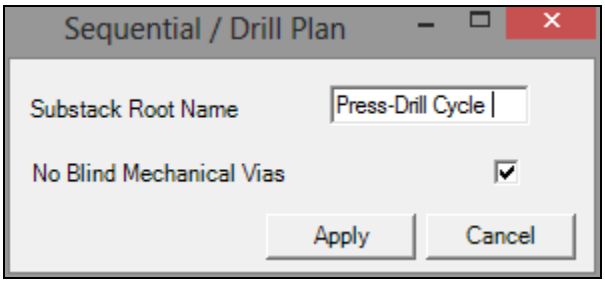
Press the F4 key to open the Navigator



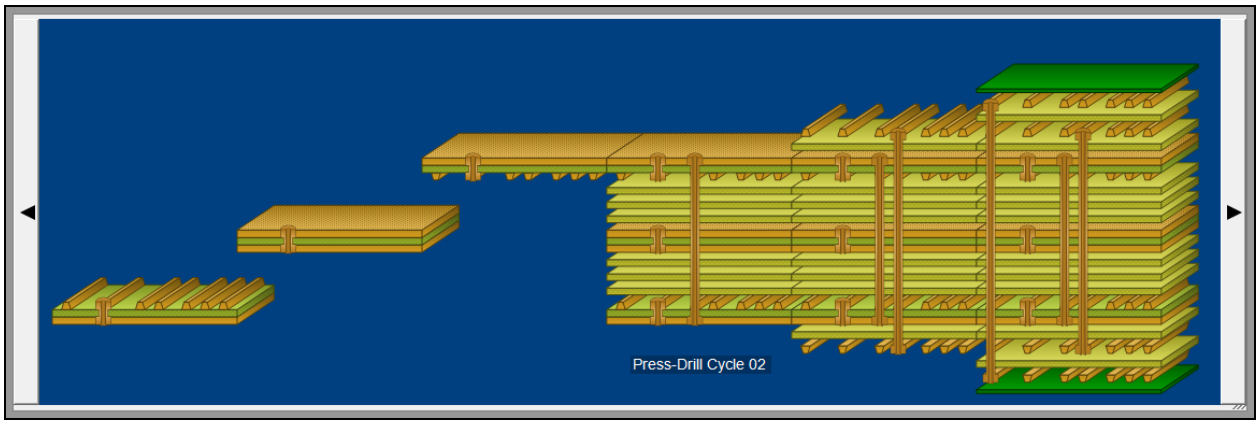
The completed Master stack is displayed. Right click the Navigator and choose HDI Build|Drill Plan.



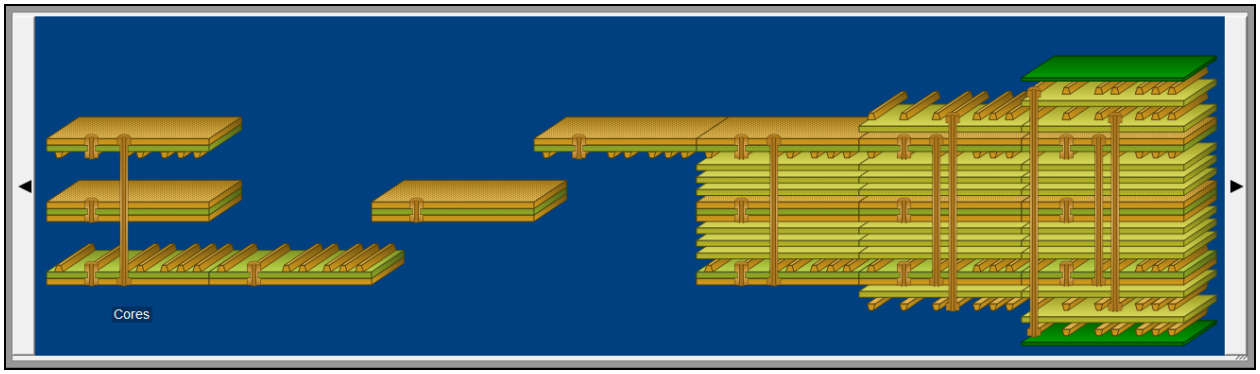
Supply the Sub-stack root name – the name willl be used when numbering the press-drill cycles.



Click Apply – Speedstack documents the build-up stages of the sequential lamination.



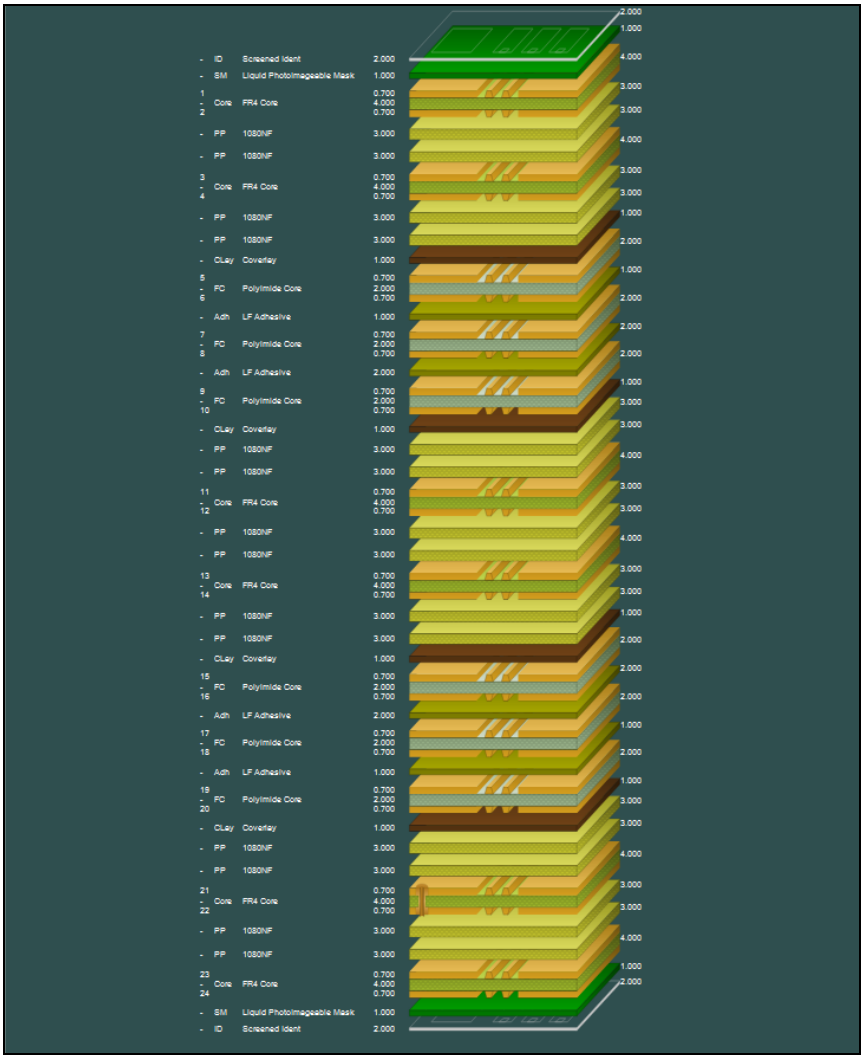
Exposing cores
Right click the Navigator and choose HDI Build|Expose Cores – the cores are shown alongside the press cycles.



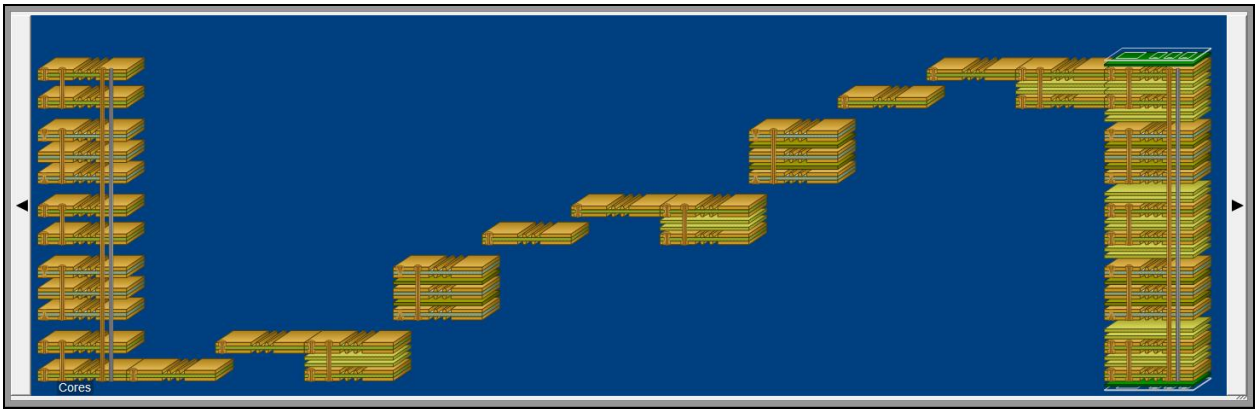
There are no limits to the number of press cycles that may be documented.

Working with multiple press cycles

The stack below is a 24 layer stack with multiple press-drill cycles. Open the Navigator, choose HDI Build|Drill Plan.



The Navigator displays the drill plan and cores below:



Printing the Navigator screen

From the File menu choose Print Technical Report – Speedstack prints the Navigator screen with its press cycles along with individual stack data, impedance data and drill data tables.

Using Speedstack materials libraries

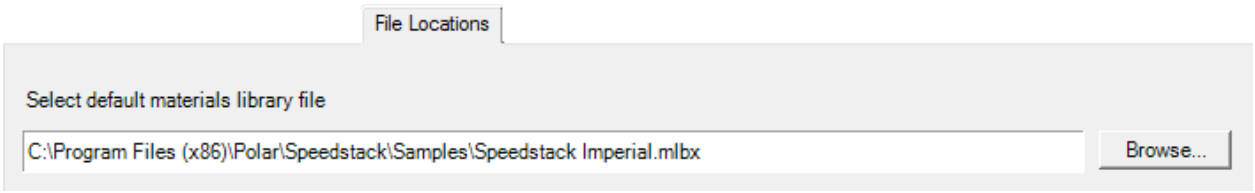
The materials libraries allow designers to manage their own libraries of board materials.

Materials Library

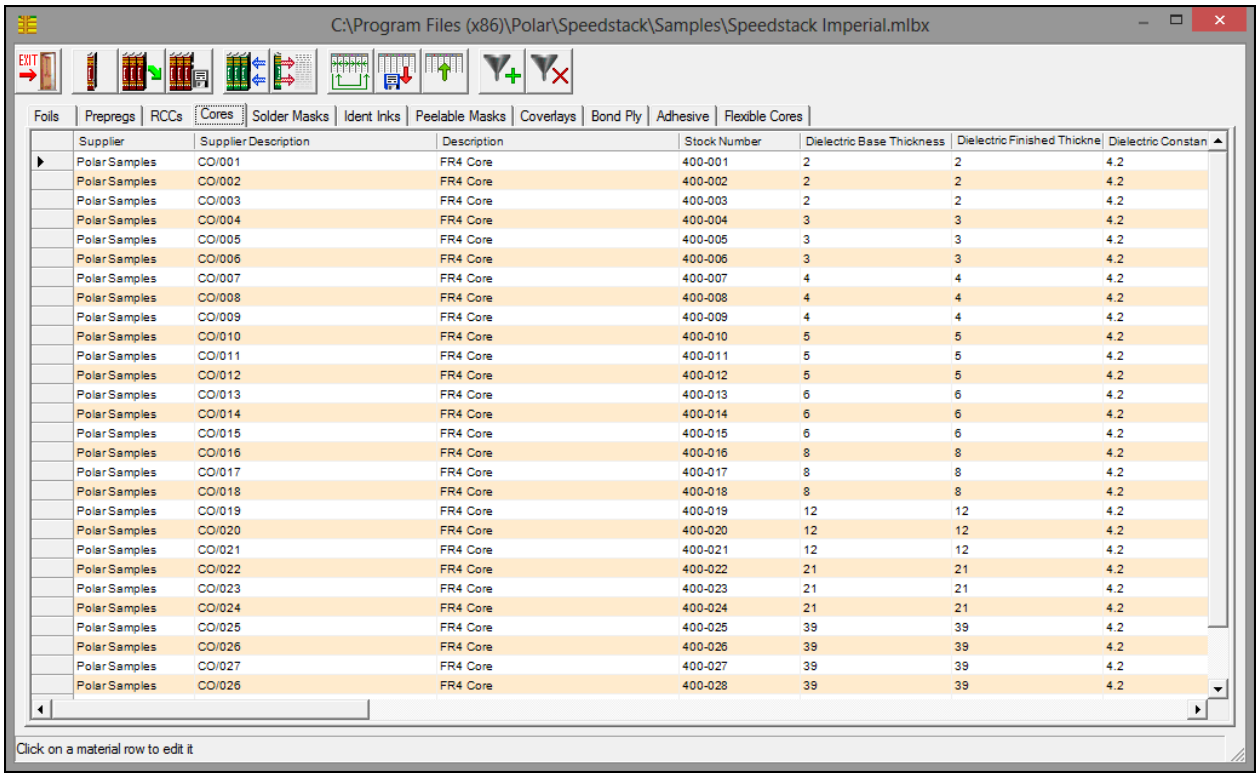
Click the Materials Library button to display the Materials Library window.

Working with the materials libraries

When Speedstack is started the materials library specified as the default materials library file (via Tools|Options|File Locations) is opened.



Each library component type is accessible via its associated tab. Click on the tab to view or edit the component type.



The Materials Library is managed via its toolbar.

Materials library toolbar

Use the toolbar to load and save libraries, import or export libraries, arrange data columns and filter by data field. The Toolbar is shown below.

 Exit Library

 Clear Materials Library

 Open Materials Library

 Save Materials Library

 Import CSV Library

 Export CSV Library

 Select & arrange Column fields

 Save column order

 Load column order

 Set Filter

 Clear Filter

Creating a new library

Clear Materials Library

To create a new library, click Clear Materials Library; the library is removed from the library manager.

Save Materials Library

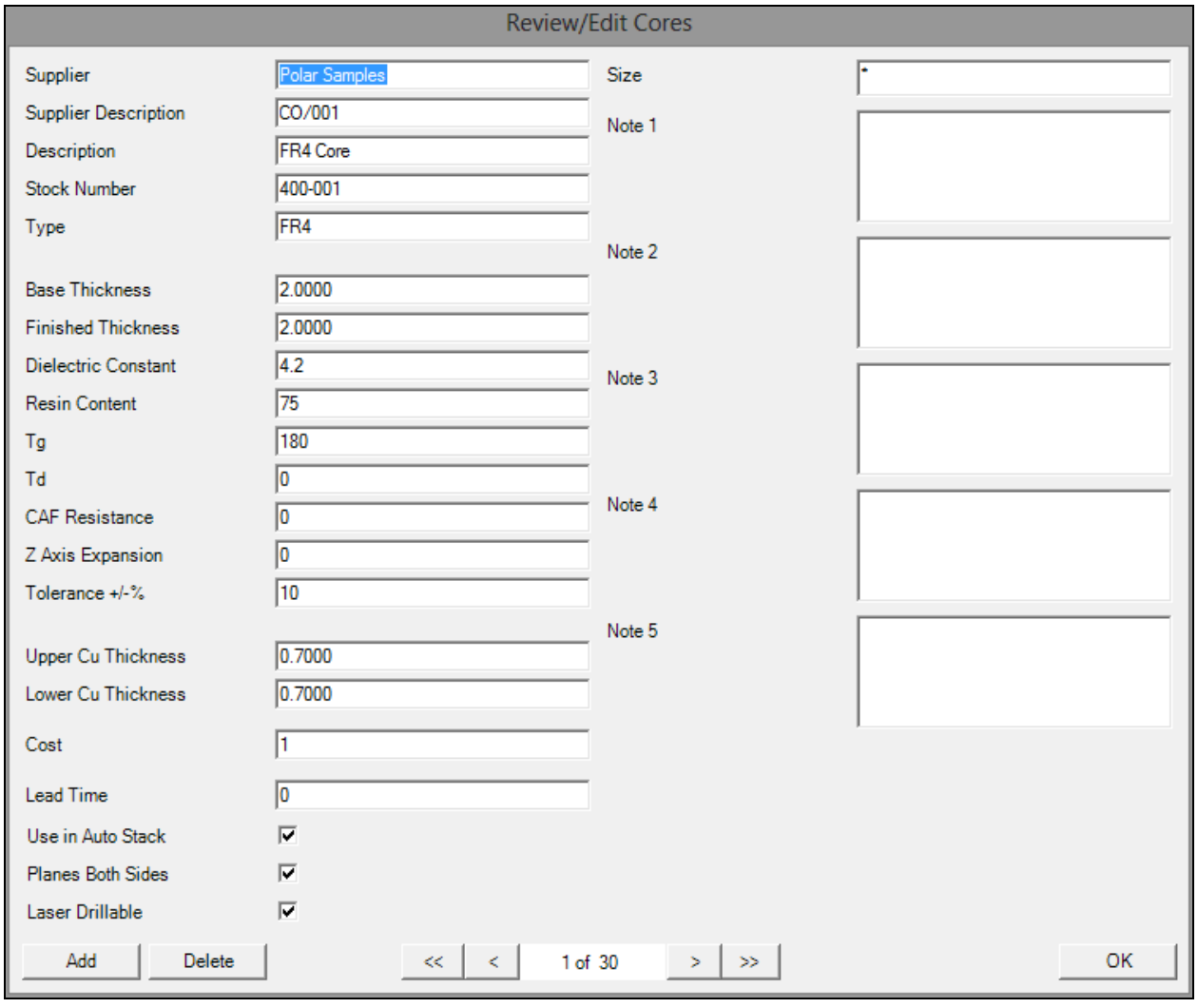
Click Save Materials Library to create the new library. To have the library load as the Speedstack starts, specify it as the default materials library file via Tools|Configuration Options|File Locations.

Adding material to the library

Caution: ensure consistency of units

When defining dimensions, e.g. layer thicknesses, for a stackup ensure that all measurements are defined using the same units (mils, mm, etc) throughout the structure and its associated libraries.

Open the library to be modified. To add materials to a library click the associated component type tab; click onto a material, or empty line. An editing box will open which will contain the material clicked on, or the last material in that type library.



The material can be edited or deleted, or a new material can be added. To speed up the process of adding families of materials, when a material is added the properties of the last material are copied to the new material. The details can then be edited. Clicking OK will add any new materials to the end of the list.

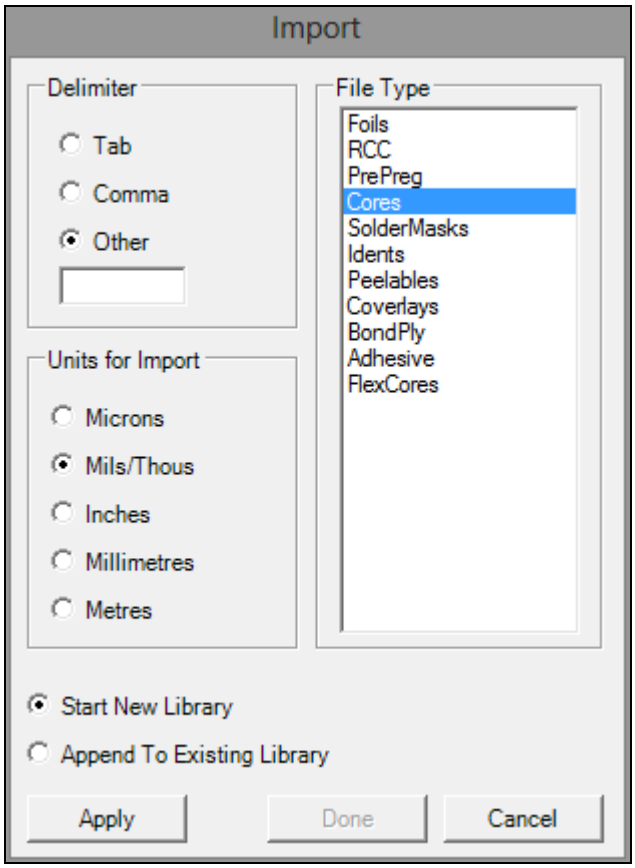
Importing material to the library

Speedstack allows users to add existing material lists to its library; material data must be arranged in the format and order used by the Speedstack library.

Sample files in comma separated value format and Microsoft Excel spreadsheet and template formats suitable for importing to the Speedstack are included in the Speedstack Material Library Import folder.


Import CSV Library

Click the Materials Library button to open the Library, and then click Import CSV Library to open the Import dialog.



Choose Start New Library or Append to Existing Library as appropriate.

Creating a new materials library

Choose the Start New Library option and choose the field delimiter type.

The library import function can accept files in a variety of formats, tab delimited, comma separated and Excel worksheet and template formats.

Sections of the sample files suitable for Speedstack are shown below.

	A	B	C	D	E	F	G	H	I
1	* Cores								
2	*							Dielectric	Dielectric
3	*Type	Supplier	Supplier Description	Description	Stock Number	Upper Cu Thickness	Lower Cu Thickness	Base Thickness	Finished Thickness
4	FR4	Polar Samples	CO/001	FR4 Core	400-001	0.018	0.018	0.05	0.05
5	FR4	Polar Samples	CO/002	FR4 Core	400-002	0.035	0.035	0.05	0.05
6	FR4	Polar Samples	CO/003	FR4 Core	400-003	0.07	0.07	0.05	0.05
7	FR4	Polar Samples	CO/004	FR4 Core	400-004	0.018	0.018	0.075	0.075
8	FR4	Polar Samples	CO/005	FR4 Core	400-005	0.035	0.035	0.075	0.075
9	FR4	Polar Samples	CO/006	FR4 Core	400-006	0.07	0.07	0.075	0.075
10	FR4	Polar Samples	CO/007	FR4 Core	400-007	0.018	0.018	0.1	0.1
11	FR4	Polar Samples	CO/008	FR4 Core	400-008	0.035	0.035	0.1	0.1

Sample library file in Microsoft Excel format

```
* Cores,,,,,,,,,,,,,,,,,,,,,,,,
*,,,,,,,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,Dielectric,,,,,,,,
*Type,Supplier,Supplier Description,Description,Stock Number,Upper Cu Thickness,Lower Cu Thickness,Base Thickness,Finished Thickness,
Content,Tg,Td,CAF Resistance,ZAxisExpansion,ExcessResin,Tolerance,Cost,Lead Time,Notes 1,Notes 2,Notes 3,Notes 4,Notes 5,Size
FR4,Polar Samples,CO/001,FR4 Core,400-001,0.018,0.018,0.05,0.05,4.2,75,180,0,0,0,0,10,0,0,,,,,,*
FR4,Polar Samples,CO/002,FR4 Core,400-002,0.035,0.035,0.05,0.05,4.2,75,180,0,0,0,0,10,0,0,,,,,,*
FR4,Polar Samples,CO/003,FR4 Core,400-003,0.07,0.07,0.05,0.05,4.2,75,180,0,0,0,0,10,0,0,,,,,,*
FR4,Polar Samples,CO/004,FR4 Core,400-004,0.018,0.018,0.075,0.075,4.2,60,180,0,0,0,0,10,0,0,,,,,,*
```

Sample library file in comma separated format

Files for importing into the library must be in the above format, with columns in the correct order.

Specify the delimiter if necessary and choose the file type (Foil, RCC, Prepreg, etc.) and units for import and click Apply. Choose the file from the list displayed in the Open dialog and click Open. Repeat the procedure for every file type; Click Done when all file types have been imported.

Save the file as a .mlbx library file.

Adding material data to an existing library

To add material data to an existing library, open the library click Import CSV Library, click the Append to Existing Library and click Apply. Choose the .csv or .txt file and click Open then click Done. Save the modified Library file as a .mlbx file.

Selecting Materials from the Library

Column Order (Materials Library)

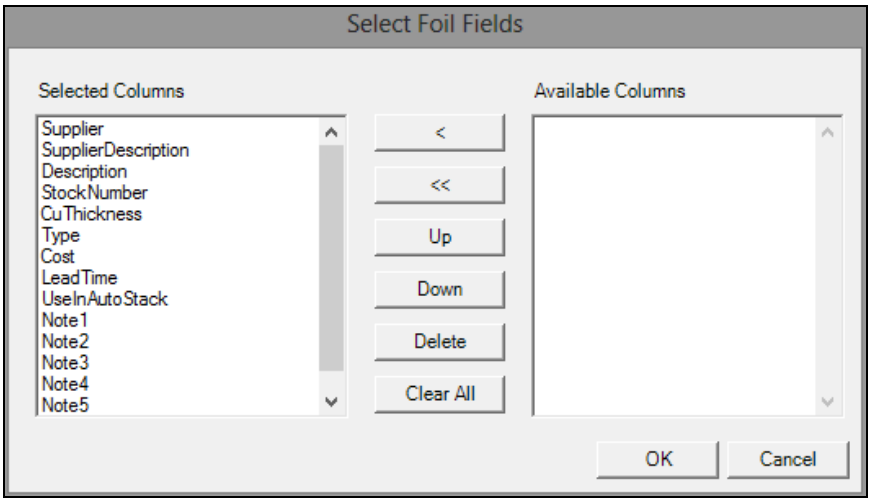
The default setting displays all columns. The columns displayed and the order they are displayed can be set in the materials Library form.

Arranging Columns in Library Forms

The Library windows can be customised in respect of which columns to display and in which order.

Arrange Columns

Click the Go to Materials Library button and select Arrange Columns; the dialog associated with the selected material tab (Foils, Prepregs, etc.) is opened.



The Left box of the dialog shows the columns that will be displayed and the order top to bottom is the order they will be displayed left to right in the library window.

Click OK to return to the Materials Library, which will show the columns as set.


Save Column Order


Load Column Order

Until the column order is saved the column order is only available during the current session. Click Save Column Order to define the selected column order as the default order whenever the program is run.

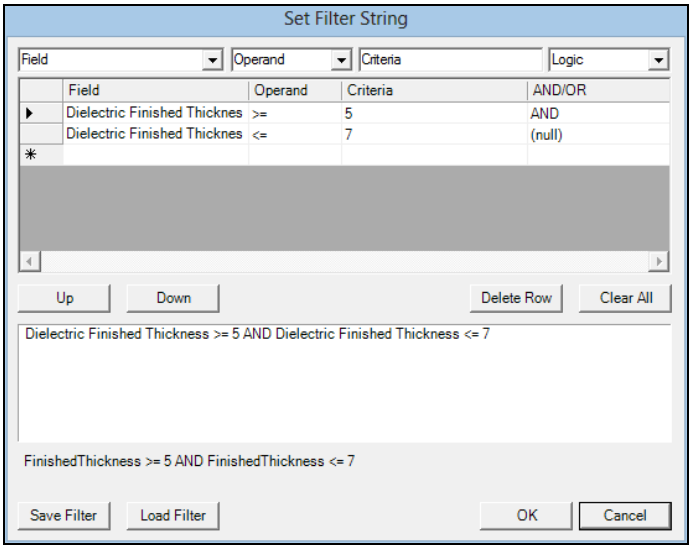
Click Load column Order to apply a saved column arrangement.

Filtering Materials

When adding or swapping materials, available materials (Foils, Prepregs, etc.) are listed in the associated material library dialog. Lists can be filtered for materials matching desired parameters (dielectric thickness, Er, etc.)


.*Set Filter*

In the library window click the Set Filter to display the Set Filter String dialog.



Filter strings can be created and saved for future use. To save click Save Filter, to recall an existing filter click the Load Filter button, choose the filter (.mlf) file and click OK.

Building the filter string

Build the filter string by selecting parameters, operands and criteria from the drop-down boxes. If the AND/OR box is selected another row is automatically added to the grid. The filter language is a sub-set of common database commands.

Use the Up/Down buttons to select a row for deletion. The arrowhead at the side of the grid indicates the selected row.

Click OK to apply the filter immediately to the selected library. If desired, save the filter string for future use. (The Speedstack provides for interaction between the library dialog and filter form. This allows complex strings to be built line-by-line and tested without saving until the string is completed.)

When saving the filter choose a descriptive name for the file that reflects the purpose of the filter. The Speedstack automatically names the files for the material type.

Using the Like operator

Use the Like operand to filter results via wild card characters. The characters * and % can be used to represent groups of starting or ending characters.

For example, specifying Like ‘Po%’ or ‘Po*’ as the criterion for the Suppliers field will show all suppliers beginning with ‘Po’.

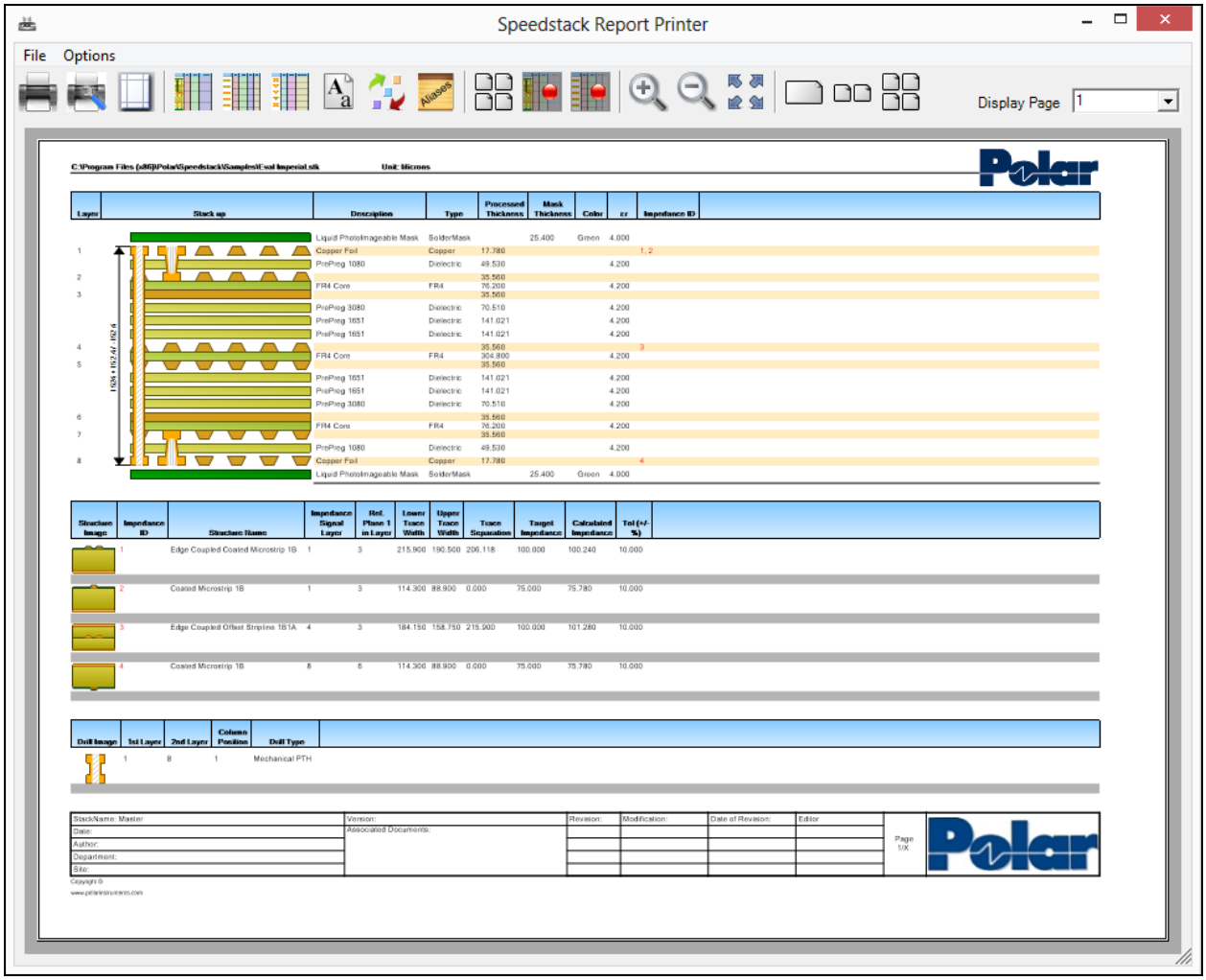
Similarly, specifying Like ‘%es’ or ‘*es’ as the criterion for the Suppliers field will show all suppliers ending with ‘es’.


Clear Filter

Click the Clear Filter to remove the filter and display all materials of the selected type.

Printing stackup information

To print the stackup information, choose the Print command. Print Technical Report includes stack details, controlled impedance structures, drill specifications and information entered into the Stack File Properties.



Speedstack Report Printer toolbar

The Speedstack Report Printer toolbar provides shortcut access to the most commonly used printing commands.

Use these commands to set up the printer, page orientation and margins, font size and printing order, select data columns for display, display or suppress data tables and choose the on-screen zoom levels. Button functions are described below.

 Send report to printer

 Print set up – choose printer, print range, copies

 Page set up – orientation and margins

 Select stack data columns

 Select impedance data columns

 Select drill data columns

 Change font size

 Select stack/drills/impedance/notes print order

 Set note field aliases

 Display/suppress stack data table

 Display/suppress controlled impedance data table

 Display/suppress drill data table

 Zoom in

 Zoom out

 Fit page to viewer

 Preview one page

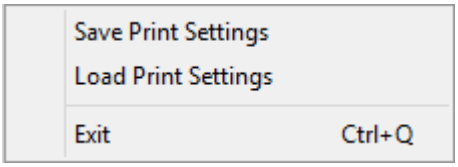
 Preview two pages

 Preview four pages

Speedstack Report Printer menu system

File menu

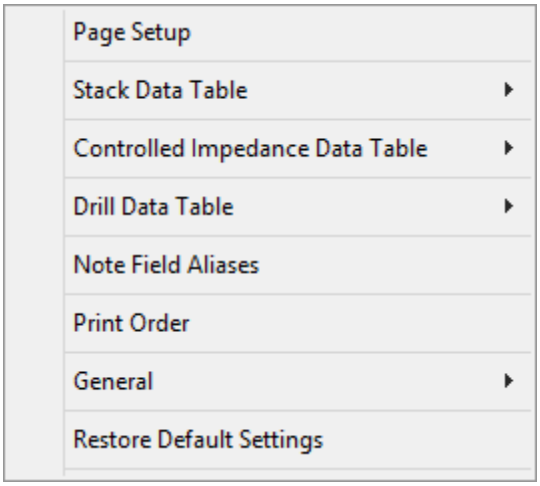
Use the File menu under the Printing window to save and load print settings.



Whichever settings were last used in a session will become the default when the Printing window is next loaded.

Options menu

The Speedstack Report Printer Options menu contains all the settings for printing.

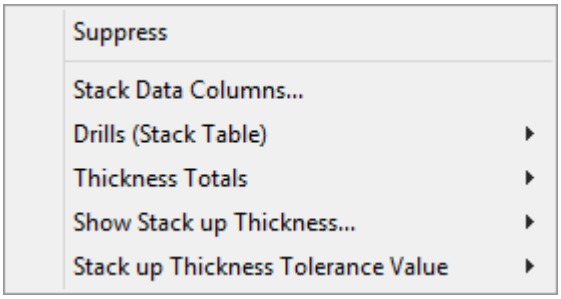


Page Setup

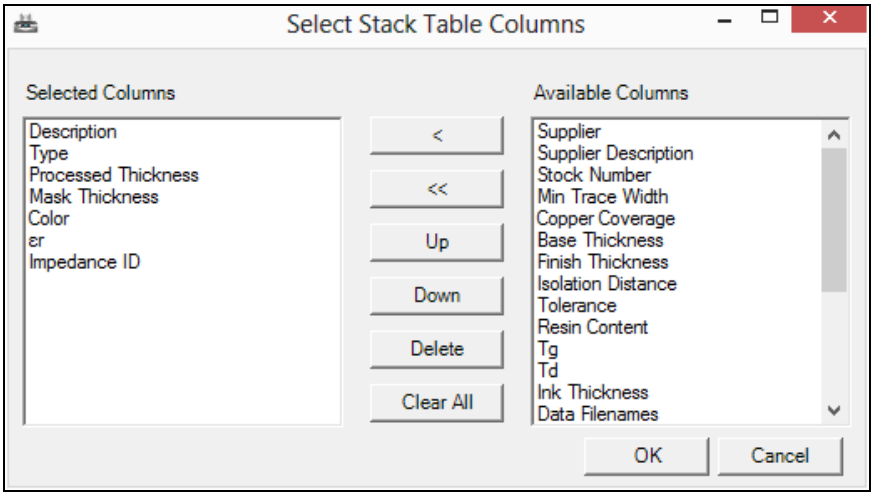
Page Setup displays the Page Setup dialog to change paper size and orientation, paper source and margins.

Stack Data Table

The Stack Data Table commands allow for optional display of stack parameters, drills, thickness totals and tolerances.



Stack Data Columns: select, combine and order the data columns available for the stack as desired.



Use the Drills (Stack Table) command to show or hide the drills in the stackup graphic in the Stack Table.

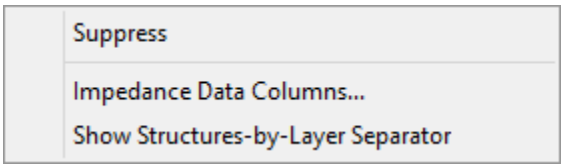
The Thickness Totals provides optional display of the sum of materials thicknesses, copper, dielectric, solder mask and the stackup – with and without the solder mask thickness.

Use the Show Stack Up Thickness command to display or hide the target or calculated values of total stack thickness.

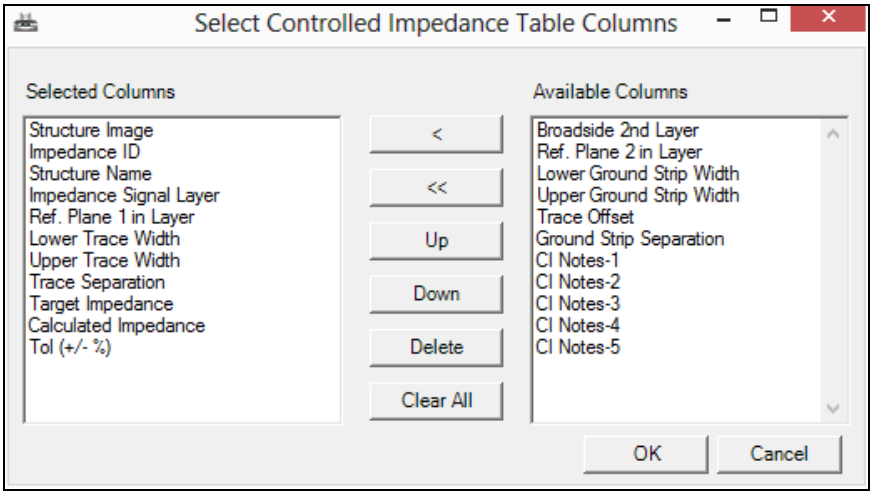
When the target value of the Stack Up thickness is chosen the Stack Up Thickness Tolerance values can be displayed as percentages of the target stack thickness or as actual values.

Controlled Impedance Data Table

Use the Controlled Impedance Data Table options to show or hide the controlled impedance structures and parameters.



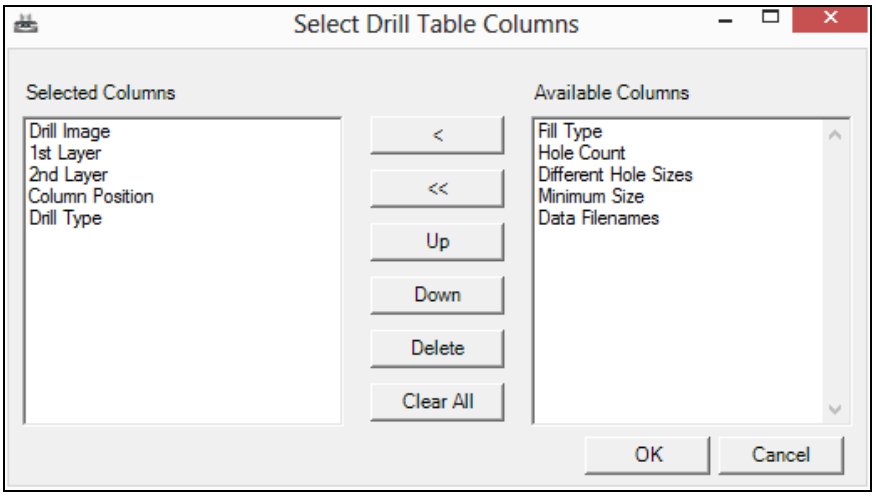
Impedance Data columns can be selected for display and ordered as required. Choose the parameters for display from the Available Columns pane and change the order of display using the Up and Down buttons.



Within the Impedance Data Table structures can be grouped by layer; choose Show Structures-By-Layer Separator. The Separator will add a black structure separator bar on the print out between structure groups, allowing the structures to be sorted by layer number rather than the order that the structures are added to the stack.

Drill DataTable

Use the Drill Data Table command to show or hide the table of drill parameters and to select and order parameter values for display.

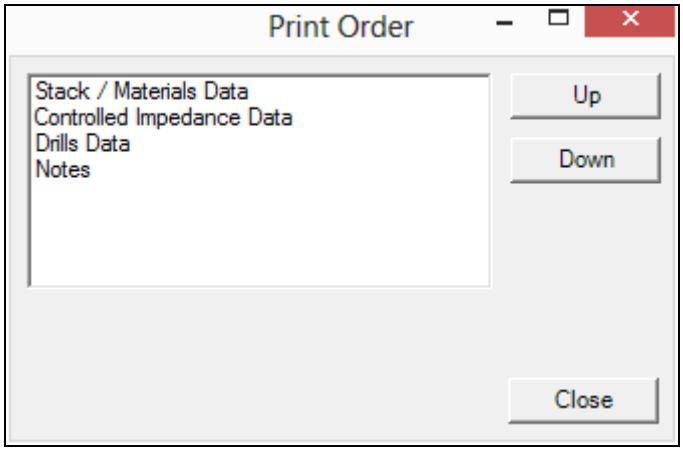


Note Field Aliases

Note Field Aliases allows for the free-text note fields (for the Stack and Controlled impedance tables) to be given descriptive names.

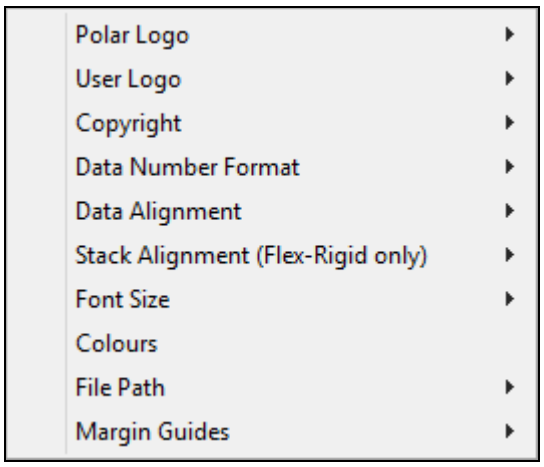
Print Order

Use the Print Order dialog to move the Controlled Impedance Table, Drill Tables and Notes sections up or down within the report.



Note: the Stack/Materials data Table cannot be reordered and must remain the first item in the print order.

General options
Use the General Options to specify



Polar Logo: toggles on and off the Polar Instruments logo.

User Logo: toggles on and off the user-defined logo (as set in the application configuration).

Copyright: toggles on and off the copyright information and allows copyright test to be edited.

Data Number Format: sets the precision of numeric data in the printout.

Data Alignment: specifies alignment (left, centre, etc.) for stack, impedance and drill data.

Stack Alignment (Flex-Rigid only): – Align to Master Stack allows the vertical position of sub-stacks (printed on separate pages within the report) to be preserved with respect to the master stack; Align to Page Top presents each sub-stack at the top of each page.

Colours: allows for the colours of items within the report to be customised. Click Override Default Colours and Change to

specify the new colour. Click Reset All to return to the default colours.

File Path: toggles on and off the file path/file name

Margin Guides: toggles on and off boundary markings (in the user selected units.) These match the Speedstack units selected within the Stackup Editor | Units menu.

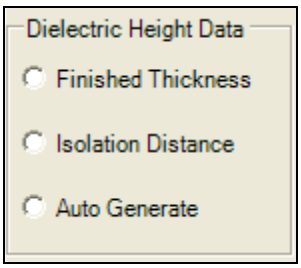
The margin guides allow for display of the printable area of the page – which can vary depending upon the device – even though the page size remains the same. (With some devices the report cannot use the full extents of the page.)

Appendix A

Creating a stack with Autostack

The Polar Instruments Speedstack PCB Stackup Builder allows users to create and modify stacks manually via the Stack Editor or automatically using Autostack. This section steps through the process of using Autostack to create a simple stack from a set of manufacturer's data. When completed the stack can be transferred to the Stack Editor for manual editing.

Autostack offers three methods of specifying dielectric height, Finished thickness, Isolation distance and Auto Generate.



In this example it’s assumed the values of dielectric height are unknown and select the Auto Generate method. For a discussion of calculating dielectric height with Speedstack refer to Polar Instruments Application Note AP507.

When using Auto Generate the dielectric heights are calculated automatically so only the following information is required (the manufacturer's sample data values chosen for this example are typical for a standard PCI card):

- The overall board thickness – in this example we specify 64 mil (1.6mm) ± 10%.
- Build type (foil or core)
- A reference dielectric constant – in this example, 4.2.
- The controlled impedance requirements:

  – 50 ohm (±10%) single-ended on Layer 1 referenced to Layer 2. Trace width (W1) 22 mil ~ 0.56mm.

  – 100 Ohm (±10%) differential on Layer 1 referenced to Layer 2. Trace width (W1) 13 mil ~ 0.33mm, Separation (S1) – 9 mil ~ 0.23mm.

– 100 Ohm (±10%) differential on Layer 3 referenced to Layers 2 and 5. Trace width (W1) 6 mil ~ 0.15mm, Separation (S1) – 7.5 mil ~ 0.19mm.

– 75 Ohm (±10%) single-ended on Layer 6 referenced to Layer 5. Trace width (W1) 9.5 mil ~ 0.24mm.

- The trace dimensions and their tolerances – ± 20%.
- Finished copper weights – 1oz, 1.4 mil (35um).
- Solder mask requirements.

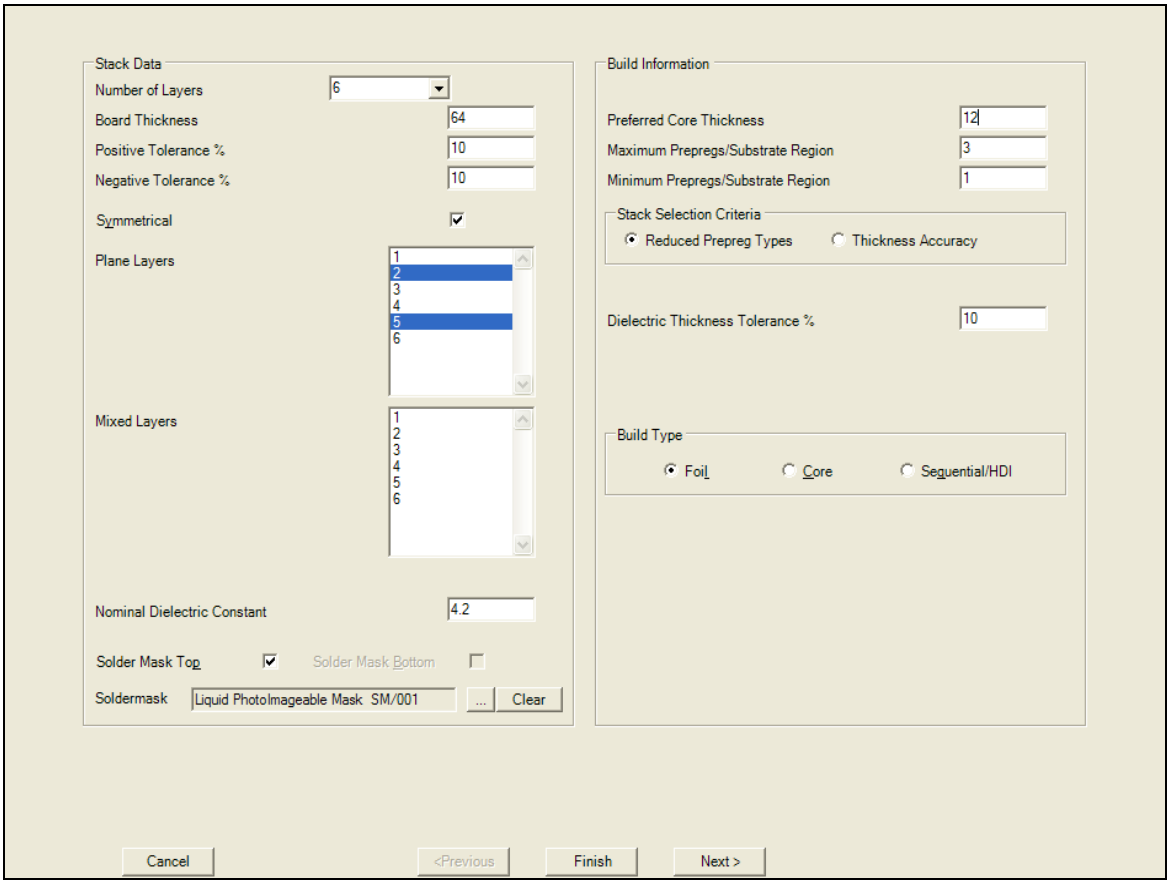
Inputting designers' information into Speedstack

When Speedstack is first opened the Stack Builder screen is displayed. The Stack Builder screen allows for selection between stack data, the project defaults and stack overview.

The Stack Data screen provides a data entry interface for specifying stack parameters and predefined material filters.

Creating a new stack

From the File menu Choose New to begin a new stack. The Stack Data screen is displayed; enter the values from the manufacturer's data:



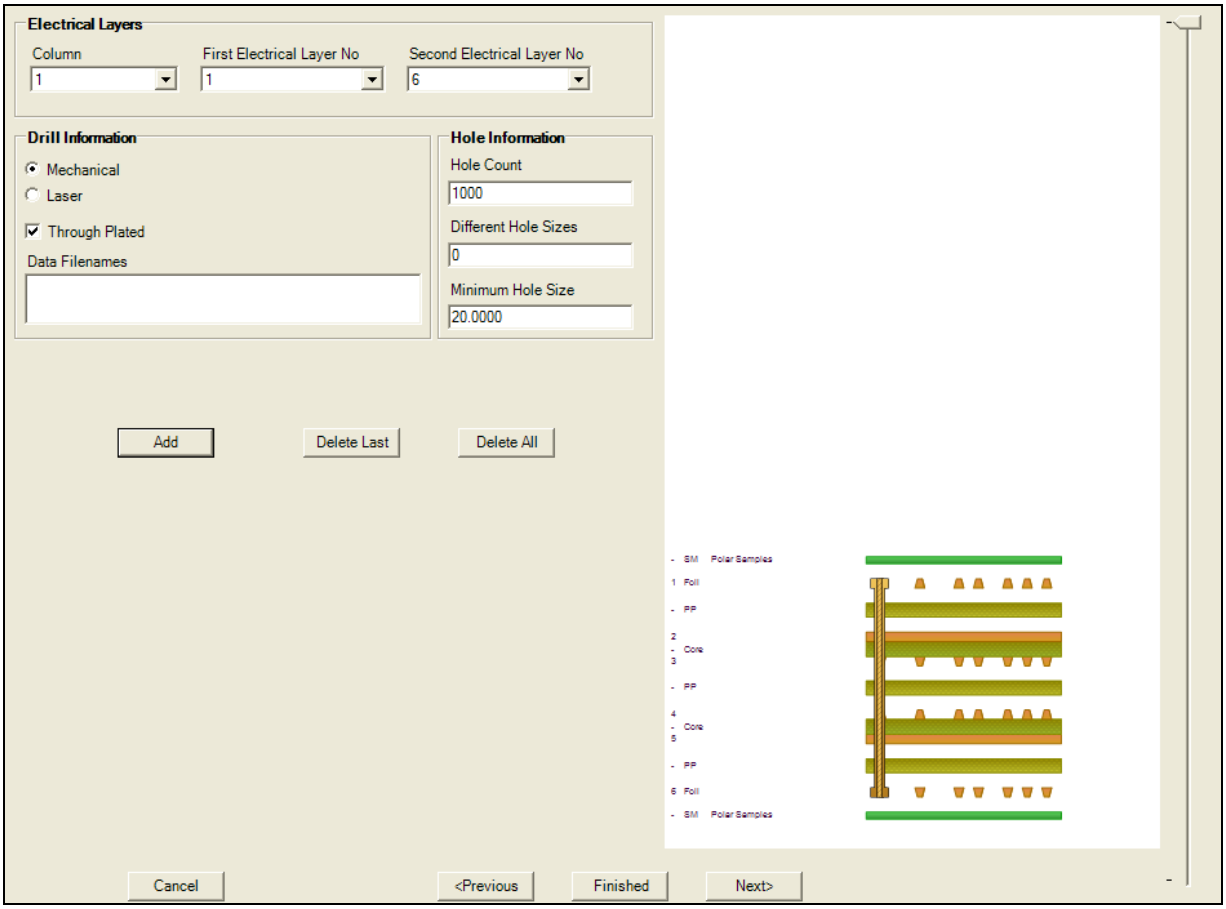
Adding stack data

For this example we specify a board thickness of 64 mil (1.6mm) and a tolerance of 10%.

We specify a symmetrical build, designate layers 2 and 5 plane layers and choose a solder mask from the materials library. Note that for a symmetrical build it is only necessary to specify a mask for the top layer.

We specify a dielectric constant of 4.2, a preferred core thickness of 12 mil and a maximum of 3 and minimum of 1 prepreg per substrate region and choose to build the stack with a minimum of prepreg types (in some applications accuracy of finished thickness will be of greater importance than reducing the number of prepreg types).

For this example we specify a Foil build. Click Next to progress to the Add Drills screen.

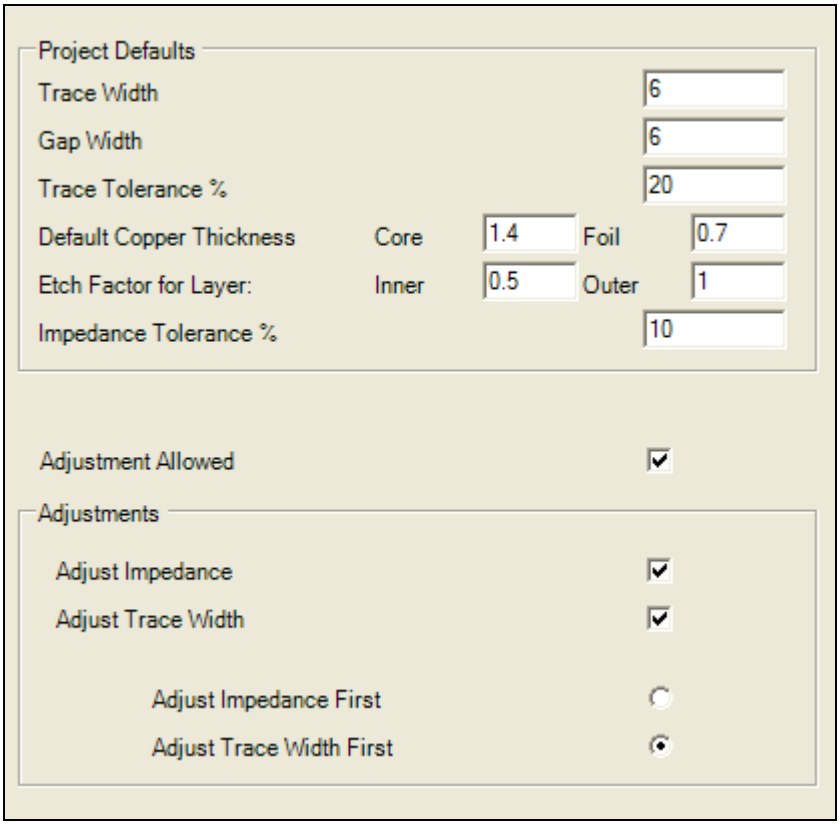


Adding drills

From the Add Drills screen choose the drill type, mechanical or laser and, for each drill, the first and second electrical layers; click Add. Up to six drill columns can be specified; for this example we specify a minimum hole size of 20 mil.

Changes made to the stack are reflected in the stack overview graphic. Click Next to display the Project Defaults screen

Use the Defaults screen to provide controlled impedance structure defaults for the current Autostack session.



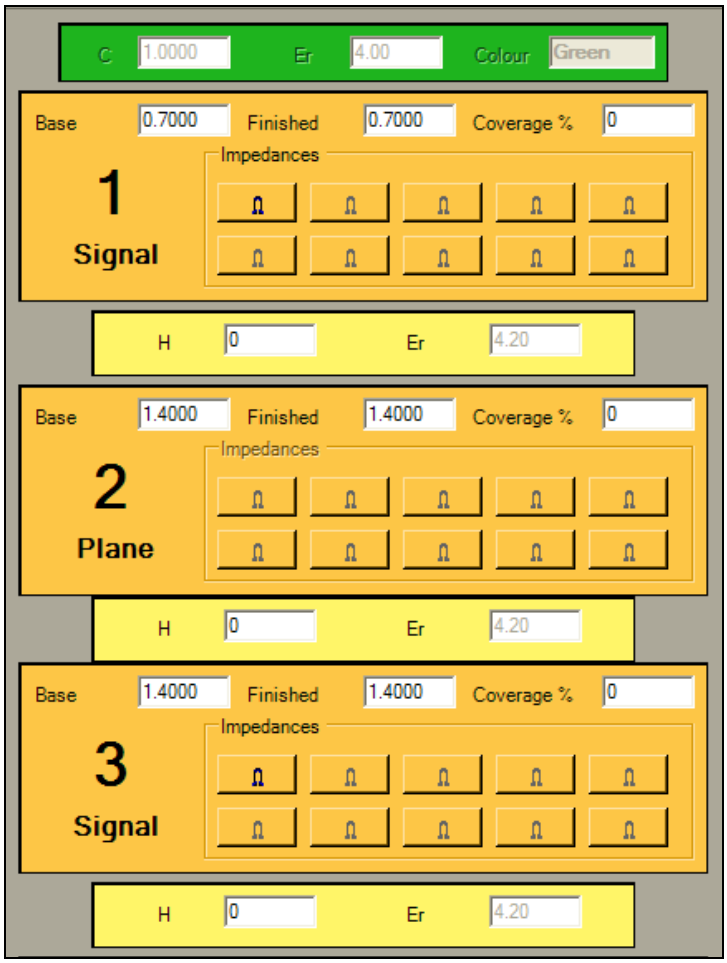
The Project Defaults screen provides default values as a starting point for the impedance structures and other settings and provides for minor adjustments of impedance and trace widths to allow the Si8000/SI9000 goal seeker to produce a stack meeting all specifications.

Set trace and gap widths, copper weights and etch factors to the values shown.

Impedance and trace width adjustments
Click the Adjustments Allowed check box to enable the adjustments options and allow the target impedance and the trace width to be adjusted within specifications; allow the trace width to be changed first. Click Finish; the screen returns to the Stack Definition Page with its graphical representation of the data fields.

With the stack defined we can add the finished copper weights and the impedance structures. In this example symmetrical mode has been selected so layer type and H values are disabled on the lower half of the stackup.

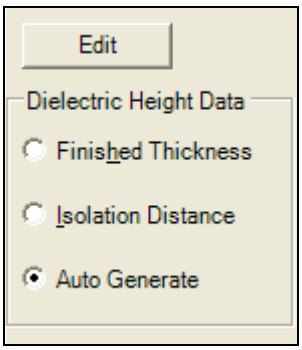
Note: Although the stack is defined as symmetrical, controlled impedance structures can be specified on an individual layer basis.



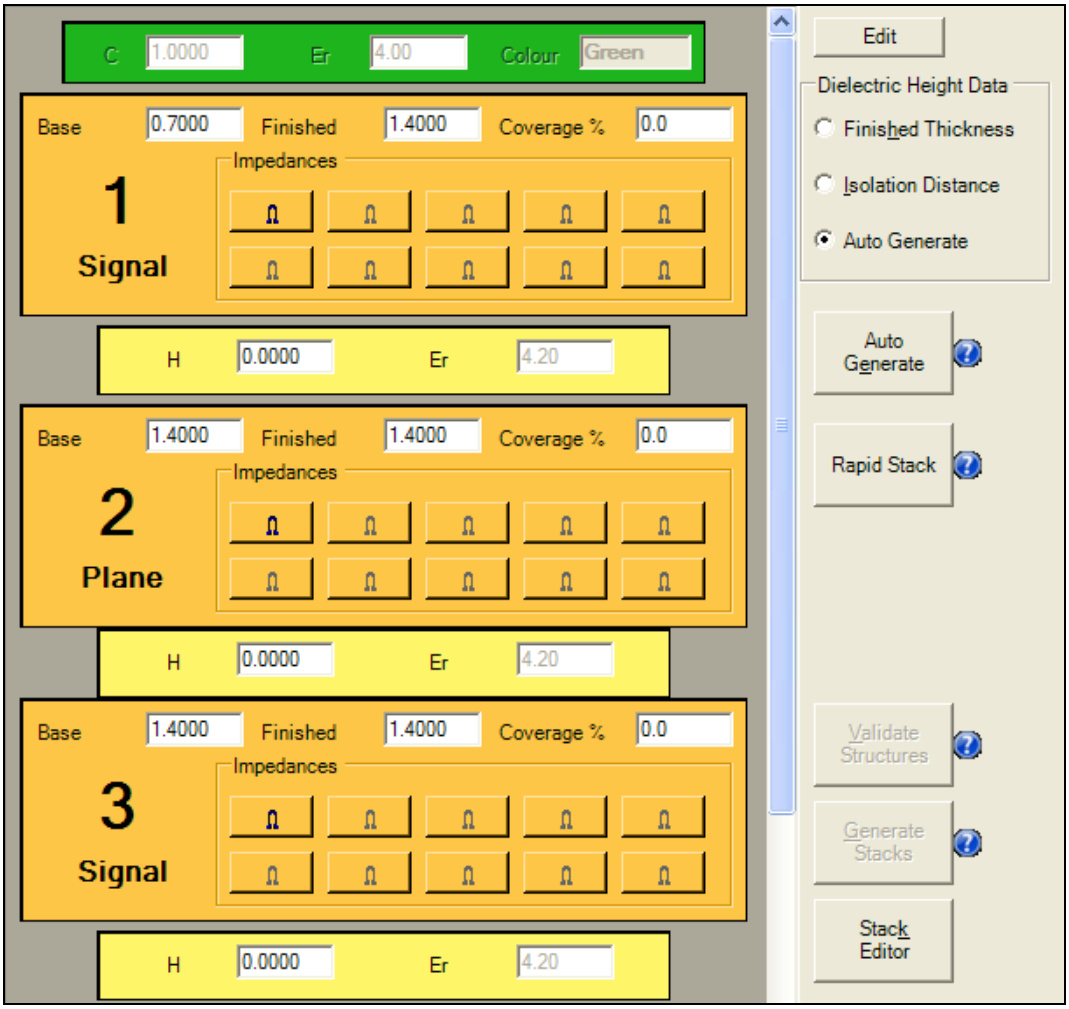
Adding copper weights

The stack is symmetrical so only the top half of the stack is shown. The finished copper weights – 1.4 mil ~ 35um – are taken from the sample designer supplied data. Note that the signal and plane layers and core and prepreg layers are shown as designated.

From Dielectric Height Data select the Auto Generate option to enable Autostack to derive dielectric heights automatically.

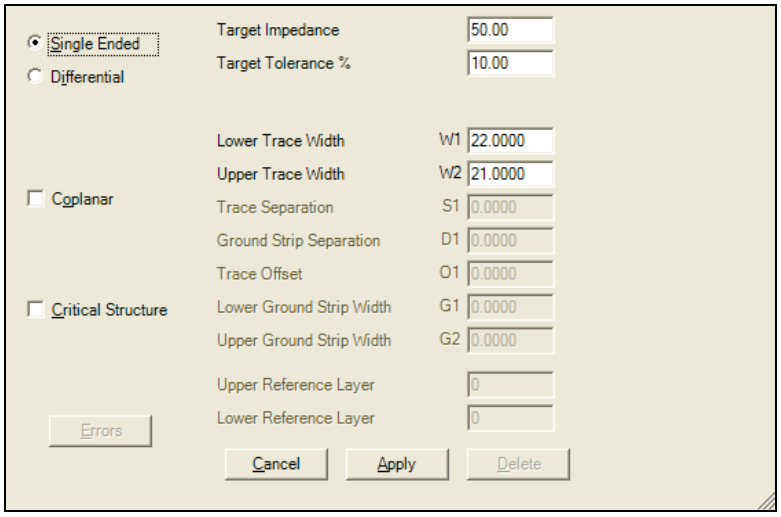


As symmetrical mode has been specified it is not necessary to setup layers 4, 5 and 6. Stack definition data supplied for layers 1 – 3 will be reflected into the lower half of the stack.

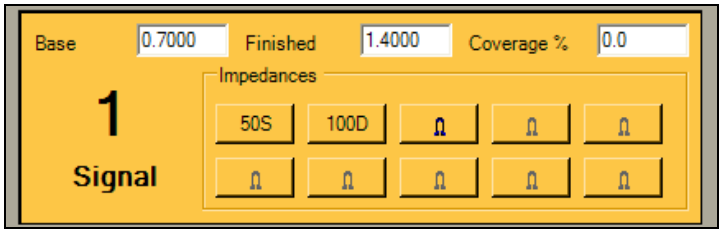


Adding impedance structures

Click the upper left Impedance button on Layer 1 to specify the first impedance structure via the Structure Data dialog – 50 ohm (±10%) single-ended on layer 1 referenced to layer 2. Trace width (W1) 22 mil ~ 0.56mm.



Click Apply and repeat for the remaining structures on their associated layers.



Up to ten impedance structures may be specified for each layer, note that for each impedance defined the omega symbol has been replaced with text describing the structure.

Click Auto Generate to create a set of candidate stacks that match the stack definition criteria.

Cost	Number Of	Prepreg Type	Lead Time	σ	-3 σ	Nominal Thickness	+3 σ
64	7	2	0	1.4062	61.9633	66.16	70.4003
65	7	2	0	0.9849	62.9306	65.86	68.84
66	6	1	0	2.1179	59.7689	66.16	72.4762
67	6	2	0	1.8902	62.3368	68.06	73.6779
67	7	2	0	1.4114	61.8894	66.16	70.3575
68	7	2	0	1.8455	62.5323	68.16	73.6055
68	8	2	0	1.5689	61.4105	66.16	70.8241
68	8	2	0	1.6158	61.2288	66.06	70.9238
69	9	1	0	1.6311	61.168	66.16	70.9544
70	9	2	0	1.7704	62.8093	68.16	73.4316

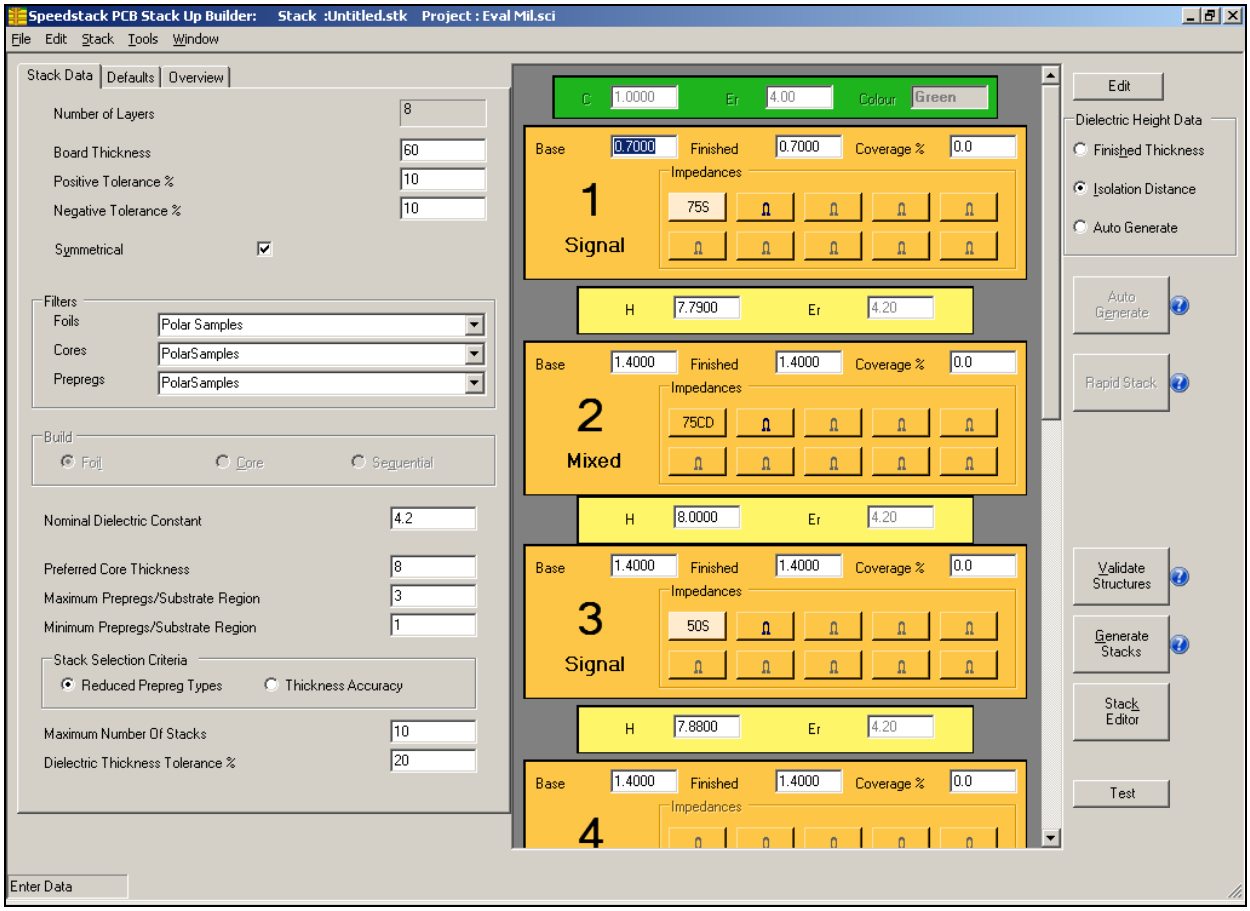
Using the Stack Preview screen, examine each stack and sort the stacks by cost, mean thickness, lead time for materials and the sigma functions. It will normally be most appropriate to choose the most cost effective or the most accurate stack, taking into account the material costs and availability, process costs, design parameters, etc.

Click Retain original specified trace width, select the stack and click Apply. With the virtual stack chosen Speedstack will re-validate all impedance structures and open the Stack Editor window. See *Using the Speedstack Stackup Builder* for a detailed discussion of the Stack Editor.

The Speedstack Stackup Builder

Double-click the Speedstack icon to start the Speedstack program.

In installations with the Autostack (Virtual Stack Realization) feature activated Speedstack opens the Stack Definition screen; otherwise the Stack up Editor screen is displayed.



The Stack Definition screen

This section provides a brief introduction to the Autostack process. Detailed Speedstack definition training documentation is available from Polar Instruments.

Creating a new stack with Autostack

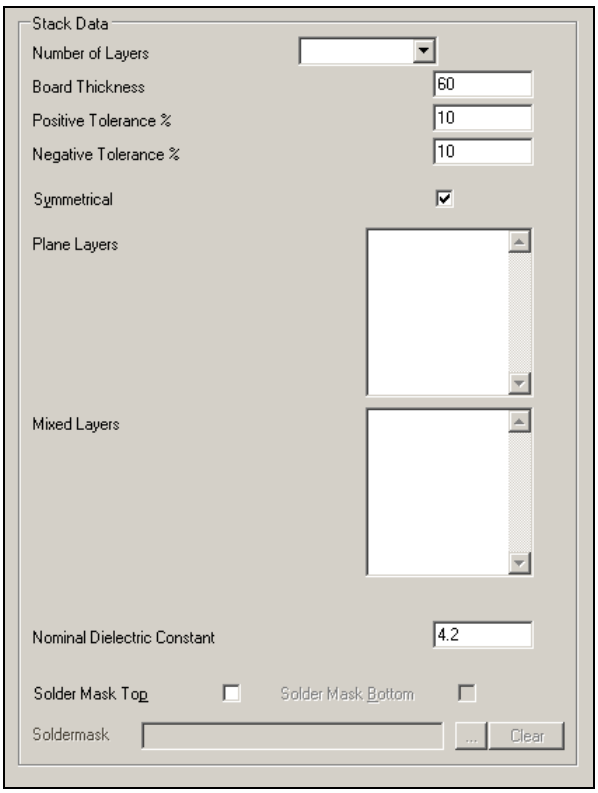
From the File menu select New to initiate a new stack. Most initial data are provided from the Configuration Options.

Stack data

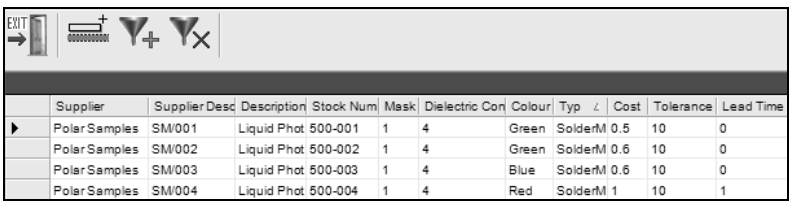
In the Stack Data section, select the required number of electrical layers and specify the board thickness and the dimension tolerances.

Specify the plane layers, mixed layers, dielectric constant (Er) and solder mask type.

If Symmetrical build is specified it will only be necessary to define the “top” half of the stack; Speedstack will reflect the supplied settings into the lower half of the stack.



If solder mask is to be used click the Solder Mask browse button to open the library at the Solder Mask database.



	Supplier	Supplier Desc	Description	Stock Num	Mask	Dielectric Con	Colour	Typ	Cost	Tolerance	Lead Time
▶	Polar Samples	SM/001	Liquid Phot	500-001	1	4	Green	SolderM	0.5	10	0
	Polar Samples	SM/002	Liquid Phot	500-002	1	4	Green	SolderM	0.6	10	0
	Polar Samples	SM/003	Liquid Phot	500-003	1	4	Blue	SolderM	0.6	10	0
	Polar Samples	SM/004	Liquid Phot	500-004	1	4	Red	SolderM	1	10	1

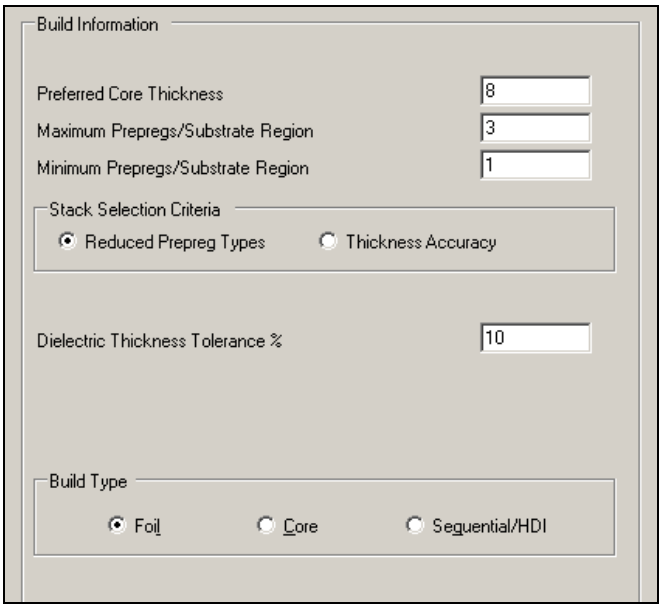
Select the mask and click the Add Material Above button; mask will be added to the top side (or both sides for a symmetrical build.)

Build Information

Use the Build Information section to refine the build parameters used by the Virtual Stack Realization engine.

Specify the preferred core thickness and the maximum and minimum numbers of prepregs per substrate; use the Stack Selection Criteria option box to direct the Autostack engine to design the stack for the lowest number of prepreg types or for accuracy of finished thickness.

Specify the tolerance for dielectric thickness and the build type (Foil, Core or Sequential build).



If required these defaults can be changed (for this project) on further pages. In addition, drills can be added or lamination and HDI sequences can be defined.

With the stack defined, for Foil or Core builds click Finish; all other parameters will be defined from the Tools/Options settings.

If Sequential/HDI is chosen via the Build Information screen click ‘Next’ to define the sequence.

Defining sequential builds

Sequential build toolbar

Type I stack

Type II stack

Type III stack

Set number of foils added to foil build

Foil build subsection with one core

Foil build subsection with two cores

Foil build subsection with three cores

Set number of cores in foil build subsection

Reset to foils and prepregs

Reset to foil build

Reset to core build

Upon first entry to the Define Sequential Build screen the stack view shows that the stack consists simply of foils and prepregs. The stack can then be defined as required.

Using the toolbar buttons shown above preset combinations can be defined.

Sequential build combinations

Name	Tooltip	Purpose
1N1	Type I	Makes foil build stack with 1 extra foil on either side
2N2	Type II	Makes foil build stack with 2 extra foil on either side
3N3	Type III	Makes foil build stack with 3 extra foil on either side
XNX	Set number of foils to be added to foil build	Makes foil build stack with X extra foil on either side
F1CF	Foil build sub-section with 1 core	Makes multiples of foil built sub-sections with 1 core in sub-section
F2CF	Foil build sub-section with 2 cores	Makes multiples of foil built sub-sections with 2 cores in sub-section
F3CF	Foil build sub-section with 3 cores	Makes multiples of foil built sub-sections with 3 cores in sub-section
FXCF	Foil build sub-section with X cores	Makes multiples of foil built sub-sections with X cores in sub-section
Reset	Reset to Foils and Prepregs	Makes stack simply of foils and prepregs probably as a start point for a more complex laminated stack
FB	Reset to Foil Build	Makes a foil build stack probably as a start point for a more complex laminated stack
CB	Reset to Core Build	Makes a core build stack probably as a start point for a more complex laminated stack

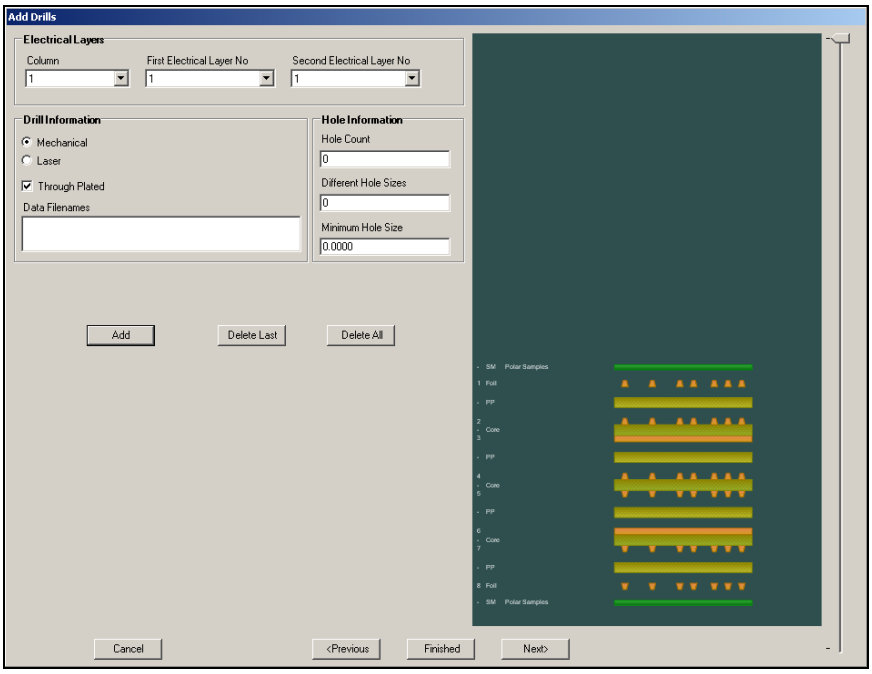
To produce non-standard sequences it is possible to start from any predefined sequence and by changing components, from combinations of foils and prepreg to cores and vice versa, any sequence can be defined (both practical and impractical.)

To select multiple components hold down the control key while left-clicking on materials.

Right click options

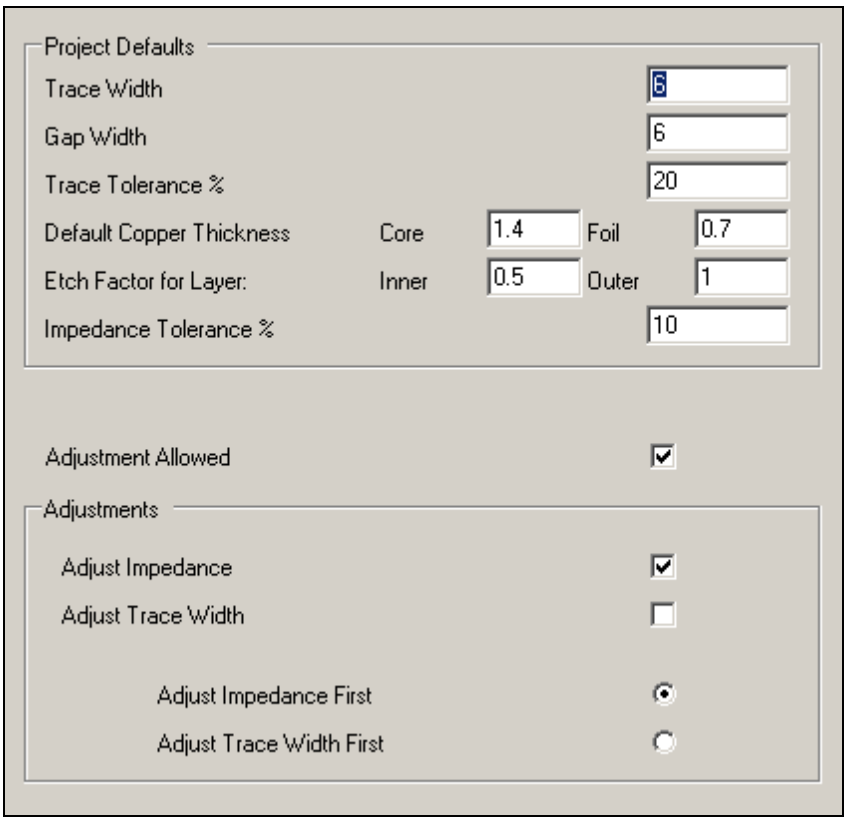
Right Click	Action
Single Foil	Mirror (invert) Foil
Single Prepreg	Nothing
Single Core	Convert to components, i.e. Cores and Prepreg
Two Cores with a prepreg sandwiched between	Convert to Core
N Materials	Copy block, this will copy a block of materials for pasting elsewhere in the stack. NB this will only copy the materials not copper layer types
Single Copper Material	Paste Block this will paste a block of materials in four different orientations

Adding drills



Drills are added in a similar manner to that below, see Core layer Information.

Project defaults



The Project Defaults screen allows the Tools/Options defaults to be overwritten *for the current project only*. It also allows for the setting of allowable adjustments to be made in the Automatic generation of stacks.

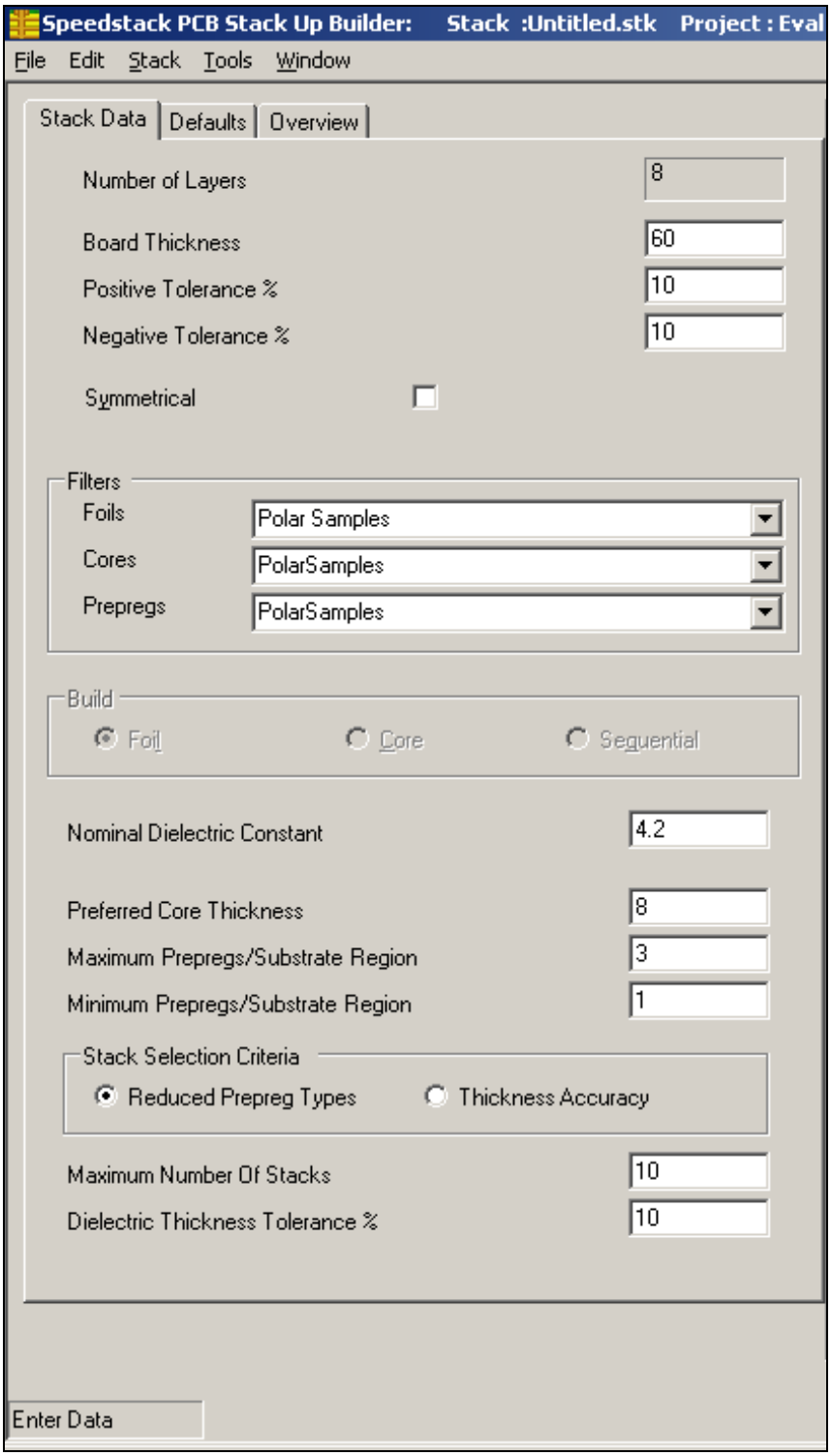
Allowing adjustments during goal seeking

When goal seeking takes place the initial goal seek is performed using the nominal values provided. Should that fail, the user may allow the target impedance and/or the nominal trace width to be varied in an attempt to find a solution.

The Adjustments Allowed check box enables the adjustments options: whether the target impedance and/or the trace width can be adjusted and, if both are allowed, which should be changed first.

When the Stack has been fully defined the screen returns to the Stack Definition Page.

Stack Definition page

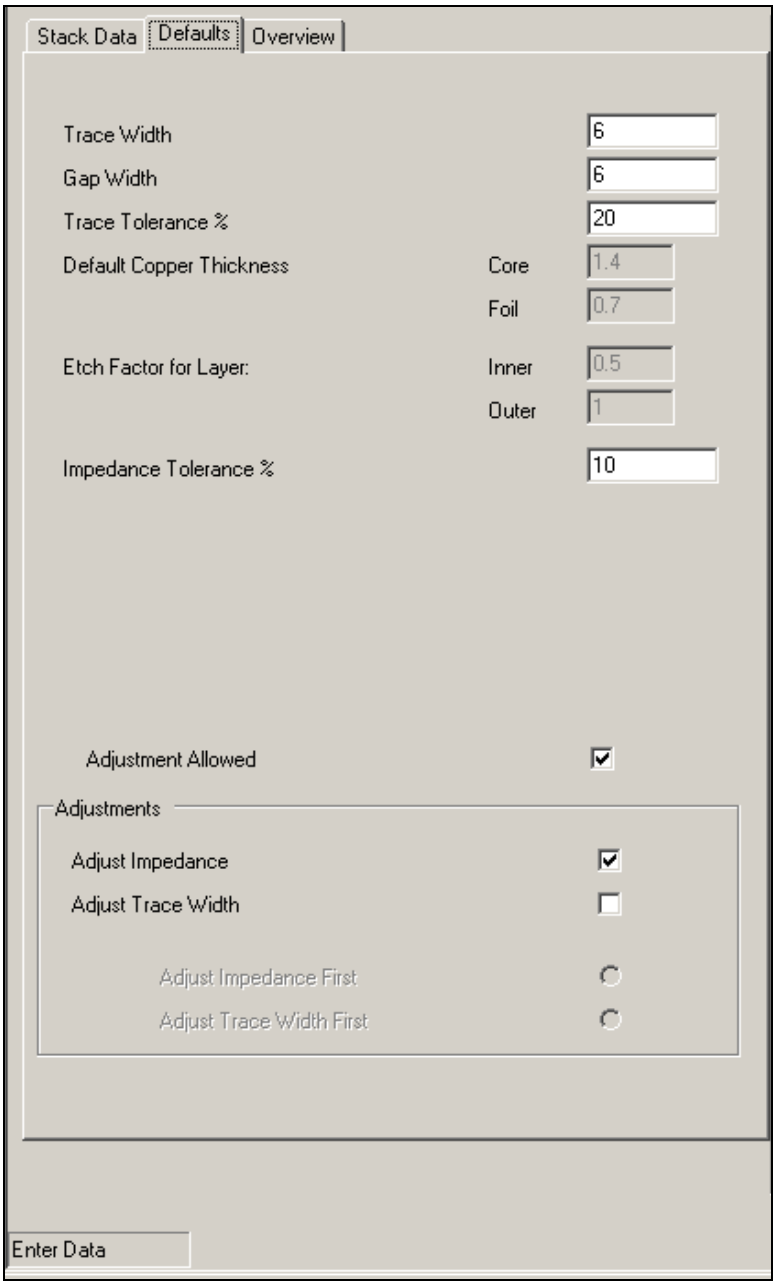


The left-hand side of the Stack Definition screen includes a series of tab-pages showing a summary of the data which has been selected. The screen also includes the means of selecting, via filters, the materials from the current library which are to be used. Many of the parameters provided in the definition stage can be amended.

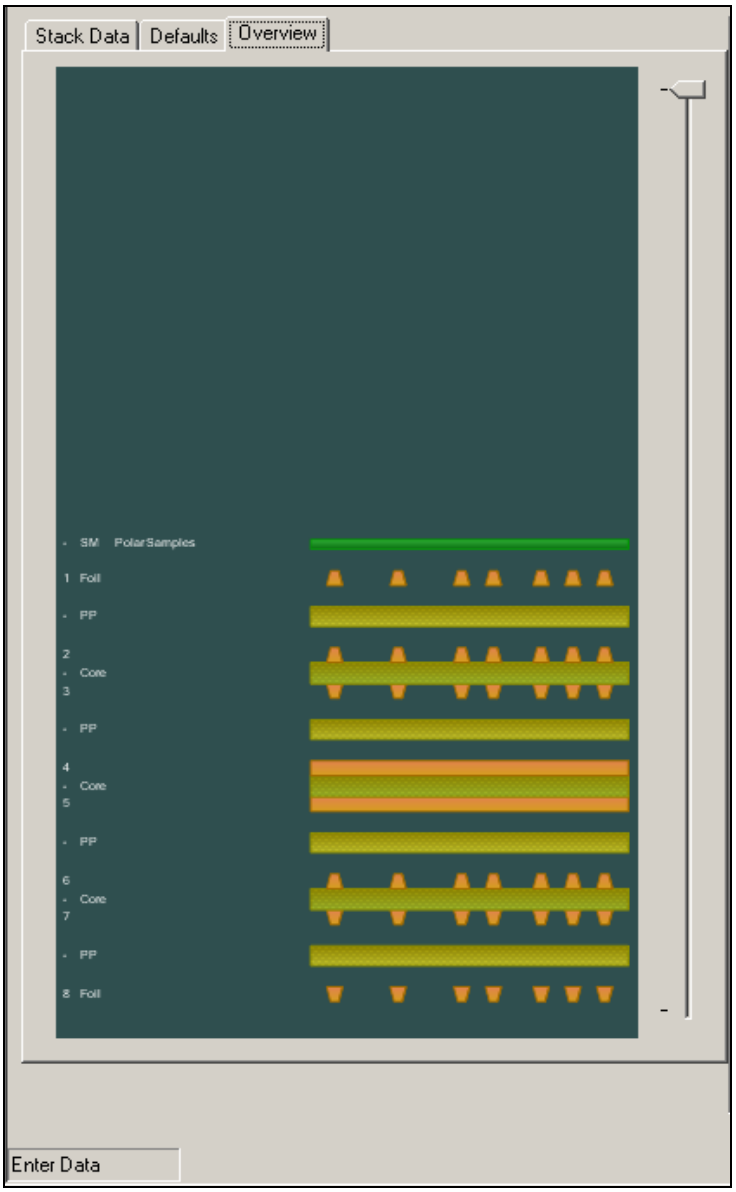
Filters

Where it is envisaged that a filter or set of filters will be used regularly then that/those filter(s) should be saved with the name “Default”. These will then be the default filters loaded on launch; they should be paired with the correct default library defined in the Tools/Options.

If a filter named “Default” is not available then the Filter with the name which occurs first in alphabetical order will be loaded on launch.



Stack Overview



Clicking on any material in the Overview screen will cause the stack representation to jump to that material, aiding the input of data on large layer count stacks.

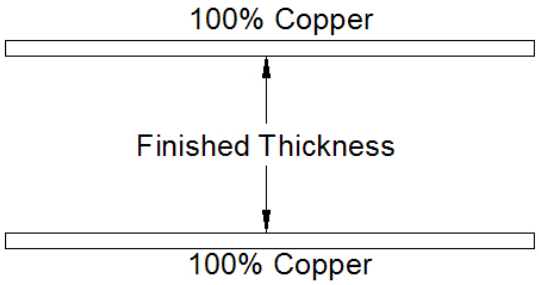
Speedstack will accommodate dielectric heights (H) calculated on the basis of *finished thickness* or *isolation distance*. H values are extracted from the stackup and used for calculating impedance (via the integrated Si8000 Controlled Impedance Quick Solver or Si9000 PCB Transmission Line Field Solver) in controlled impedance structures included in the stackup. H is the effective height of a dielectric substrate after the pressing of the stack.

The VSR engine will calculate for the minimum number of prepreg types (for ease of manufacture or minimum cost) or accuracy of board thickness at the user's option.

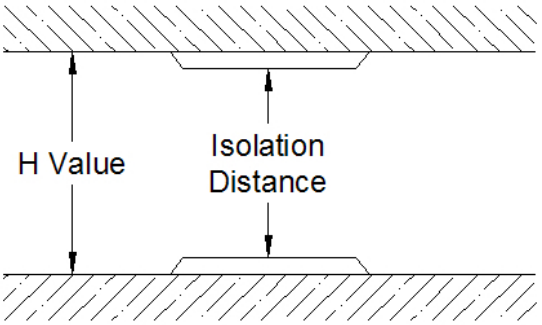
Specifying finished thickness

Finished thickness is the thickness of a prepreg after pressing between two solid sheets of copper, and should be defined in the materials library; it will be a lower value than the Base Thickness. Its value will be dependent upon the board shop's process parameters and is a critical dimension in many applications.

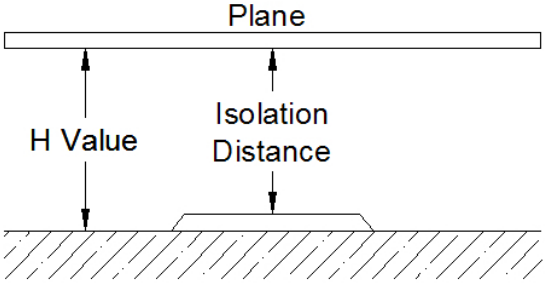
Speedstack keeps track of the finished thickness and tolerance, and allows fabricators to add in house post press thickness for prepreg layers, taking into account plating thickness where appropriate.



Copper may be embedded into the prepreg from either or both sides. Embedding copper in the prepreg reduces the thickness from the Finished Thickness. This reduced thickness is referred to as the Isolation Distance (see diagrams below).



Note: where more than one prepreg layer is involved the reduction is averaged across all the prepregs. A figure for Isolation Distance of less than zero implies an impossible build (i.e. the embedded copper totals more than the thickness of the prepreg).



The H Value is the sum of the isolation thickness and the full thickness of the adjacent copper(s). See Polar Instruments Application Note 507 for a discussion of calculating dielectric height with the Speedstack.

Adding controlled impedance structures

Apply the Stack Data and click on the Impedance buttons to add the controlled impedance structures for each layer, setting trace widths and H values if available. Up to ten structures may be specified for each layer; if the H values are unavailable then set for Autogenerate.

If a set of structures is required to be placed on more than one copper layer, define them on one layer, right click on that layer and select ‘Copy Structures’. Right click on the layer to receive these structures and select ‘Paste Structures’. Be aware that pasting structures will overwrite any existing structures on that layer, so define the common structures first then add any additional structures.

Critical structures

When defining structures for a layer a critical structure for that layer can be selected. This is the structure that will be the basis for all goal-seeking on that layer. The default critical structure is the one which has the widest trace width.

Validating structures

Click Validate Structures to validate each specified controlled impedance structure; valid structures may be unachievable with the current settings (H, trace widths, etc.); it may be necessary to return to the board designer to resolve. With all structures validated generate the stacks.

With all structures resolved the Speedstack will generate a series of stackups along with the associated costs.

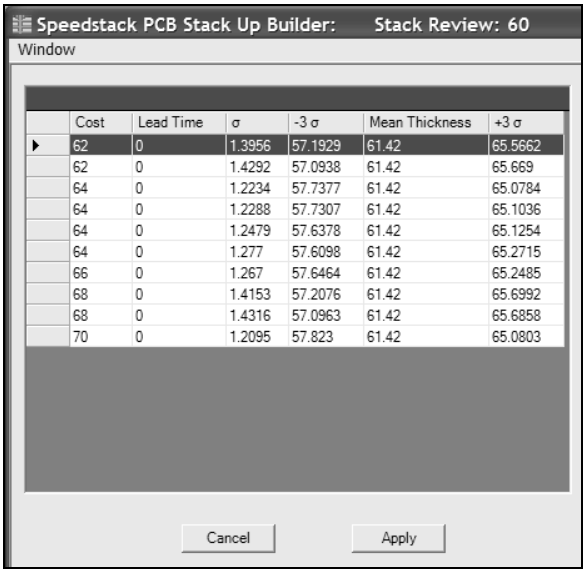
Reviewing the stack

Candidate stacks are displayed in the Stack Review screen (below). With the stacks generated, from the Stack Review screen specify the calculation method:

trim the trace widths to obtain the optimum impedance

calculate the impedances with the original trace widths

perform no impedance calculations.



The Stack Review screen

With the stacks displayed in the Stack Review screen, choose from the list of generated stacks and click Apply.

The completed stack will be transferred to the Speedstack Stackup Editor in asymmetrical mode.

Switch between the Speedstack screens, the Stack Definition screen, the Stack Review and the Stackup Editor screen using function keys, F10, F11 and F12.