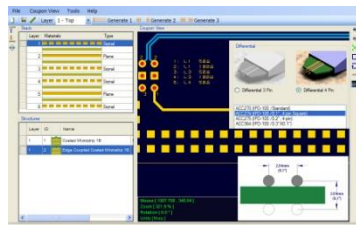
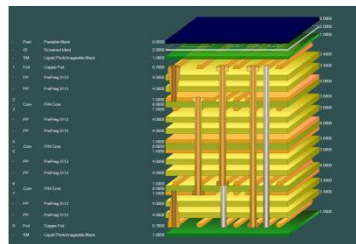
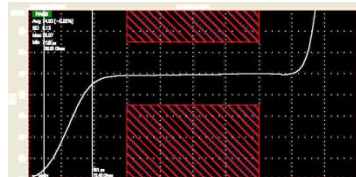
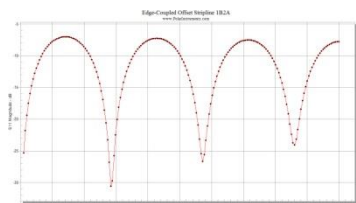
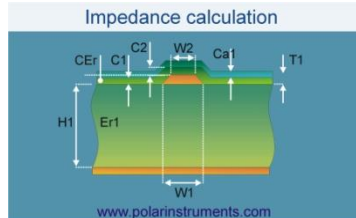




# Getting Started with Speedstack

Richard Attrill - August 2019



## Welcome to Speedstack

This Getting Started tutorial will familiarize you with the features and operation of Polar's Speedstack PCB Stack Up design system and guide you through the steps to create a Speedstack project (.sci) file.

If you would like a copy of the completed project file please request it from [polarcare@polarinstruments.com](mailto:polarcare@polarinstruments.com).

## Contents

- 4. Overview
- 7. Introducing the interface
- 10. Setting units and Virtual Material Mode
- 11. Using the Stack Up Wizard
- 14. Display modes
- 15. Editing the stack up
- 13. Drill information
- 27. Adding impedance structures
- 36. Frequency dependent loss calculations
- 41. Printing technical report
- 46. Summary – contact details

## Overview of Speedstack

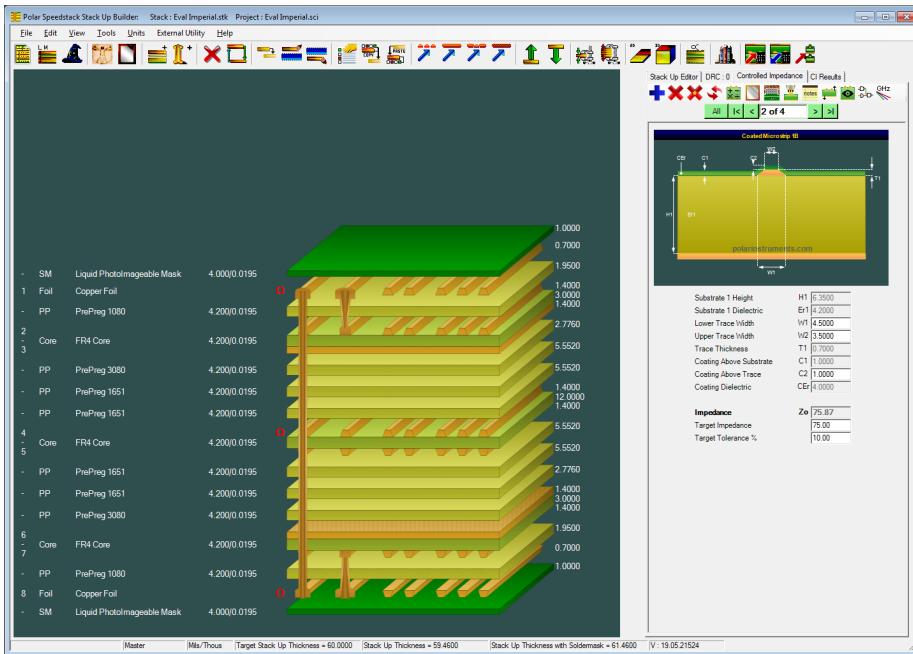
Speedstack is a comprehensive stack up design environment for pre-layout engineers, PCB fabricators and value-add PCB brokers. By collating libraries of materials, costs and suppliers with critical design data, such as transmission line specifications or impedance control, Speedstack lets you produce accurate build documentation.

Speedstack's end-to-end approach to stack up design allows you to create documents that can be shared at every stage of the PCB supply chain and drastically reduces the time you need to create, document and control PCB layer stack ups.

Speedstack links directly with the Si8000m Controlled Impedance and the Si9000e Insertion Loss field solvers

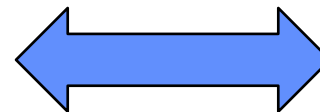
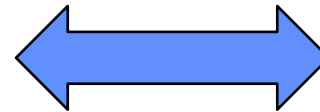
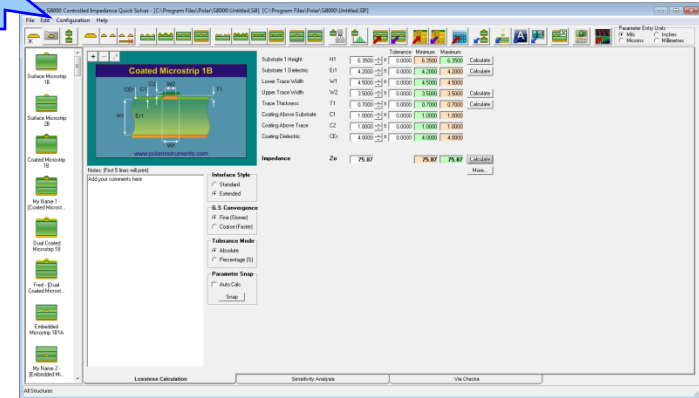
# Controlled Impedance and Insertion Loss Modelling

Speedstack

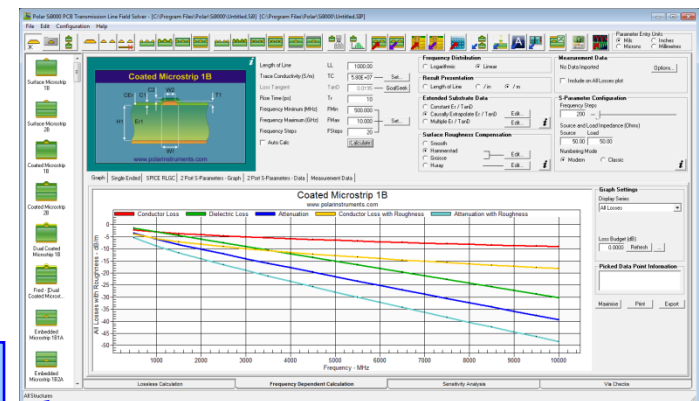


Si8000m  
(Speedstack PCB package)

Si8000m



Si9000e



Si9000e  
(Speedstack Si package)

## Speedstack – Methods of creating stack ups

Speedstack has two key methods to create stack ups:

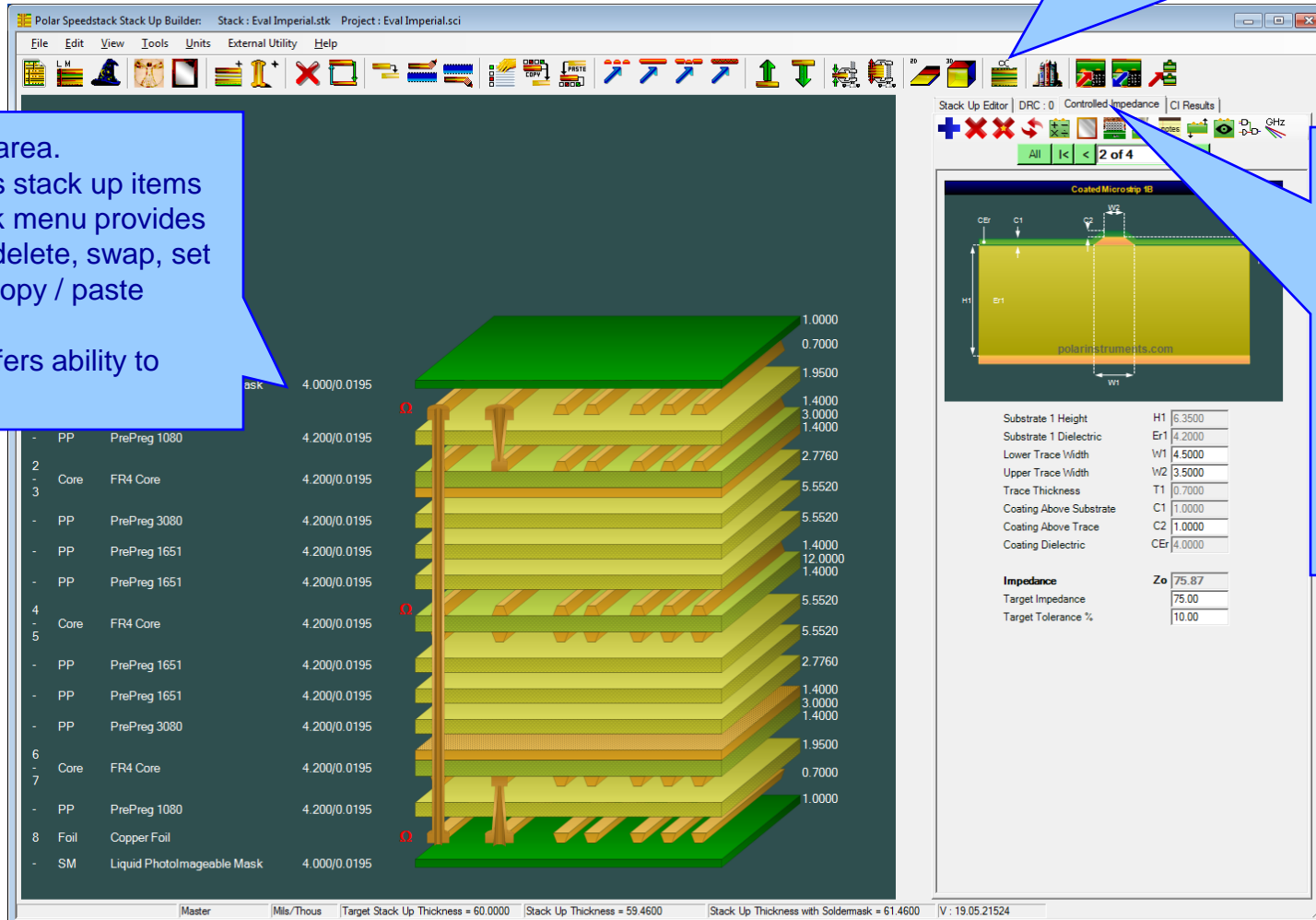
- Virtual Material Mode (VMM) – uses ‘virtual’ materials to generate stack ups. This is useful for exploring design options before committing to real materials.
- Material Library Mode – uses real materials to generate stack ups by referencing the Speedstack material library. This method provides an absolute definition of the stack up down to the exact materials used in the build.

The principle of building stack ups with Speedstack is the same regardless of the method used. The following slides will guide you through the process.

## Speedstack – Introducing the interface

Toolbar provides access to commonly used functions included add, delete and swap materials.

Stack up editor area.  
Left-click selects stack up items (blue), right-click menu provides options to add, delete, swap, set properties and copy / paste materials.  
Mouse wheel offers ability to zoom in / out



Tabs provide access to Stack Up, DRC and Controlled Impedance options.  
The Controlled Impedance tab allows structures to be added to the stack on a per layer basis. The browser buttons provide access to each structure

Stack up thickness can be monitored via the status bar



## Building a stack up from scratch

The following slides will guide you through the process of creating an 8 layer stack up. The stack has the following specification:

Units: Mils

Number of Layers: 8

Target Stack Up Thickness: 60 mils  $\pm$  10%

Signal Layers: 1, 3, 6, 8 Plane Layers: 2, 4, 5, 7. Symmetrical build

Material: Standard FR4, dielectric constant  $\sim$ 4.2, loss tangent  $\sim$ 0.02

Preferred Core Thickness: 8 mils

Copper Thickness: All layers 1oz copper, 1.4 mils



## Building a stack up from scratch (continued)

Solder Mask: Covering outer layers, 1 mil

PTH drill passes: layers 1 – 8

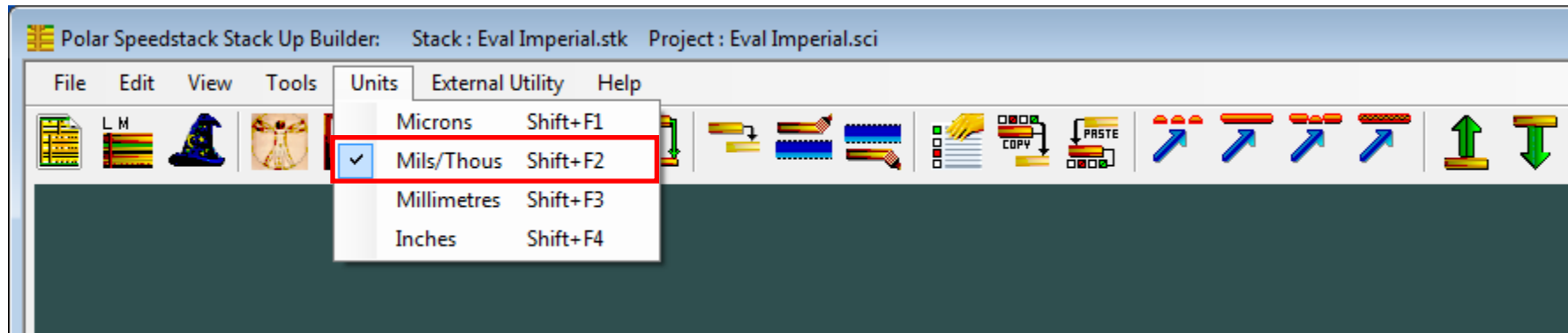
Laser microvia passes: layers 1 – 2, 8 – 7

Singled-ended impedance: 50 ohms  $\pm$  10% on layers 1, 3, 6, 8

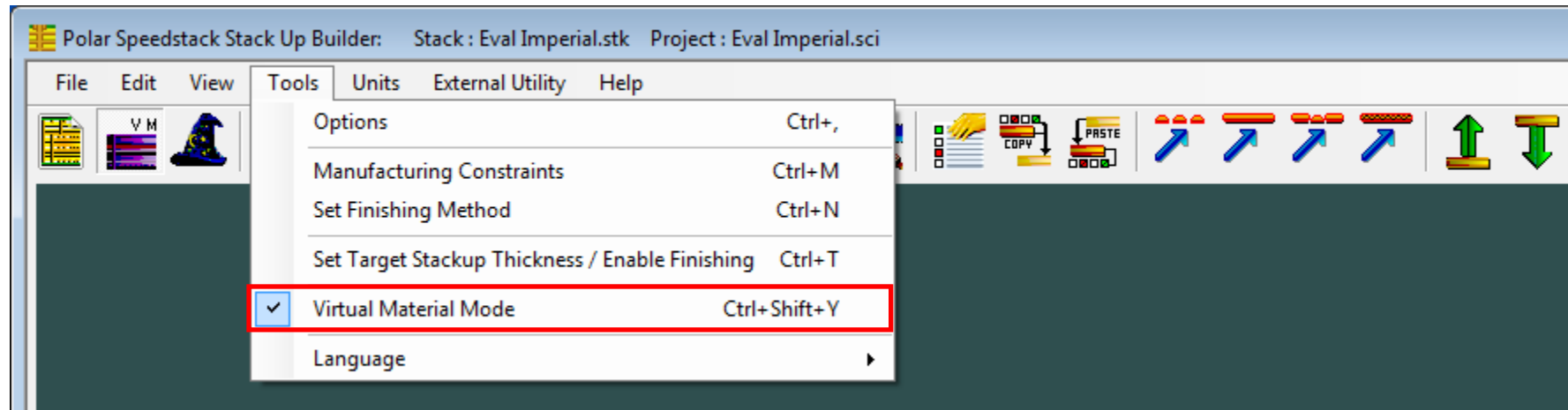
Differential impedance: 100 ohms  $\pm$  10% on layers 1, 3, 6, 8

## Step 1: Setting the Units and Virtual Material Mode

From the Units menu select the 'Mils/Thou' option



From the Tools menu select the 'Virtual Material Mode' option



## Step 2: Using the Stack Up Wizard to rapidly build the stack up

Select the Stack Up Wizard toolbar icon 

Stack Up Wizard (Virtual Material Mode)

Number of Layers	8	Nominal Dielectric Constant	4.2000
Target Stack Up Thickness	60.0000	Nominal Loss Tangent	0.0200
Positive Tolerance %	10	Solder Mask Top <input checked="" type="checkbox"/>	Solder Mask Bottom <input checked="" type="checkbox"/>
Negative Tolerance %	10	Solder Mask Dielectric Constant	4.0000
Symmetrical <input checked="" type="checkbox"/>		Solder Mask Loss Tangent	0.0200
Plane Layers	Mixed Layers	Solder Mask Thickness	1.0000
1	1	Preferred Core Thickness	Select 8.0000
2	2	Copper Thickness	1.4000
3	3		
4	4		
5	5		
6	6		
7	7		
8	8		

Build Type

Foil  Core  Sequential/HDI

<Previous Next > Finish Cancel

- Enter the Basic Stack Data as previously described in the stack up specification
- The Number of Layers dropdown will populate the Plane Layers and Mixed Layers lists
- The Symmetrical checkbox setting will control how the Plane Layers are selected
- Once the fields are populated select the Finish button

## Step 2: Using the Stack Up Wizard (continued)

An option to enter the Stack Up Properties can be skipped

The stack up created by the Wizard will now be displayed

**Configuring the display.**  
 The fields displayed next to the stack can be configured using the Tools | Options | General tab. In this case:  
 Field 3 = Description  
 Field 4 = Dielectric Constant / Loss Tangent  
 Field 5 = Processed Thickness

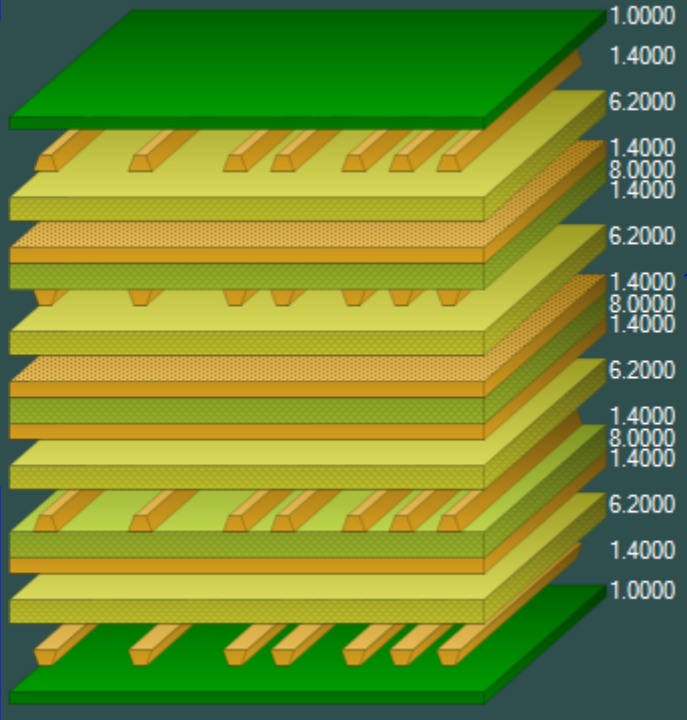
Dielectric Constant / Loss Tangent

Processed Thickness:  
 Copper Finished Thickness  
 Dielectric Isolation Distance  
 Stack Up Thickness =  
 Copper Finished Thickness +  
 Dielectric Isolation Distance

Electrical Layer Number

Material type:  
 SM: Solder Mask  
 Foil: Copper Foil  
 PP: Prepreg (dielectric)  
 Core: Copper clad dielectric

Electrical Layer Number	Description	Dielectric Constant / Loss Tangent	Processed Thickness
1	SM		1.0000
2	Foil		1.4000
3	PP	4.200/0.0200	8.0000
4	Core	4.200/0.0200	6.2000
5	PP	4.200/0.0200	1.4000
6	Foil		1.4000
7	PP	4.200/0.0200	8.0000
8	Core	4.200/0.0200	6.2000
9	PP	4.200/0.0200	1.4000
10	Foil		1.4000
11	SM		1.0000



## Step 3: Saving the Speedstack project

Now that a stack has been created we can save it

Use the File | Save Project As menu option and specify a filename

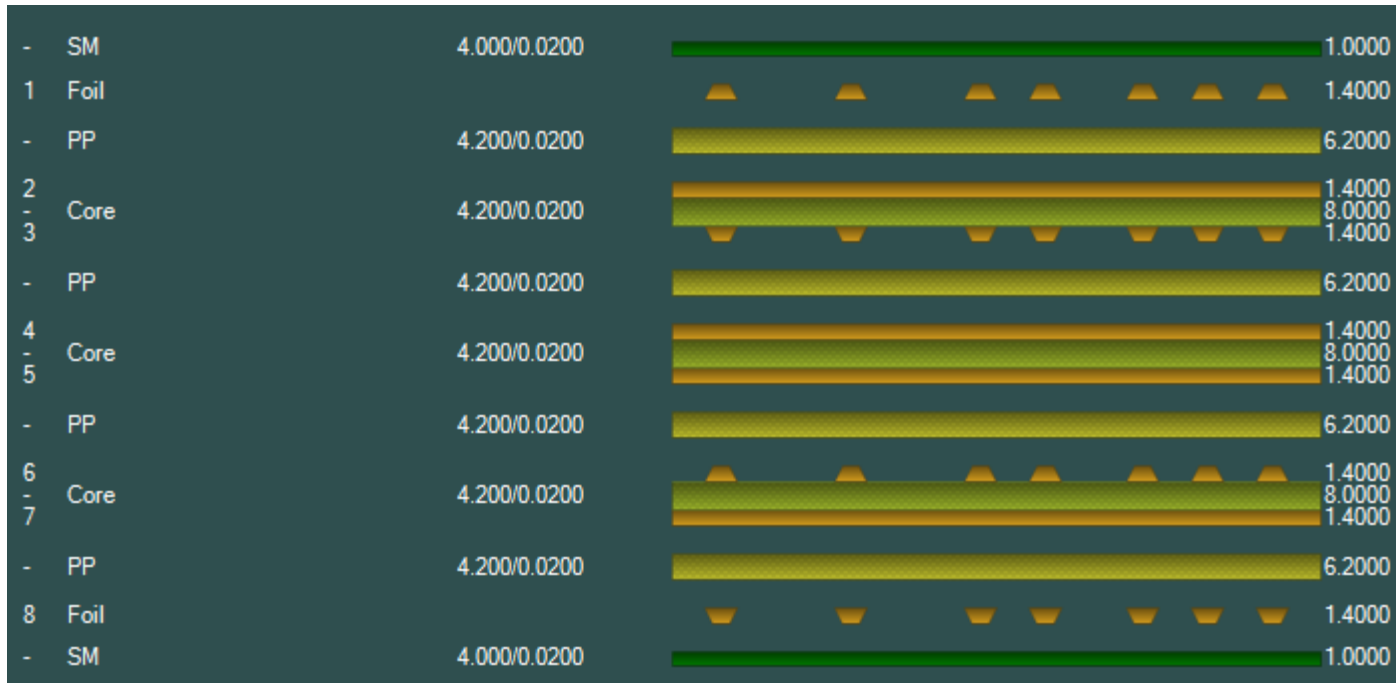
The filename will have a .SCI extension, recognisable by this icon 

## Step 4: Switching between 3D and 2D display modes

It is sometimes easier to view stack up in 2D by selecting



This will result in the following stack up display



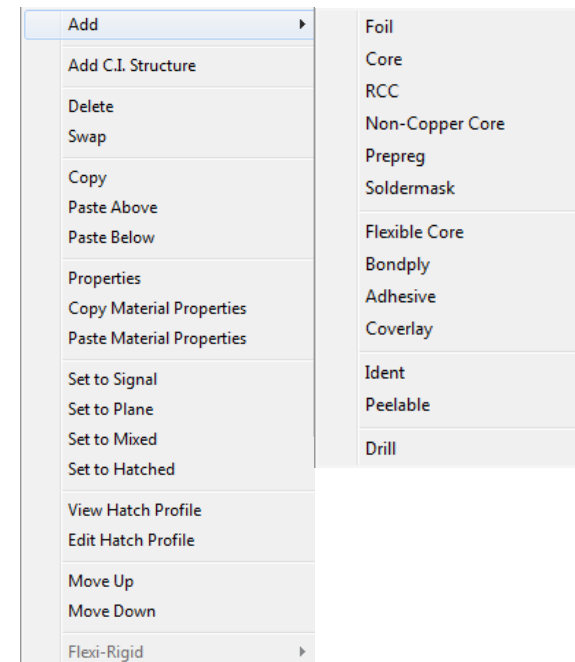
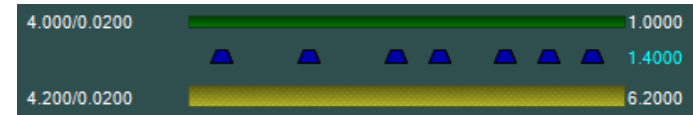
The 3D display mode can be activated by selecting



## Step 4: Editing the stack up

Once the stack up has been created using the Wizard it is possible to make changes on a per material basis using the various editing functions

- Click on the material that you wish to edit
- Selected material will highlight in blue
- Use the right-click menu and select option or use toolbar icons





## Step 4: Editing the stack up (continued)

Add: Adds the chosen material above or below the selected item 

Delete: Removes the selected material 

Swap: Swaps material with another of the same type 

Copy: Copies the selected material to clipboard 

Paste Above: Pastes the copied material above selected item 

Paste Below: Pastes the copied material below selected item 

Move Up: Move the selected material up one position 

Move Down: Move the selected material down one position 

Properties: Change the properties of the selected material 

## Step 4: Editing the stack up – electrical layers only

Signal: Set electrical layer to signal



Plane: Set electrical layer to plane



Mixed: Set electrical layer to mixed




Hatched: Set electrical layer to hatched (separately licensed)



Setting the electrical layer types on the stack up will allow Speedstack to guide you through the process of adding controlled impedance structures. It will suggest the appropriate structure based on the signal layer and plane layer positions within the stack. More details will be shown in Step 6.

## Step 4: Editing the stack up – symmetrical mode

Many stack ups are symmetrical, so viewing from the centre the upper and lower sections of the stack up have exactly the same materials

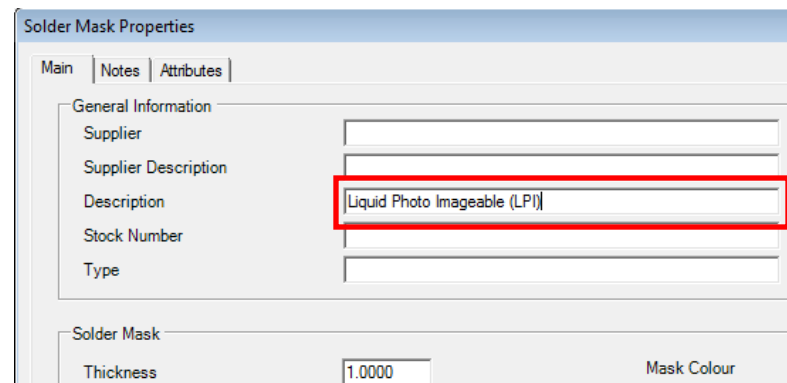
Speedstack allows you to work in symmetrical mode by selecting  This is a toggle function, selecting this option again disables this mode

When this mode is enabled the editing functions will process both the upper and lower materials of the stack simultaneously, saving significant time.

## Step 4: Editing the stack up – change material properties

All the information about each material is stored in the material properties. To change properties of the stack created by the Wizard

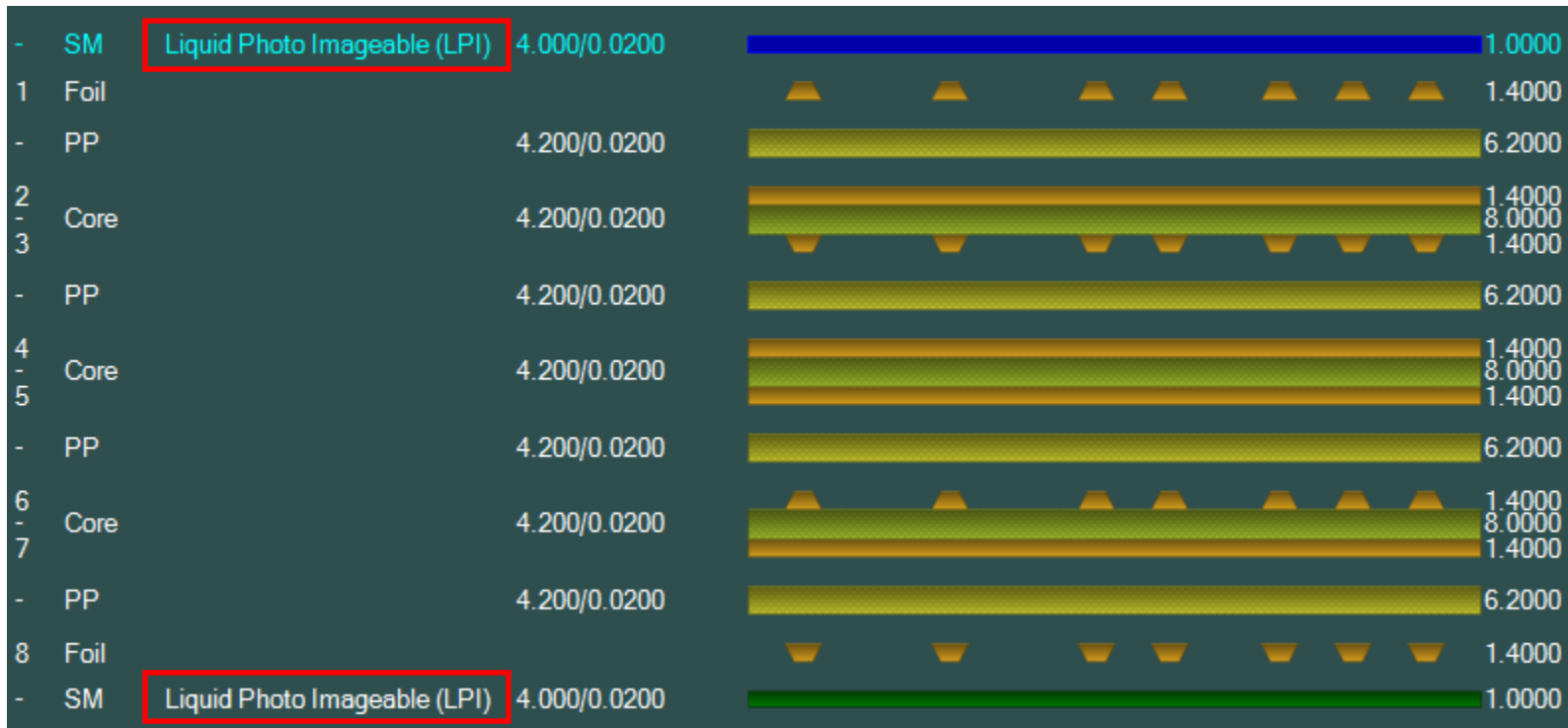
- Enable symmetrical mode
- Select the top solder mask layer
- Select Properties
- Enter text in the Description field
- Select Apply to store information



Solder Mask Properties	
Main   Notes   Attributes	
General Information	
Supplier	
Supplier Description	
Description	Liquid Photo Imageable (LPI)
Stock Number	
Type	
Solder Mask	
Thickness	1.0000
	Mask Colour

## Step 4: Editing the stack up – change material properties (cont'd)

The stack up will now display the solder mask description text



## Step 4: Editing the stack up – change material properties (cont'd)

Repeat the process to set properties for the other materials

- Foil properties

Description	Copper Foil 1oz
-------------	-----------------

- Prepreg properties

Description	Prepreg Region
-------------	----------------

- Core properties

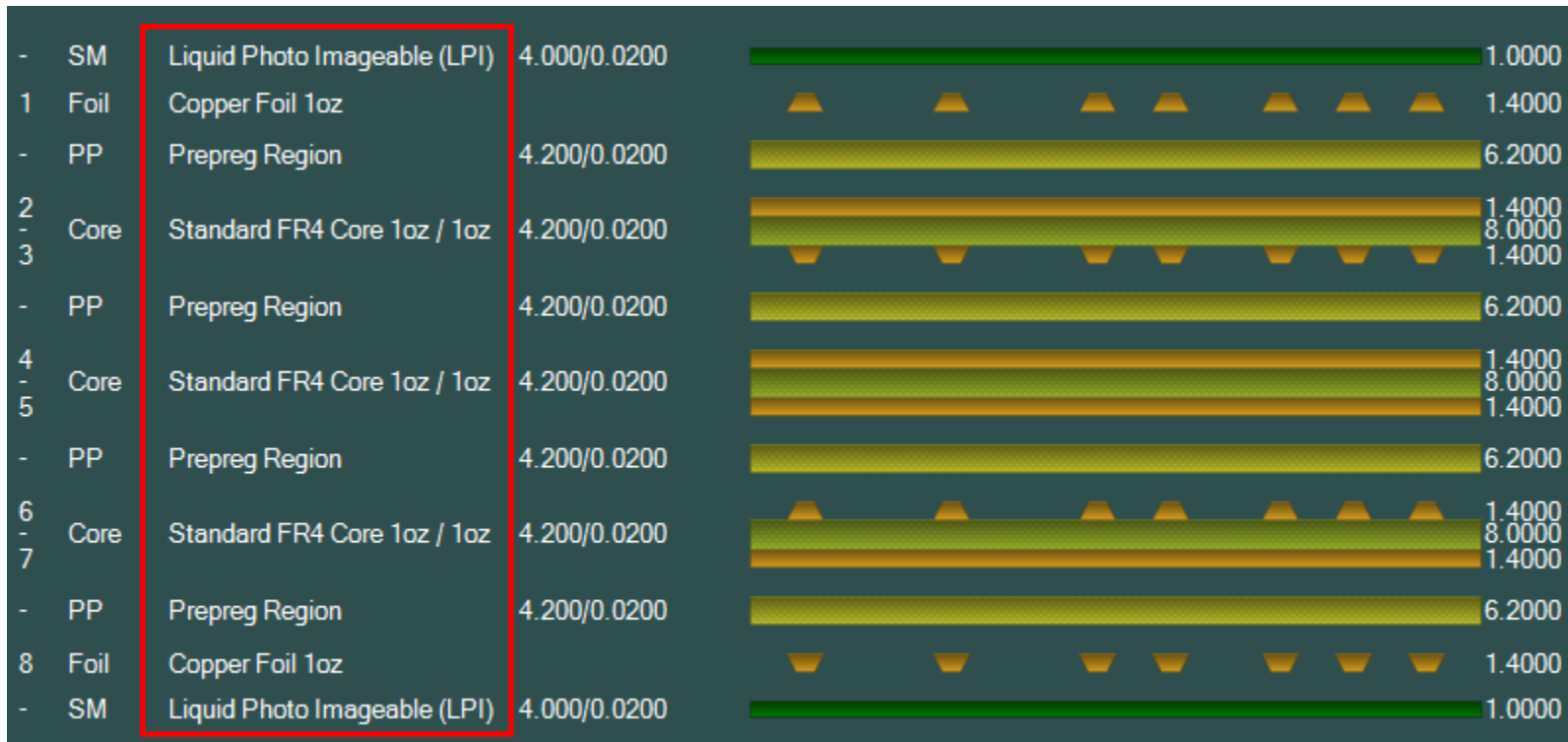
Description	Standard FR4 Core 1oz / 1oz
-------------	-----------------------------

- When complete  
disable symmetrical  
mode



## Step 4: Editing the stack up – change material properties (cont'd)

The stack up will now display description properties for all materials

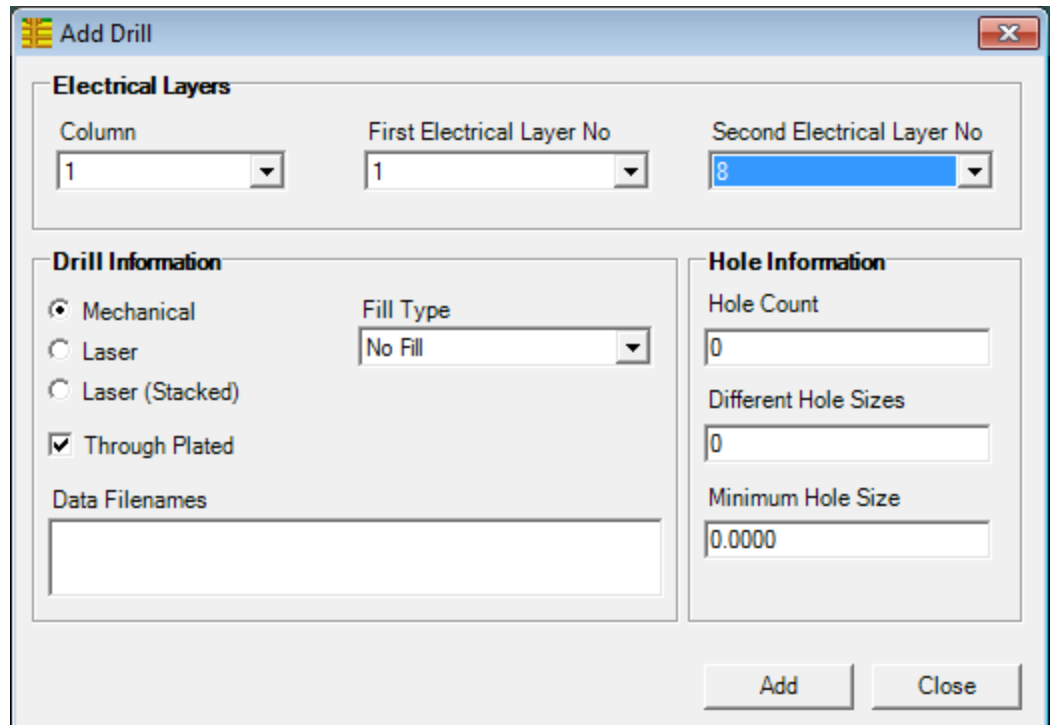




## Step 5: Adding drilling information

Select the Add Drill toolbar icon 

- Select the Column where the drill will be added to the stack. 1 is the left-most column.
- Set the First and Second Electrical Layer Numbers, in this case a PTH drill will start on layer 1 (top) and end on layer 8 (bottom)
- Select Add to add the drill



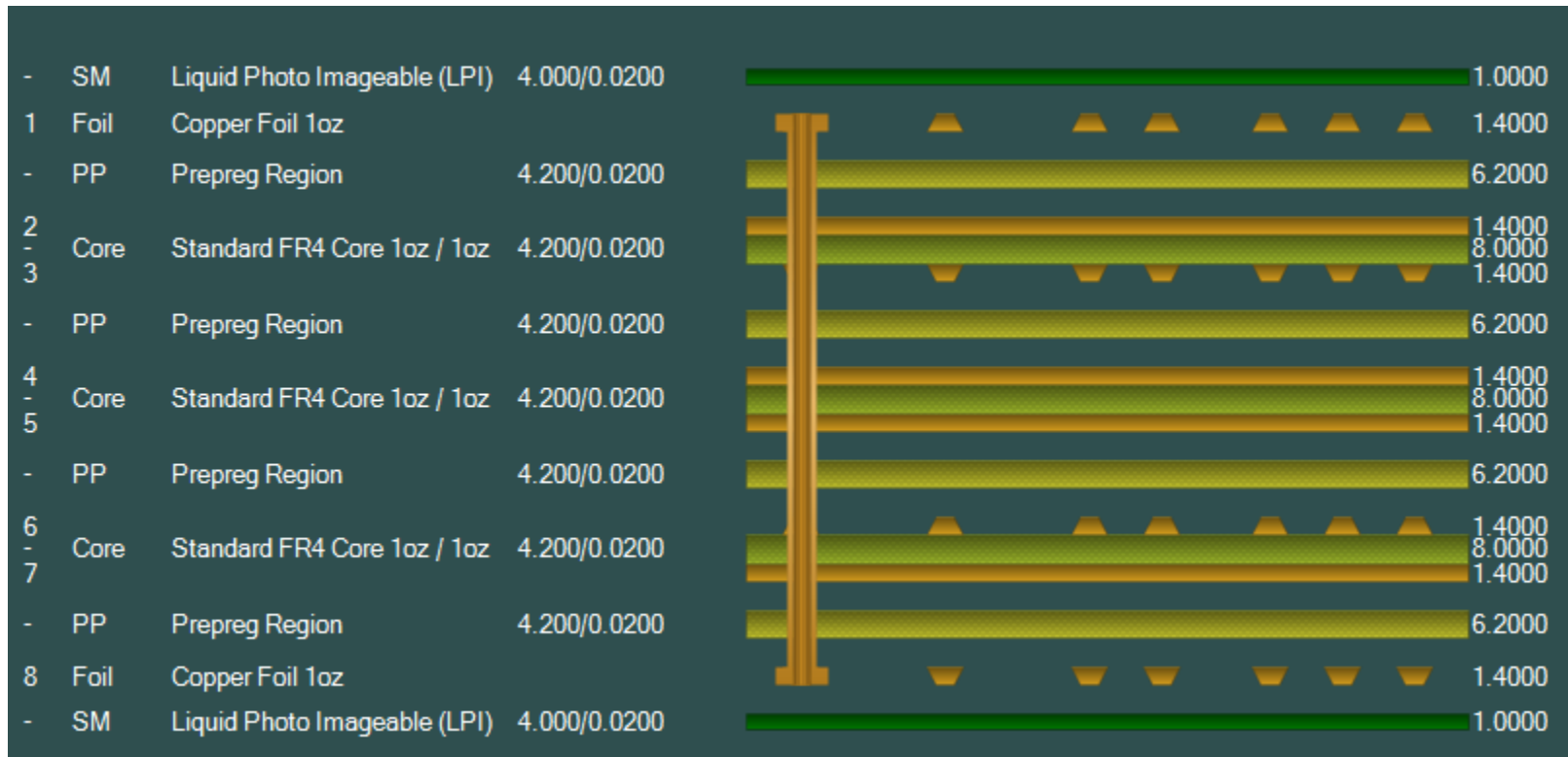
The screenshot shows the 'Add Drill' dialog box with the following settings:

- Electrical Layers:**
  - Column: 1
  - First Electrical Layer No: 1
  - Second Electrical Layer No: 8
- Drill Information:**
  - Mechanical
  - Laser
  - Laser (Stacked)
  - Through Plated
  - Fill Type: No Fill
  - Data Filenames: (empty text box)
- Hole Information:**
  - Hole Count: 0
  - Different Hole Sizes: 0
  - Minimum Hole Size: 0.0000

Buttons: Add, Close

## Step 5: Adding drilling information (continued)

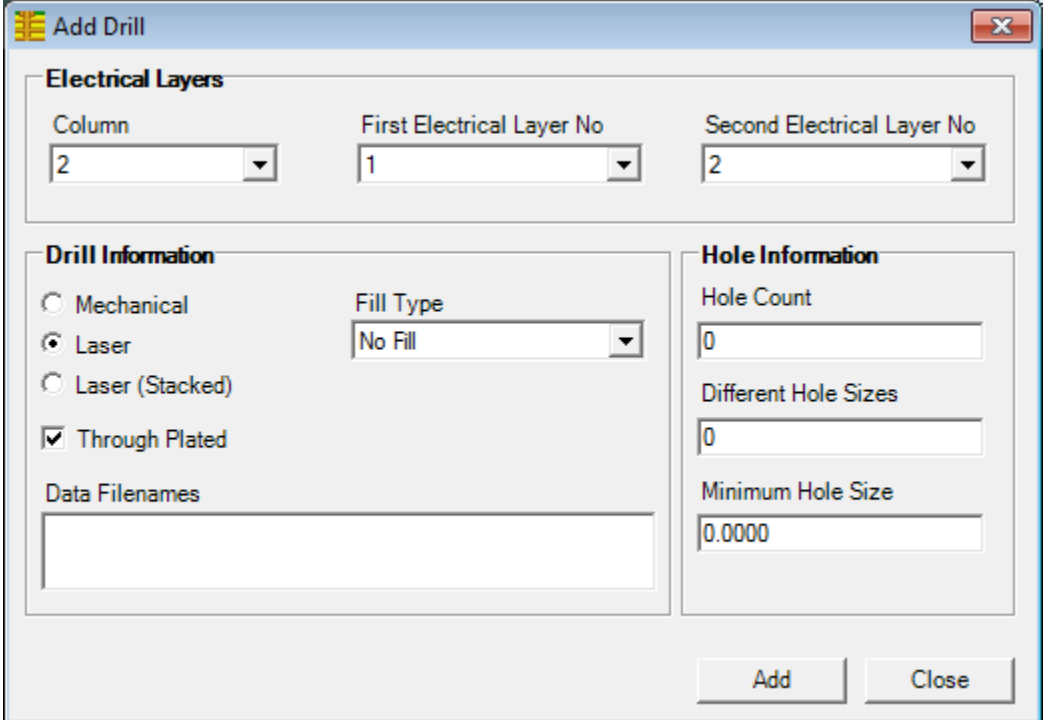
The stack up will now display the Plated Through Hole (PTH) drill



## Step 5: Adding drilling information (continued)

Now we will add the laser microvias. Select the Add Drill toolbar 

- Select Column = 2
- Set the First and Second Electrical Layer Numbers, in this case the drill will start on layer 1 and end on layer 2
- Select Laser
- Select Add to add the drill
- Repeat the process, Column = 2, First = 8, Second = 7, select Laser
- Select Add to add the drill



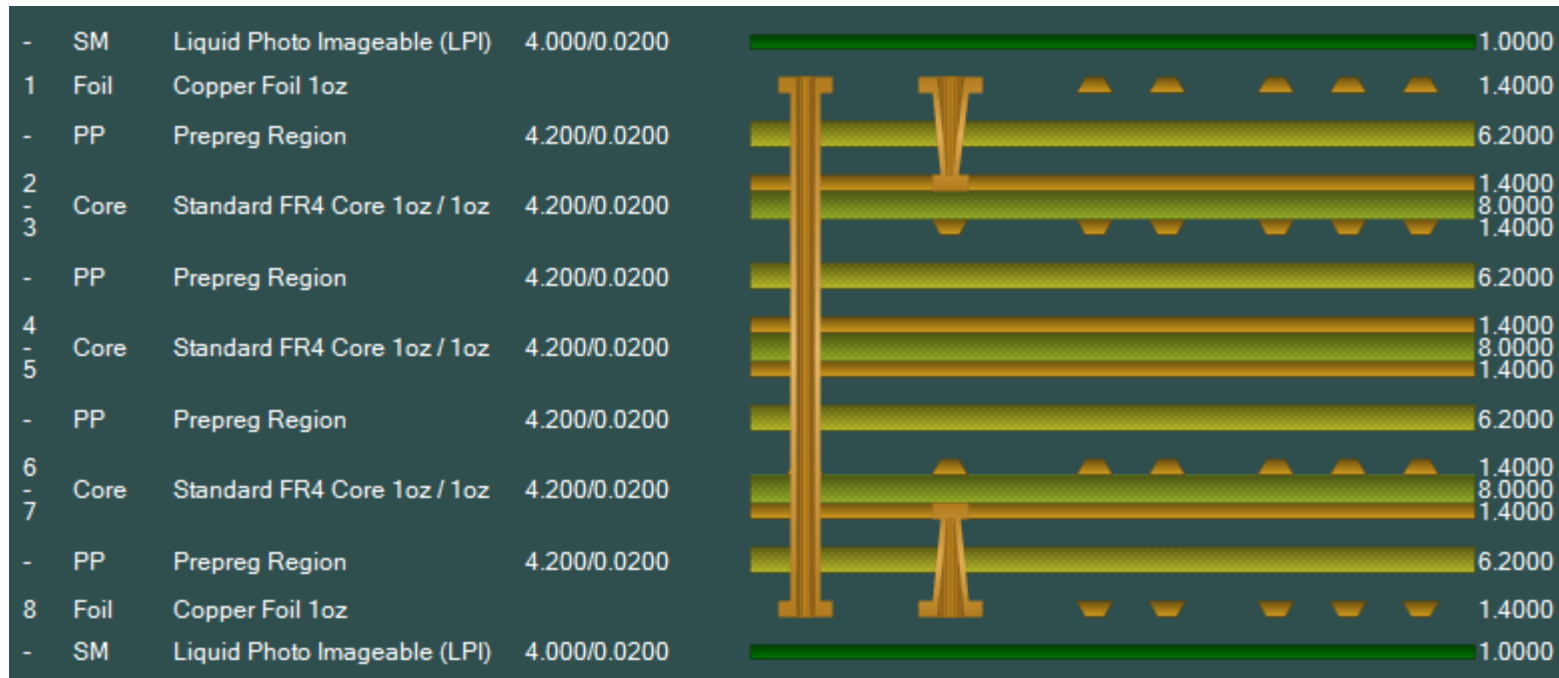
The screenshot shows the 'Add Drill' dialog box with the following settings:

- Electrical Layers:**
  - Column: 2
  - First Electrical Layer No: 1
  - Second Electrical Layer No: 2
- Drill Information:**
  - Mechanical
  - Laser
  - Laser (Stacked)
  - Through Plated
  - Fill Type: No Fill
  - Data Filenames: (empty text box)
- Hole Information:**
  - Hole Count: 0
  - Different Hole Sizes: 0
  - Minimum Hole Size: 0.0000

Buttons: Add, Close


## Step 5: Adding drilling information (continued)

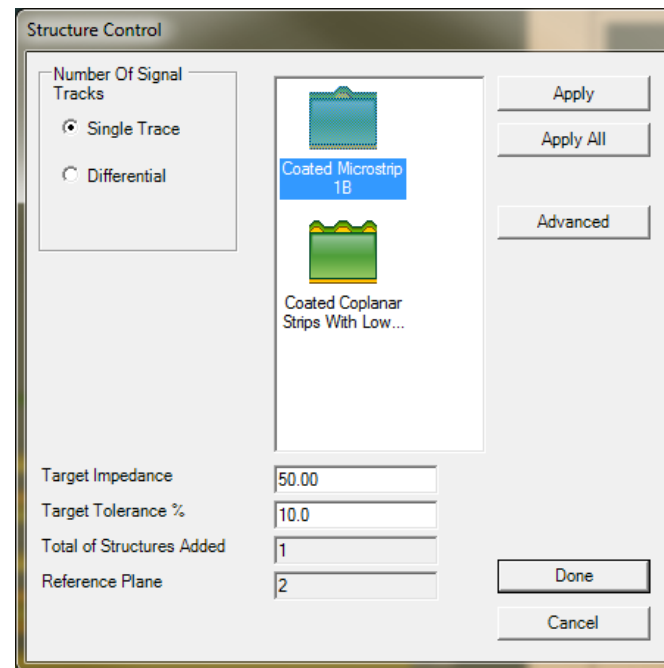
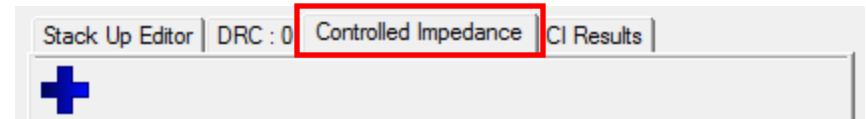
At this stage the stack up will display all the required drilling information



This is an appropriate stage to save the stack up project as described in Step 3.

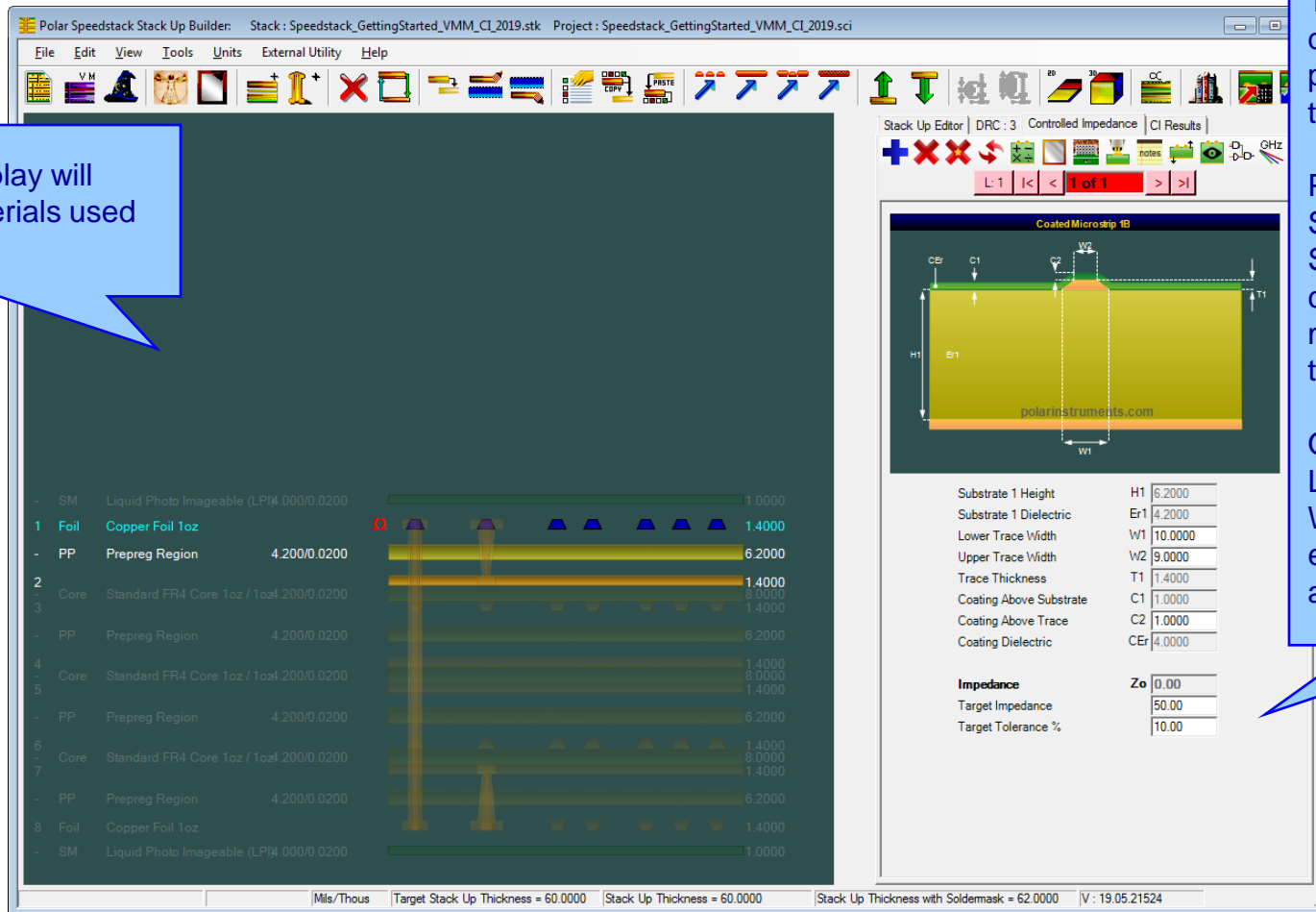
## Step 6: Adding impedance structures

- Select the Controlled Impedance tab
- Click on the signal layer of the stack where the structure is to reside, in this case layer 1
- Select  to add a structure, the Structure Control dialog will be displayed. Only structures appropriate to layer 1 will be offered.
- Enter Target Impedance and Tolerance as shown, select 'Coated Microstrip 1B' icon, Apply and then Done to dismiss dialog



## Step 6: Adding impedance structures (continued)

The new structure will appear on the controlled impedance tab





The stack up display will highlight the materials used by the structure

The structure image is displayed together with the parameters that are required to calculate the impedance.

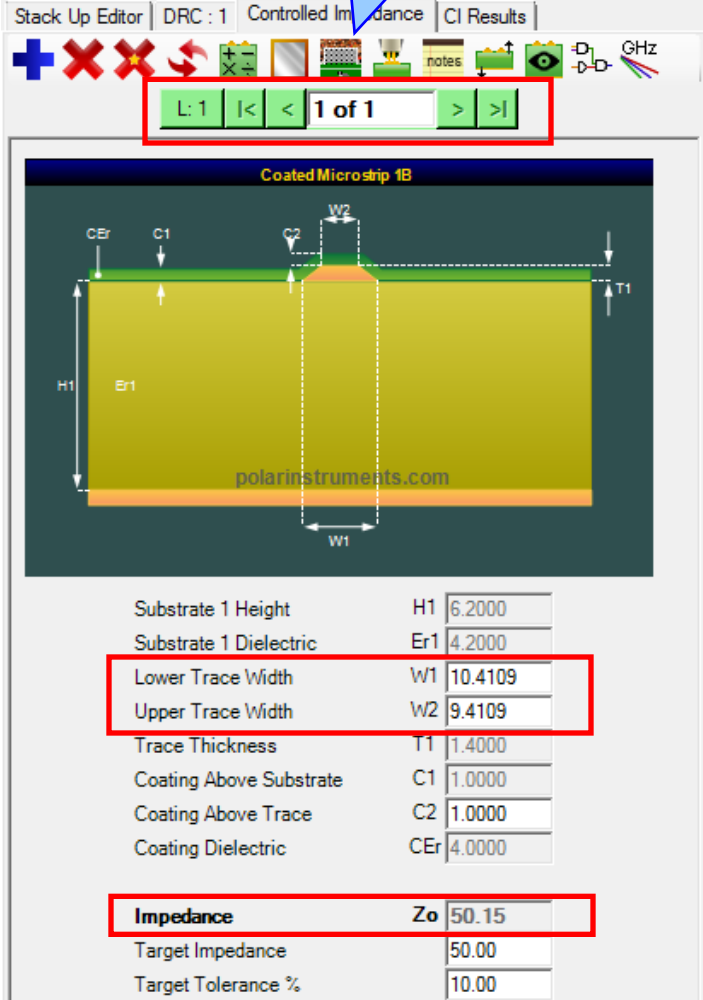
Parameters such as Substrate Height (H1) and Substrate Dielectric (Er1) are calculated from the stack up materials used. Therefore, they are read-only.

Other parameters such as Lower and Upper Trace Widths (W1 / W2) may be entered by the user, these are read/write fields.

## Step 6: Adding impedance structures (continued)

- Key in the desired trace widths
- Click on the  to Rebuild and Calculate the impedance structures
- Notice that the Impedance ( $Z_0$ ) result updates
- Use the  option to Goal Seek parameter(s) in order that the Target Impedance is met. Select 'W1 / W2 only' and watch Speedstack adjust these parameters to achieve the 50 ohms Target Impedance
- Notice that the trace widths (W1/W2) and the impedance results ( $Z_0$ ) updates
- Green indicator denotes within tolerance

Goal Seek option



Stack Up Editor | DRC : 1 | Controlled Impedance | CI Results

L: 1 | < | < | 1 of 1 | > | >

Coated Microstrip 1B

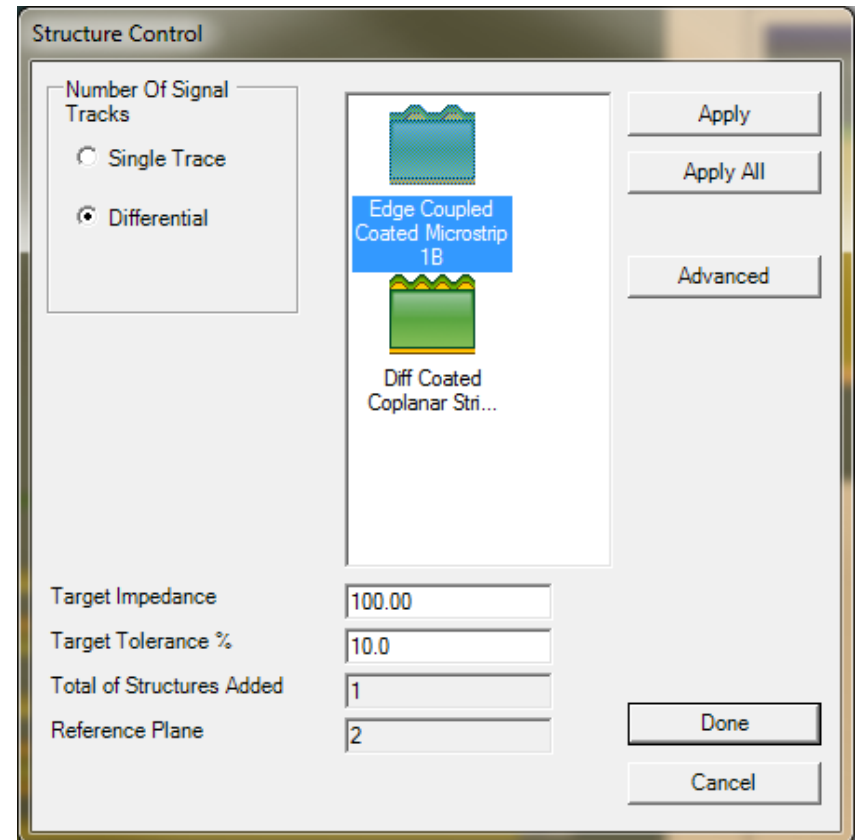
Diagram labels: CEr, C1, C2, W2, T1, H1, Er1, W1

Substrate 1 Height	H1	6.2000
Substrate 1 Dielectric	Er1	4.2000
Lower Trace Width	W1	10.4109
Upper Trace Width	W2	9.4109
Trace Thickness	T1	1.4000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Dielectric	CEr	4.0000
<b>Impedance</b>	<b>Zo</b>	<b>50.15</b>
Target Impedance		50.00
Target Tolerance %		10.00




## Step 6: Adding impedance structures - differential

- Click on layer 1 of stack
- Select **+** to add a structure, select Differential, enter Target Impedance and Tolerance as shown, choose 'Edge Coupled Coated Microstrip 1B', Apply and then Done to dismiss dialog
- The differential structure will be added to the stack. Notice that this is structure 2 of 2.

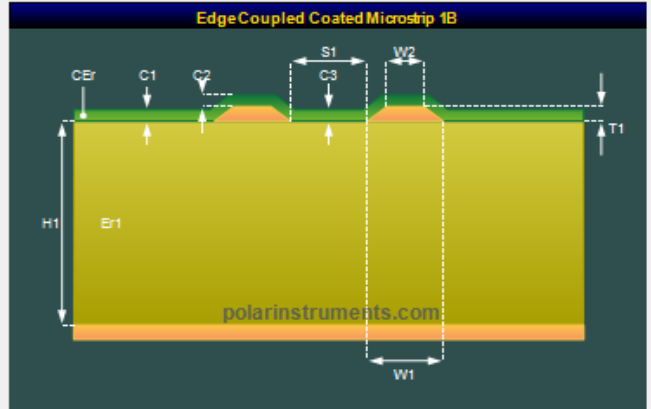


## Step 6: Adding impedance structures - differential

- Key in the desired trace widths / separation
- Use the  option to Goal Seek parameter(s) in order that the Target Impedance is met. Select 'W1 / W2 constant pitch' and watch Speedstack adjust these parameters to achieve the 100 ohms Target Impedance
- Notice that the trace widths and separation (W1 / W2 / S1) and the impedance results (Zd) updates
- Green indicator denotes within tolerance

Stack Up Editor | DRC : 1 | Controlled Impedance | CI Results

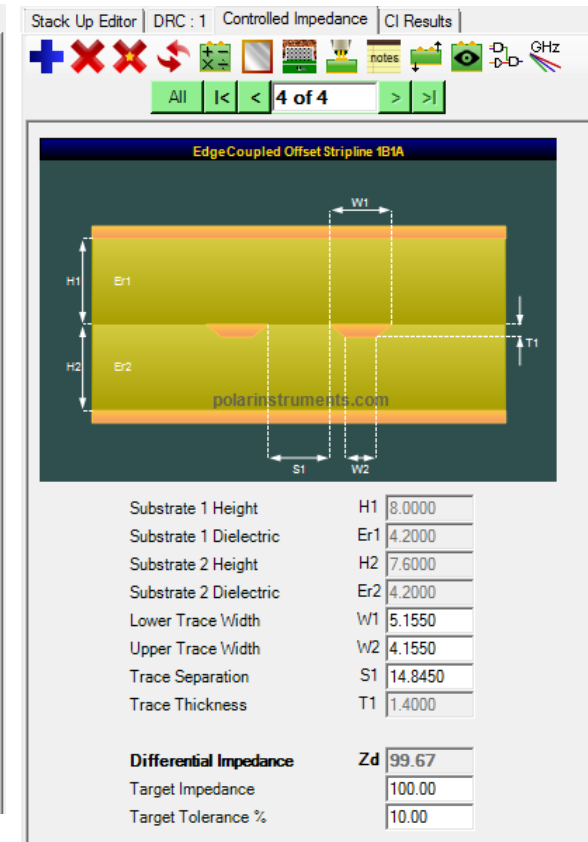
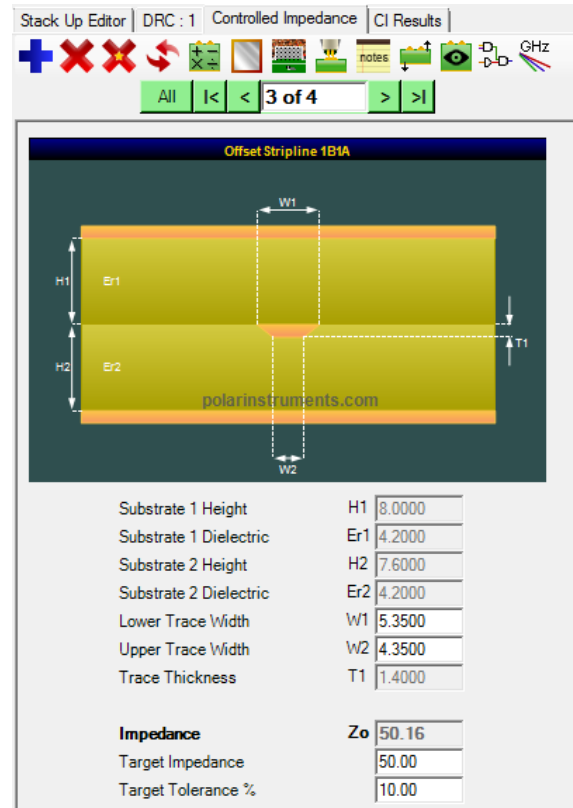
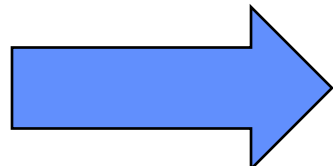
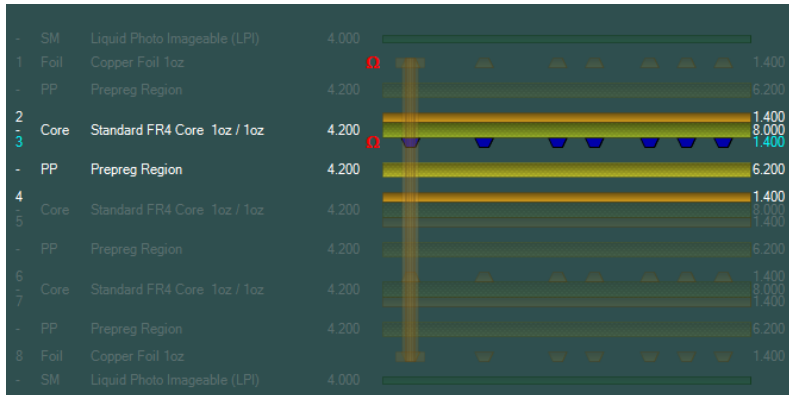
L: 1 | K | < 2 of 2 > | > | > |



Substrate 1 Height	H1	6.2000
Substrate 1 Dielectric	Er1	4.2000
Lower Trace Width	W1	8.5685
Upper Trace Width	W2	7.5685
Trace Separation	S1	11.4315
Trace Thickness	T1	1.4000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Between Traces	C3	1.0000
Coating Dielectric	CER	4.0000
<b>Differential Impedance</b>	<b>Zd</b>	<b>100.04</b>
Target Impedance		100.00
Target Tolerance %		10.00

## Step 6: Adding impedance structures – layer 3

Follow the same process to add single-ended 50 ohms and differential 100 ohms structures to layer 3.



## Step 6: Adding impedance structures

At this point we have four structures, two on layer 1, two on layer 3

The screenshot shows the Polar Speedstack Stack Up Builder interface. The main window displays a stack up configuration with various layers and materials. A callout box points to the structure browse control, which shows four structures. Another callout box points to the Omega ( $\Omega$ ) symbol placed next to layers that contain structures.

**Structure Browse Control:**

The structure browse control shows four structures. The current structure is "Edge Coupled Offset Stripline IBIA".

**Structure Parameters:**

Substrate 1 Height	H1	8.0000
Substrate 1 Dielectric	Er1	4.2000
Substrate 2 Height	H2	7.6000
Substrate 2 Dielectric	Er2	4.2000
Lower Trace Width	W1	5.1550
Upper Trace Width	W2	4.1550
Trace Separation	S1	14.8450
Trace Thickness	T1	1.4000
<b>Differential Impedance</b>	<b>Zd</b>	<b>99.67</b>
Target Impedance		100.00
Target Tolerance %		10.00

**Stack Up Configuration:**

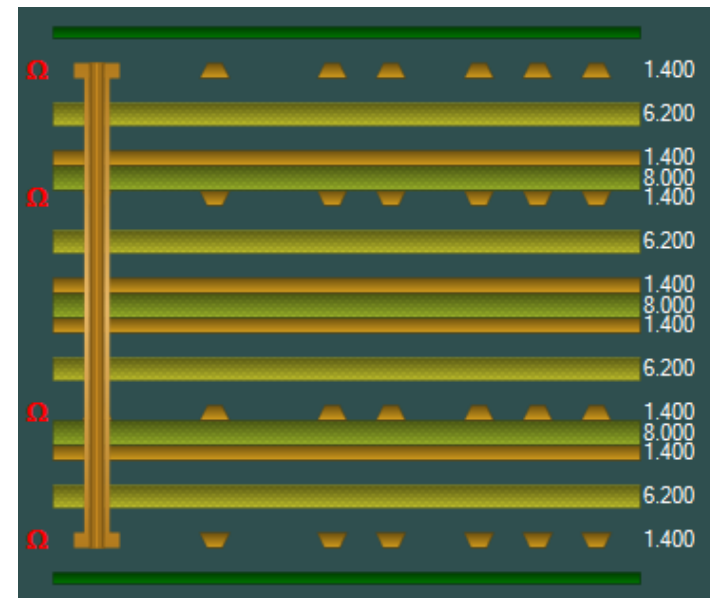
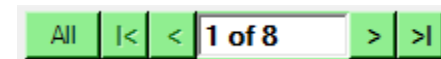
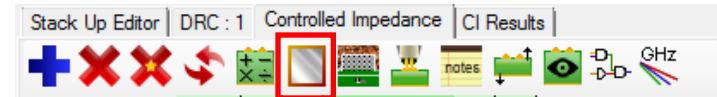
SM	Liquid Photo Imageable (LPI)	4.000/0.0200	1.0000
1	Foil	Copper Foil 1oz	1.4000
PP	Prepreg Region	4.200/0.0200	6.2000
2	Core	Standard FR4 Core 1oz / 1oz	1.4000
3	Core	Standard FR4 Core 1oz / 1oz	8.0000
3	Core	Standard FR4 Core 1oz / 1oz	1.4000
PP	Prepreg Region	4.200/0.0200	6.2000
4	Core	Standard FR4 Core 1oz / 1oz	1.4000
5	Core	Standard FR4 Core 1oz / 1oz	8.0000
5	Core	Standard FR4 Core 1oz / 1oz	1.4000
PP	Prepreg Region	4.200/0.0200	6.2000
6	Core	Standard FR4 Core 1oz / 1oz	1.4000
7	Core	Standard FR4 Core 1oz / 1oz	8.0000
7	Core	Standard FR4 Core 1oz / 1oz	1.4000
PP	Prepreg Region	4.200/0.0200	6.2000
8	Foil	Copper Foil 1oz	1.4000
SM	Liquid Photo Imageable (LPI)	4.000/0.0200	1.0000

The structure browse control shows four structures

Omega ( $\Omega$ ) symbol placed next to layers that contain structures

## Step 6: Adding impedance structures – mirroring structures

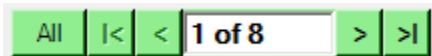
- As the stack is symmetrical, selecting ‘Mirror Structures’ will place four more structures on the lower half of the stack
- At this point the structure browse control will display eight structures in total
- The  $\Omega$  symbol is now placed next to layers 1, 3, 6, 8
- This is an appropriate stage to save the stack up project as described in Step 3.





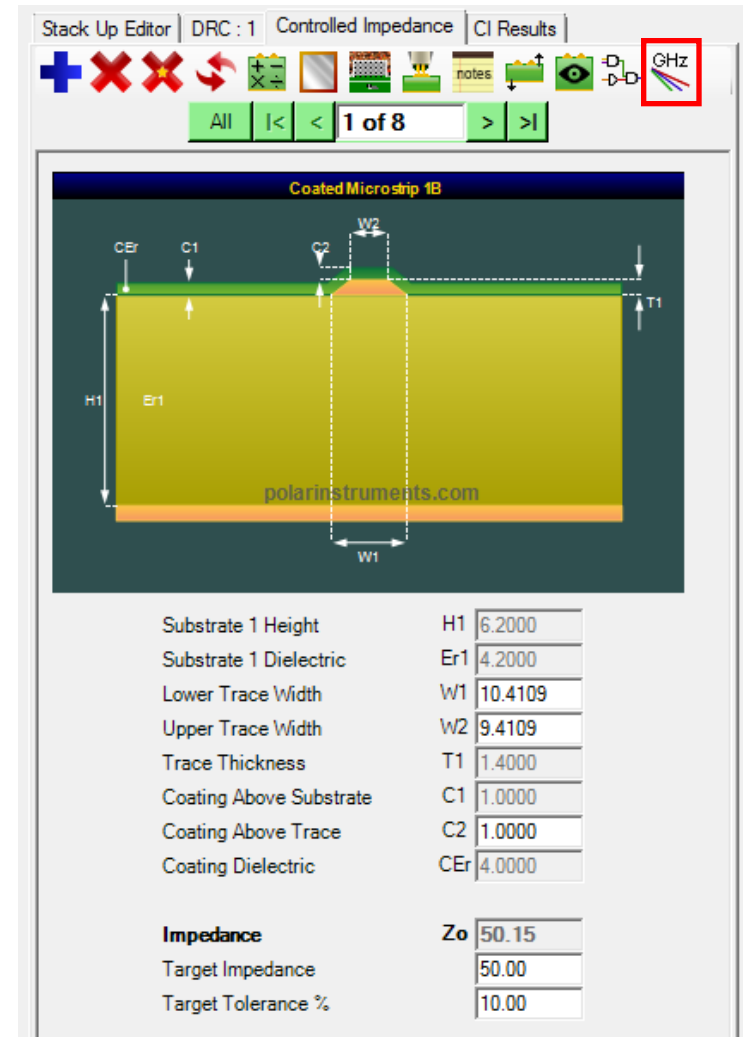
## Step 7: Frequency Dependent Loss Calculations

- Each structure that has been added to the stack up has a set of Frequency Dependent Properties that are accessible using this icon
- In this example we have selected structure 1 of 8.



- On selecting the  icon the following dialog is displayed

- Please note: Frequency Dependent Loss Calculations are only available with the Speedstack Si package*



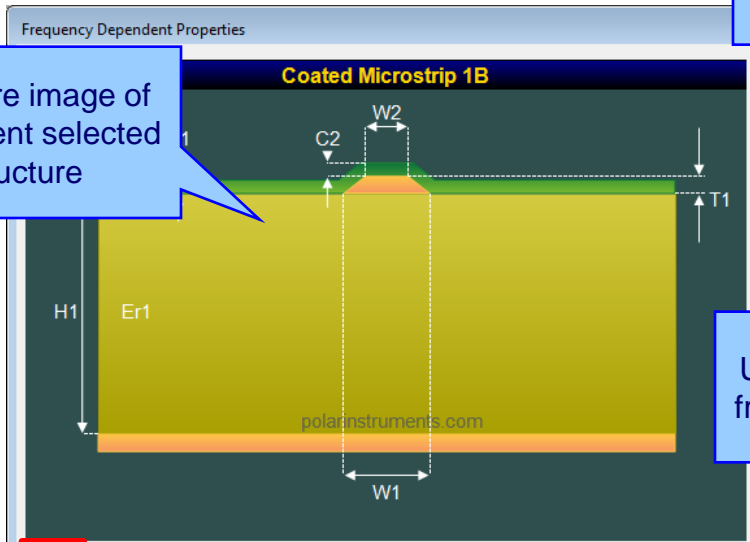
The screenshot shows the 'Stack Up Editor' interface with 'DRC : 1', 'Controlled Impedance', and 'CI Results' tabs. A 'GHz' icon is highlighted in a red box. Below the navigation buttons, a cross-section diagram of a 'Coated Microstrip 1B' is shown with labels for CEr, C1, C2, W2, W1, H1, E1, and T1. Below the diagram is a table of properties:

Substrate 1 Height	H1	6.2000
Substrate 1 Dielectric	Er1	4.2000
Lower Trace Width	W1	10.4109
Upper Trace Width	W2	9.4109
Trace Thickness	T1	1.4000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Dielectric	CEr	4.0000
<b>Impedance</b>		<b>Zo</b>
Target Impedance		50.00
Target Tolerance %		10.00



Result presentation, show plot and table of results in preferred units.

Structure image of the current selected structure



User-specifiable frequency range.

Frequency Dependent Properties

Length of Line LL: 1000.0000

Trace Conductivity (S/m) TC: 5.800E+07

Frequency Minimum (MHz) FMin: 500.0000

Frequency Maximum (GHz) FMax: 10.0000

Frequency Steps FStep: 20

Frequency of Interest (MHz) Fr: 1000.0000

Calculate

Result Presentation

Length of Line  in  /m

Substrate Causal Extrapolation Reference Points

Set Dielectric Constant (Er) from Stack Up materials

Set Loss Tangent (TanD) from Stack Up materials

	Freq (Hz)	Ref Er	Ref TanD
H1	1.000E+09	4.2000	0.0200
H2			
H3			
H4			
REr			
CEr	1.000E+09	4.0000	0.0200

Surface Roughness Compensation

Smooth

Hammerstad

Grosse

Huray

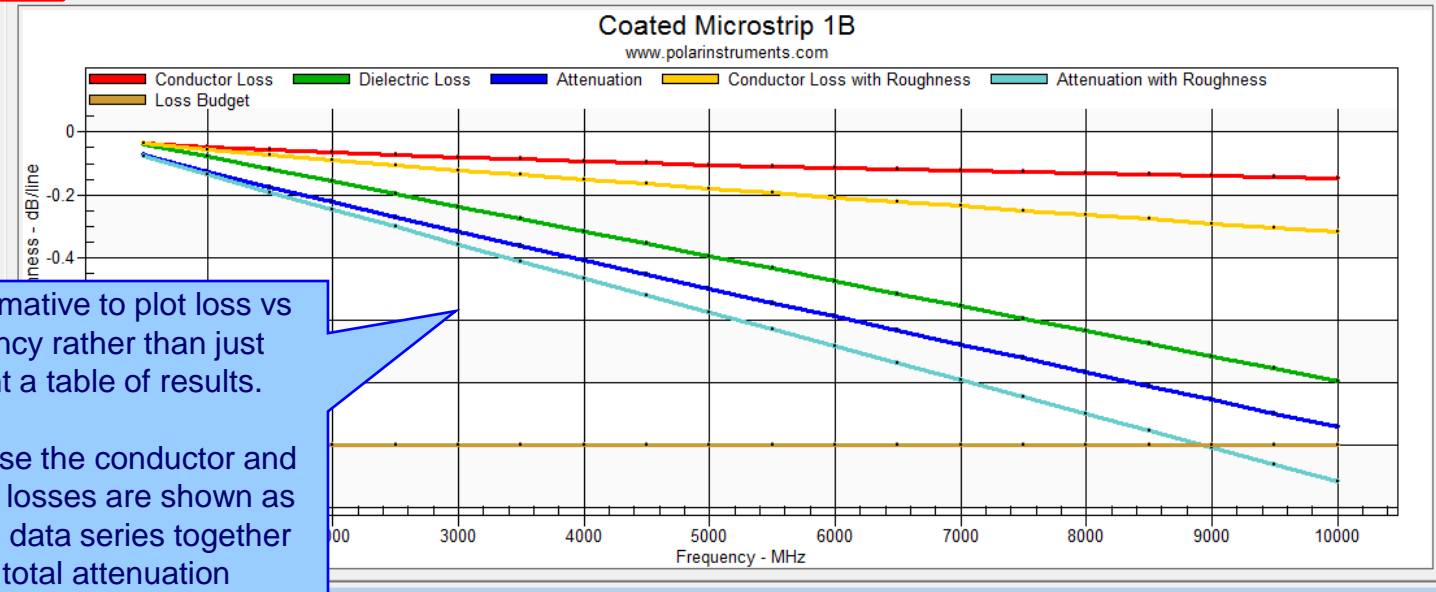
Print Settings

Include Loss Graph for this structure

Dielectric constant and loss tangent properties for each substrate dielectric / region

Surface roughness compensation model. Hammerstad, Grosse and Huray methods supported

Graph Single Ended



It is informative to plot loss vs frequency rather than just present a table of results.

In this case the conductor and dielectric losses are shown as separate data series together with total attenuation

Graph Settings

Display Settings

All Losses

Loss Budget (dB)

-1.0000 Refresh

Picked Data Point Information

Frequency (MHz): 10000.000

Attenuation with Roughness (dB): -1.113

Maximise Print Export

The plot is interactive. It is possible to select data points and drill down to the underlying loss data

**Coated Microstrip 1B**

Length of Line LL: 1000.0000

Trace Conductivity (S/m) TC: 5.800E+07

Frequency Minimum (MHz) FMin: 500.0000

Frequency Maximum (GHz) FMax: 10.0000

Frequency Steps FStep: 20

Frequency of Interest (MHz) Freq: 4000.0000

Calculate

Result Presentation

Length of Line  /in  /m

Substrate Causal Extrapolation Reference Points

Set Dielectric Constant (Er) from Stack Up materials

Set Loss Tangent (TanD) from Stack Up materials

	Freq (Hz)	Ref Er	Ref TanD
H1	1.000E+09	4.2000	0.0200
H2			
H3			
H4			
REr			
CEr	1.000E+09		

Surface Roughness Comp...  
 Smooth  
 Hammerstad  
 Groisse  
 Huray

Print Settings  
 Include Loss Graph for this structure report

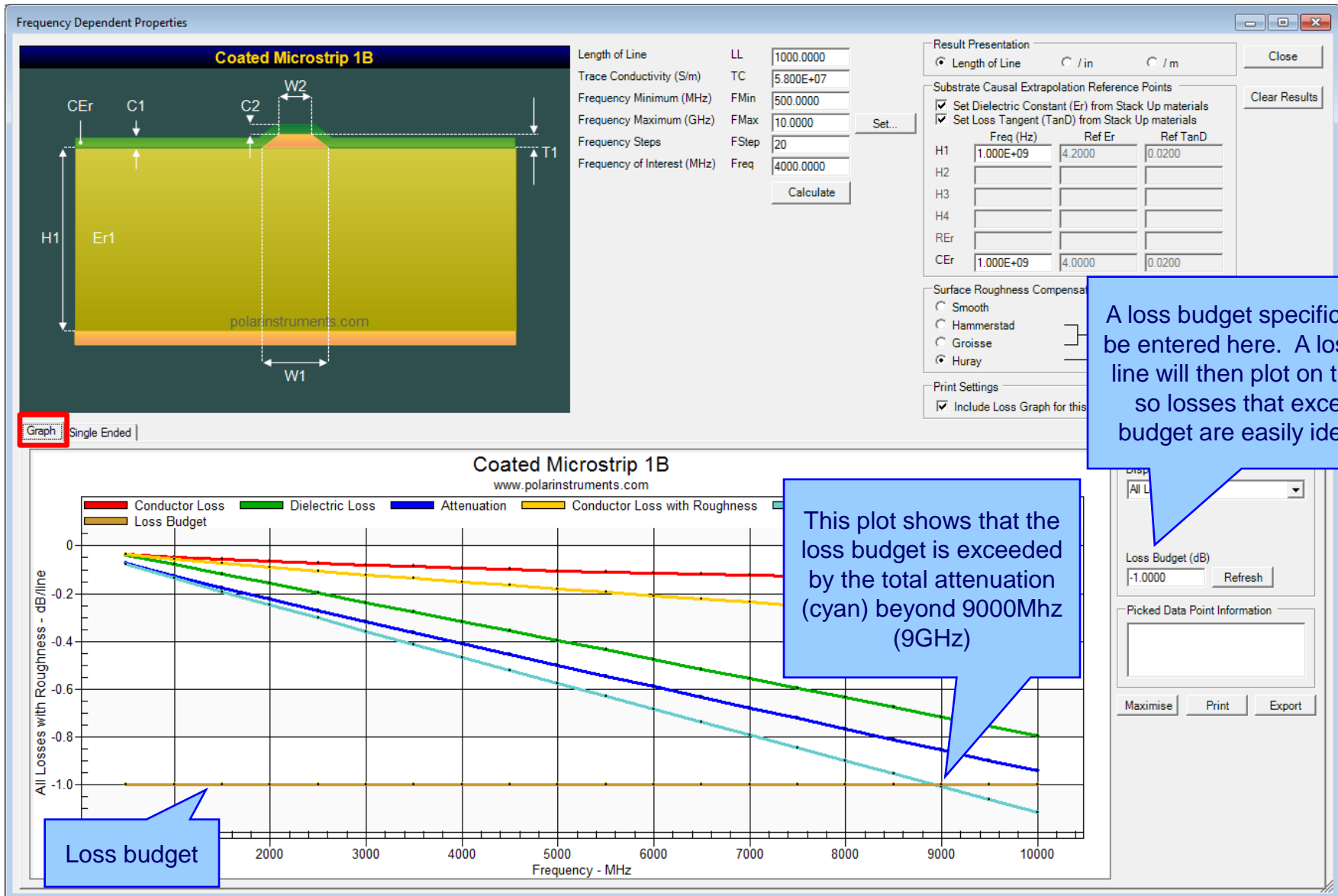
It is possible to specify a 'Frequency of Interest' as some insertion loss requirements / loss budget specifications are for a given frequency. In this case 4000MHz (4GHz)

Frequency dependent results shown as a data table

Graph [Single Ended]

Frequency Hz	Impedance Real Ohms	Impedance Imaginary Ohms	Impedance Magnitude Ohms	Inductance H/line	Resistance Ohms/line	Capacitance F/line	Conductance S/line	Skin Depth in	Conductor Loss dB/line	Dielectric Loss dB/line	Attenuation dB/line	Conductor Loss With Roughness dB/line	Attenuation With Roughness dB/line	Modal Phase Velocity in/s	Alpha Np/line
5.000E+08	5.125E+01	4.388E-02	5.125E+01	8.171E-09	4.276E-01	3.110E-12	1.795E-04	1.164E-04	-3.349E-02	-3.924E-02	-7.273E-02	-3.694E-02	-7.618E-02	6.273E+09	8.771E-03
1.000E+09	5.129E+01	1.482E-01	5.129E+01	8.118E-09	6.499E-01	3.086E-12	3.591E-04	8.228E-05	-4.710E-02	-7.863E-02	-1.257E-01	-5.637E-02	-1.350E-01	6.319E+09	1.554E-02
1.500E+09	5.132E+01	1.924E-01	5.132E+01	8.090E-09	8.472E-01	3.071E-12	5.387E-04	6.718E-05	-5.751E-02	-1.181E-01	-1.756E-01	-7.363E-02	-1.918E-01	6.344E+09	2.208E-02
2.000E+09	5.135E+01	2.178E-01	5.135E+01	8.071E-09	1.033E+00	3.061E-12	7.183E-04	5.818E-05	-6.627E-02	-1.577E-01	-2.240E-01	-8.990E-02	-2.476E-01	6.362E+09	2.850E-02
2.500E+09	5.137E+01	2.347E-01	5.137E+01	8.057E-09	1.213E+00	3.053E-12	8.980E-04	5.204E-05	-7.398E-02	-1.973E-01	-2.713E-01	-1.056E-01	-3.029E-01	6.376E+09	3.487E-02
3.000E+09	5.138E+01	2.468E-01	5.138E+01	8.045E-09	1.389E+00	3.047E-12	1.078E-03	4.750E-05	-8.094E-02	-2.370E-01	-3.179E-01	-1.209E-01	-3.579E-01	6.387E+09	4.120E-02
3.500E+09	5.140E+01	2.561E-01	5.140E+01	8.035E-09	1.561E+00	3.041E-12	1.257E-03	4.398E-05	-8.733E-02	-2.766E-01	-3.640E-01	-1.359E-01	-4.126E-01	6.397E+09	4.750E-02
4.000E+09	5.141E+01	2.635E-01	5.141E+01	8.027E-09	1.731E+00	3.036E-12	1.437E-03	4.114E-05	-9.328E-02	-3.164E-01	-4.097E-01	-1.507E-01	-4.671E-01	6.405E+09	5.378E-02
4.500E+09	5.142E+01	2.695E-01	5.142E+01	8.020E-09	1.899E+00	3.032E-12	1.617E-03	3.879E-05	-9.886E-02	-3.561E-01	-4.550E-01	-1.653E-01	-5.215E-01	6.413E+09	6.004E-02
5.000E+09	5.143E+01	2.746E-01	5.144E+01	8.013E-09	2.065E+00	3.028E-12	1.797E-03	3.679E-05	-1.041E-01	-3.959E-01	-5.000E-01	-1.798E-01	-5.757E-01	6.419E+09	6.628E-02
5.500E+09	5.144E+01	2.789E-01	5.144E+01	8.007E-09	2.230E+00	3.024E-12	1.976E-03	3.508E-05	-1.091E-01	-4.357E-01	-5.448E-01	-1.941E-01	-6.298E-01	6.425E+09	7.251E-02
6.000E+09	5.145E+01	2.827E-01	5.145E+01	8.002E-09	2.394E+00	3.020E-12	2.155E-03	3.359E-05	-1.139E-01	-4.755E-01	-5.895E-01	-2.083E-01	-6.838E-01	6.431E+09	7.873E-02
6.500E+09	5.146E+01	2.860E-01	5.146E+01	7.997E-09	2.556E+00	3.016E-12	2.334E-03	3.209E-05	-1.187E-01	-5.152E-01	-6.339E-01	-2.224E-01	-7.378E-01	6.436E+09	8.494E-02
7.000E+09	5.147E+01	2.889E-01	5.147E+01	7.992E-09	2.718E+00	3.012E-12	2.514E-03	3.069E-05	-1.235E-01	-5.549E-01	-6.782E-01	-2.364E-01	-7.916E-01	6.440E+09	9.114E-02
7.500E+09	5.148E+01	2.916E-01	5.148E+01	7.988E-09	2.878E+00	3.008E-12	2.693E-03	2.919E-05	-1.282E-01	-5.936E-01	-7.223E-01	-2.502E-01	-8.453E-01	6.445E+09	9.732E-02
8.000E+09	5.148E+01	2.940E-01	5.148E+01	7.984E-09	3.037E+00	3.004E-12	2.872E-03	2.769E-05	-1.329E-01	-6.324E-01	-7.663E-01	-2.640E-01	-8.990E-01	6.449E+09	1.035E-01

The 'Frequency of Interest' result is highlighted in the data table



A loss budget specification can be entered here. A loss budget line will then plot on the graph so losses that exceed the budget are easily identifiable

This plot shows that the loss budget is exceeded by the total attenuation (cyan) beyond 9000MHz (9GHz)

Loss budget

## Step 7: Frequency Dependent Loss Calculations

To accurately calculate Conductor Loss it is necessary to specify the surface roughness parameters. Speedstack supports multiple roughness models: Hammerstad, Groisse, Huray and Cannonball-Huray. In this example the Huray method is used, the dialog prompts for the required roughness parameters.

Substrate Causal Extrapolation Reference Points

Set Dielectric Constant (Er) from Stack Up materials  
 Set Loss Tangent (TanD) from Stack Up materials

	Freq (Hz)	Ref Er	Ref TanD
H1	1.000E+09	4.2000	0.0200
H2			
H3			
H4			
REr			
CEr	1.000E+09	4.0000	0.0200

In order to accurately calculate Dielectric Loss it is important to understand the material / substrate properties. These substrate properties including dielectric constant (Er) and loss tangent (TanD) are specified here for each structure substrate region. Speedstack causally extrapolates Er and TanD over the specified frequency range using the Svensson-Djordjevic method, hence the ability to specify the extrapolation reference points for each substrate region. The reference point data is usually available from the material supplier data sheet and can be added to the Speedstack material library. The checkbox options will automatically populate these fields from the stack up materials.

Surface Roughness Compensation

Smooth  
 Hammerstad  
 Groisse  
 Huray

Surface Roughness Compensation - Huray

Images by courtesy of Circuit Foil Luxembourg

Ratio of Areas: 1.0000  
 Effective Ball Radius (µm): 0.2690  
 Area of Ball Count (sq µm): 2.6050  
 Number of Balls in Area: 14

**Cannonball-Huray Model**

Enable Cannonball-Huray

Matte-Side Roughness  
 Rz Matte (µm): 5.0000

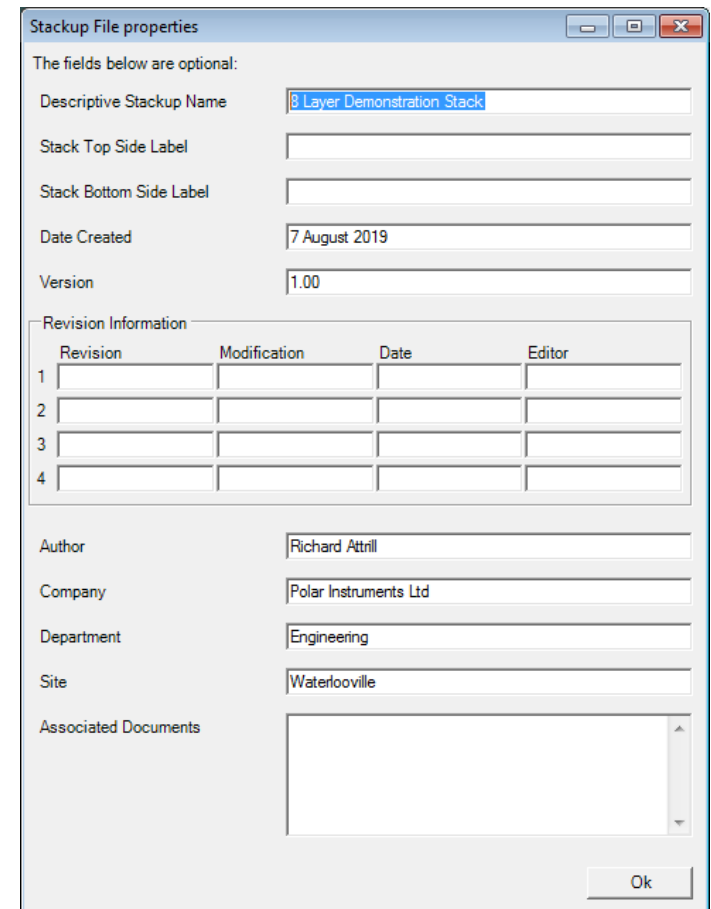
Drum-Side Roughness  
 Rz Drum (µm): 4.0000

www.polarinstruments.com  
 Courtesy of Bert Simonovich, Lamsim Enterprises Inc [Application Note](#)

## Step 8: Printing a technical report

The 8 layer stack up with its drilling and impedance structure information is now complete, the final step is to generate a technical report

- Use the File | Properties option to add useful information about the stack up, such as descriptive stack up name, date created, author and company information
- Load the Technical Report option by using the File | Print | Technical Report



Stackup File properties

The fields below are optional:

Descriptive Stackup Name: 8 Layer Demonstration Stack

Stack Top Side Label:

Stack Bottom Side Label:

Date Created: 7 August 2019

Version: 1.00

Revision Information

Revision	Modification	Date	Editor
1	<input type="text"/>	<input type="text"/>	<input type="text"/>
2	<input type="text"/>	<input type="text"/>	<input type="text"/>
3	<input type="text"/>	<input type="text"/>	<input type="text"/>
4	<input type="text"/>	<input type="text"/>	<input type="text"/>

Author: Richard Attrill

Company: Polar Instruments Ltd

Department: Engineering

Site: Waterfooville

Associated Documents:

Ok

# Step 8: Printing a technical report (continued)

**Stack up image with drilling information**

**Stack up information, with customisable columns**

**Stack up thickness info**

**Impedance information, with customisable columns**

**Stack up property info**

**Company logo goes here**



Layer	Stack up	Description	Processed Thickness	er	Loss Tangent	Impedance ID
1		Liquid Photo Imageable (LPI)	1.000	4.000	0.0200	
2		Copper Foil 1oz	1.400			1, 2
3		Prepreg Region	6.200	4.200	0.0200	
4		Standard FR4 Core 1oz / 1oz	1.400			3, 4
5		Prepreg Region	6.200	4.200	0.0200	
6		Standard FR4 Core 1oz / 1oz	1.400			5, 6
7		Prepreg Region	6.200	4.200	0.0200	
8		Copper Foil 1oz	1.400			7, 8
9		Liquid Photo Imageable (LPI)	1.000	4.000	0.0200	

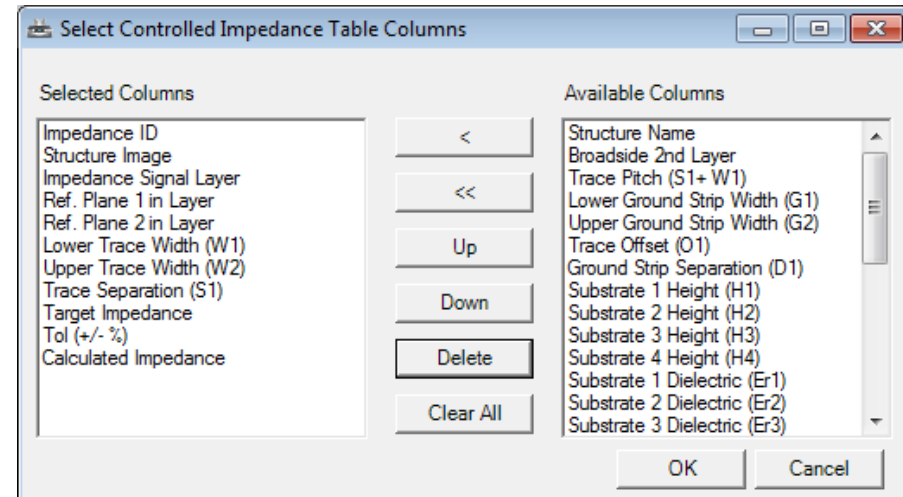
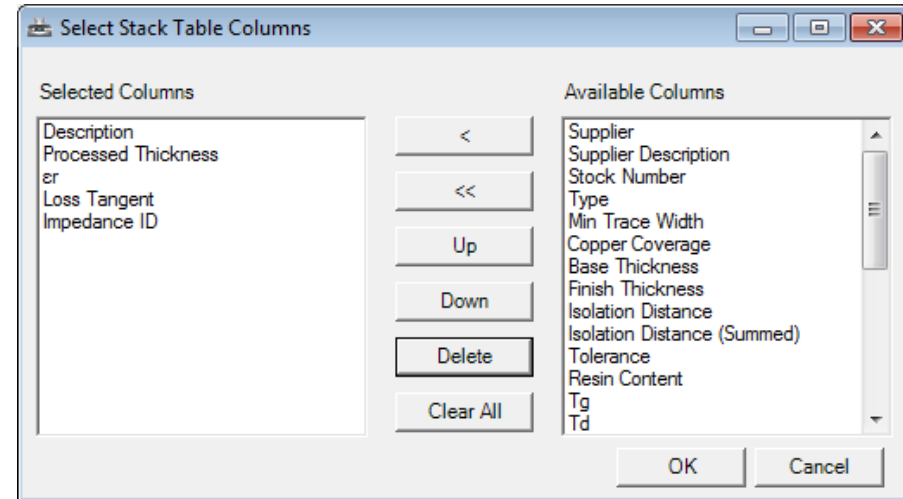
Copper Thickness = 11.200 | Dielectric Thickness = 48.800 | Solder Mask Thickness = 2.000 | Stack Up Thickness = 60.000 | Stack Up Thickness with Soldermask = 62.000

Impedance ID	Structure Image	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Target Impedance	Tol (+/- %)	Calculated Impedance
1		1	2	0	10.411	9.411	0.000	50.000	10.000	50.150
2		1	2	0	8.568	7.569	11.432	100.000	10.000	100.040
3		3	2	4	5.350	4.350	0.000	50.000	10.000	50.160
4		3	2	4	5.155	4.155	14.845	100.000	10.000	99.670
5		6	5	7	5.350	4.350	0.000	50.000	10.000	50.160

StackName: 8 Layer Demonstration Stack		Associated Documents:		Revision:	Modification:	Date of Revision:	Editor	Page 1/X
Drawing No: 1.00								
Date: 7 August 2019								
Author: Richard Atwill								
Department: Engineering								
Waterfootville								

## Step 8: Printing a technical report (continued)


- Use the  Select Stack Data Columns option to select the fields that you wish to print next to the stack up graphic
- Use the  Select Impedance Data Columns option to configure the impedance structure table

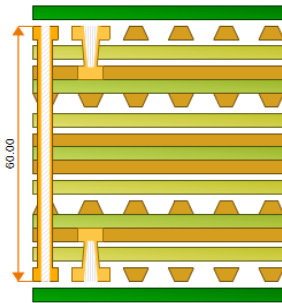









# Step 8: Printing a technical report (continued) – sample output

C:\Program Files\Polar\Speedstack\Samples\Speedstack\_GettingStarted\_VMM\_CI\_2019.sci      Units: Mils



Layer	Stack up	Description	Processed Thickness	εr	Loss Tangent	Impedance ID
		Liquid Photo Imageable (LPI)	1.000	4.000	0.0200	
1		Copper Foil 1oz	1.400			1, 2
2		Prepreg Region	6.200	4.200	0.0200	
3		Standard FR4 Core 1oz / 1oz	1.400			3, 4
4		Prepreg Region	6.200	4.200	0.0200	
5		Standard FR4 Core 1oz / 1oz	1.400			5, 6
6		Prepreg Region	6.200	4.200	0.0200	
7		Copper Foil 1oz	1.400			7, 8
8		Liquid Photo Imageable (LPI)	1.000	4.000	0.0200	

Copper Thickness = 11.200 | Dielectric Thickness = 48.800 | Solder Mask Thickness = 2.000 | Stack Up Thickness = 60.000 | Stack Up Thickness with Soldermask = 62.000

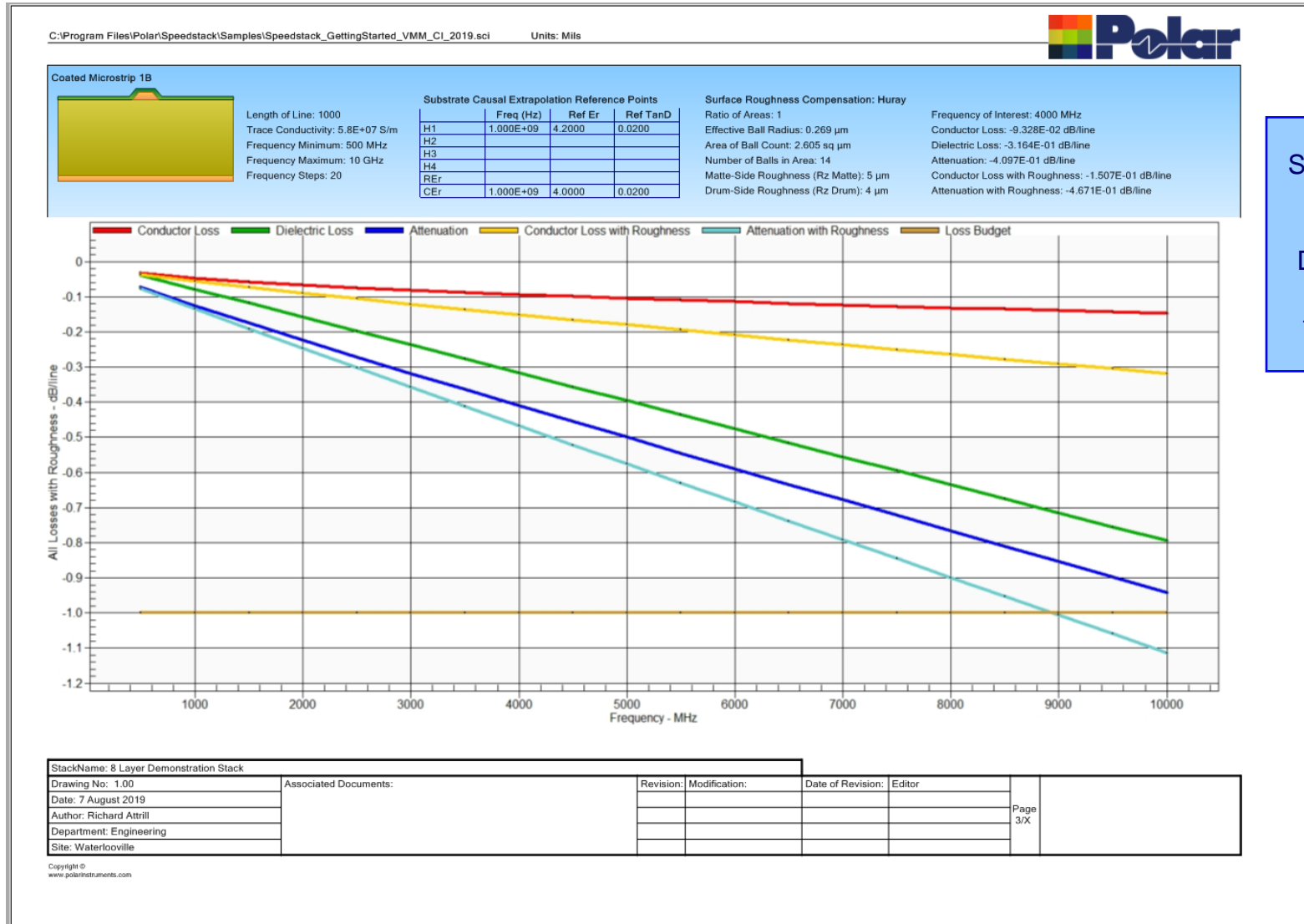
Impedance ID	Structure Image	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Target Impedance	Tol (+/- %)	Calculated Impedance
1		1	2	0	10.411	9.411	0.000	50.000	10.000	50.150
2		1	2	0	8.568	7.569	11.432	100.000	10.000	100.040
3		3	2	4	5.350	4.350	0.000	50.000	10.000	50.160
4		3	2	4	5.155	4.155	14.845	100.000	10.000	99.670
5		6	5	7	5.350	4.350	0.000	50.000	10.000	50.160

StackName: 8 Layer Demonstration Stack		Revision:		Modification:		Date of Revision:		Editor	
Drawing No: 1.00	Associated Documents:								
Date: 7 August 2019									
Author: Richard Attrill									
Department: Engineering									
Site: Waterloooville									

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# Step 8: Printing a technical report (continued) – sample output



Select this toolbar icon to add Frequency Dependent Loss Graphs to the technical report

## Summary

Thanks for completing the Getting Started tutorial.

I hope it proved a useful introduction to the stack up creation process using Speedstack and that you enjoyed using it.

If you have any questions please feel free to contact your local Polar office at:

[www.polarinstruments.com/distrib/international\\_offices.html](http://www.polarinstruments.com/distrib/international_offices.html)

or contact us at [polarcare@polarinstruments.com](mailto:polarcare@polarinstruments.com)

Thanks again for using Speedstack.

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