

Layer	Stack up	Supplier	Supplier Description	Description	Type	Processed Thickness	Mask Thickness	εr	Color	Copper Layer Type	Impedance ID	Notes-1
1		Polar Samples	SM/001	Liquid PhotoImageable Mask	SolderMask	25.400	25.400	4.000	Green			
		Polar Samples	FO/001	Copper Foil	Copper	35.560				Signal	1, 2	
		Polar Samples	PP/003	PrePreg 3113	Dielectric	88.265		4.200				
		Polar Samples	FO/001	Copper Foil	Copper	17.780				Signal		
		Polar Samples	PP/001	PrePreg 1080	Dielectric	74.422		4.200				
		Polar Samples	CO/017	FR4 Core	FR4	35.560		4.200		Plane		
		Polar Samples	CO/017	FR4 Core	FR4	203.200		4.200		Signal	3, 4	
		Polar Samples	PP/001	PrePreg 1080	Dielectric	66.718		4.200				
		Polar Samples	PP/001	PrePreg 1080	Dielectric	66.718		4.200				
		Polar Samples	PP/001	PrePreg 1080	Dielectric	66.718		4.200				
2		Polar Samples	CO/017	FR4 Core	FR4	35.560		4.200		Plane		
		Polar Samples	PP/001	PrePreg 1080	Dielectric	66.718		4.200				
		Polar Samples	PP/001	PrePreg 1080	Dielectric	66.718		4.200				
		Polar Samples	PP/001	PrePreg 1080	Dielectric	66.718		4.200				
		Polar Samples	CO/017	FR4 Core	FR4	203.200		4.200		Signal	5, 6	
		Polar Samples	CO/017	FR4 Core	FR4	35.560		4.200		Plane		
		Polar Samples	PP/001	PrePreg 1080	Dielectric	74.422		4.200				
		Polar Samples	PP/001	PrePreg 1080	Dielectric	66.718		4.200				
		Polar Samples	PP/001	PrePreg 1080	Dielectric	66.718		4.200				
		Polar Samples	PP/001	PrePreg 1080	Dielectric	66.718		4.200				
3		Polar Samples	CO/017	FR4 Core	FR4	35.560		4.200		Signal		
		Polar Samples	PP/001	PrePreg 1080	Dielectric	74.422		4.200				
		Polar Samples	FO/001	Copper Foil	Copper	17.780				Signal		
		Polar Samples	PP/003	PrePreg 3113	Dielectric	88.265		4.200				
		Polar Samples	FO/001	Copper Foil	Copper	35.560				Signal	7, 8	
		Polar Samples	SM/001	Liquid PhotoImageable Mask	SolderMask	25.400	25.400	4.000	Green			

Copper Coverage Finishing Class : 'Class 2' = 18.000

Impedance ID	Structure Image	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Target Impedance	Tol (+/- %)	Calculated Impedance	Structure Name	Error %	Trace Thickness (T1)	Lower Ground Strip Width (G1)	Upper Ground Strip Width (G2)	Broadside 2nd Layer	Trace Pitch (S1+ W1)	Trace Offset (O1)	Ground Strip Separation (D1)
1		1	3	0	304.800	279.400	0.000	50.000	10.000	50.400	Coated Microstrip 1B	0.8	35.560	0.000	0.000	0	0.000	0.000	0.000
2		1	3	0	203.200	177.800	184.150	100.000	10.000	99.710	Edge Coupled Coated Microstrip 1B	0.3	35.560	0.000	0.000	0	387.350	0.000	0.000
3		4	3	5	152.400	139.700	0.000	50.000	10.000	50.160	Offset Stripline 1B1A	0.3	35.560	0.000	0.000	0	0.000	0.000	0.000
4		4	3	5	101.600	88.900	177.800	100.000	10.000	99.960	Edge Coupled Offset Stripline 1B1A	0.0	35.560	0.000	0.000	0	279.400	0.000	0.000

StackName: Polar 10 Layer demo mils design	Release: 2023	Revision: R1 1.001	Modification: M1Sample Stack	Date of Revision: D114 October 2022	Editor: E1Mike Cotterill	Page 1/3
Timestamp: 12 Oct 2022	Associated Documents: Stackup report generated by Polar Speedstack PCB stackup design and documentation system.	R2	M2	D2	E2	
Authority: Richard Attrill		R3	M3	D3	E3	
Customer: Engineering		R4	M4	D4	E4	
Parent: Waterlooville						



Impedance ID	Structure Image	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Target Impedance	Tol (+/- %)	Calculated Impedance	Structure Name	Error %	Trace Thickness (T1)	Lower Ground Strip Width (G1)	Upper Ground Strip Width (G2)	Broadside 2nd Layer	Trace Pitch (S1+ W1)	Trace Offset (O1)	Ground Strip Separation (D1)
5		7	6	8	152.400	139.700	0.000	50.000	10.000	50.160	Offset Stripline 1B1A	0.3	35.560	0.000	0.000	0	0.000	0.000	0.000
6		7	6	8	101.600	88.900	177.800	100.000	10.000	99.960	Edge Coupled Offset Stripline 1B1A	0.0	35.560	0.000	0.000	0	279.400	0.000	0.000
7		10	8	0	304.800	279.400	0.000	50.000	10.000	50.400	Coated Microstrip 1B	0.8	35.560	0.000	0.000	0	0.000	0.000	0.000
8		10	8	0	203.200	177.800	184.150	100.000	10.000	99.710	Edge Coupled Coated Microstrip 1B	0.3	35.560	0.000	0.000	0	387.350	0.000	0.000

Drill Image	1st Layer	2nd Layer	Column Position	Drill Type	Fill Type	Hole Count	Different Hole Sizes	Minimum Size	Data Filenames	Minimum Pad Size	Minimum Drill Size	Minimum Drill Size Tolerance	Minimum Barrel Wall Thickness	Maximum Distance From Cut Layer	Minimum Distance From Cut Layer	Must-Cut Layer No	Must-Not-Cut Layer No	Primary Drill Size	Minimum Distance From Not-Cut Layer	Maximum Distance From Not-Cut Layer
	1	2	5	Laser PTH	None	0	0	762.000		0.000	0.000	0.000	0.000	0.000	0.000	-	-	0.000	0.000	0.000
	1	6	9	Mechanical PTH	None	0	0	254.000		0.000	0.000	0.000	0.000	0.000	0.000	-	-	0.000	0.000	0.000
	1	7	8	Mechanical PTH	None	0	0	254.000		0.000	0.000	0.000	0.000	0.000	0.000	-	-	0.000	0.000	0.000
	1	8	7	Mechanical PTH	None	0	0	254.000		0.000	0.000	0.000	0.000	0.000	0.000	-	-	0.000	0.000	0.000
	1	10	1	Mechanical PTH	None	0	0	254.000		0.000	0.000	0.000	0.000	0.000	0.000	-	-	0.000	0.000	0.000
	2	4	5	Laser PTH	Copper Fill	0	0	762.000		0.000	0.000	0.000	0.000	0.000	0.000	-	-	0.000	0.000	0.000
	2	9	2	Mechanical PTH	None	0	0	254.000		0.000	0.000	0.000	0.000	0.000	0.000	-	-	0.000	0.000	0.000

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Authority: Richard Attrill	Stackup report generated by Polar Speedstack PCB stackup design and documentation system.	R2	M2	D2	E2	
Customer: Engineering		R3	M3	D3	E3	
Parent: Waterlooville		R4	M4	D4	E4	