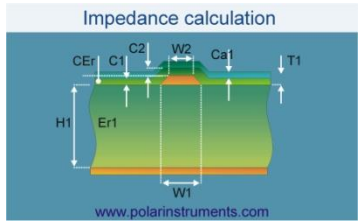
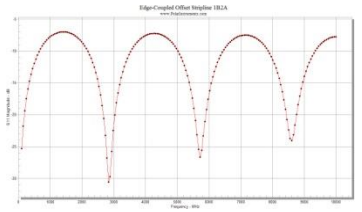
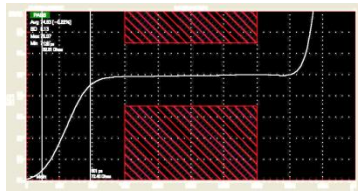
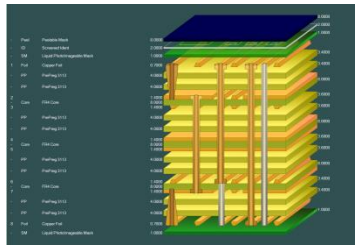
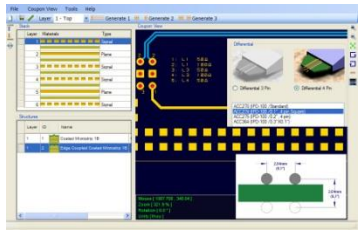




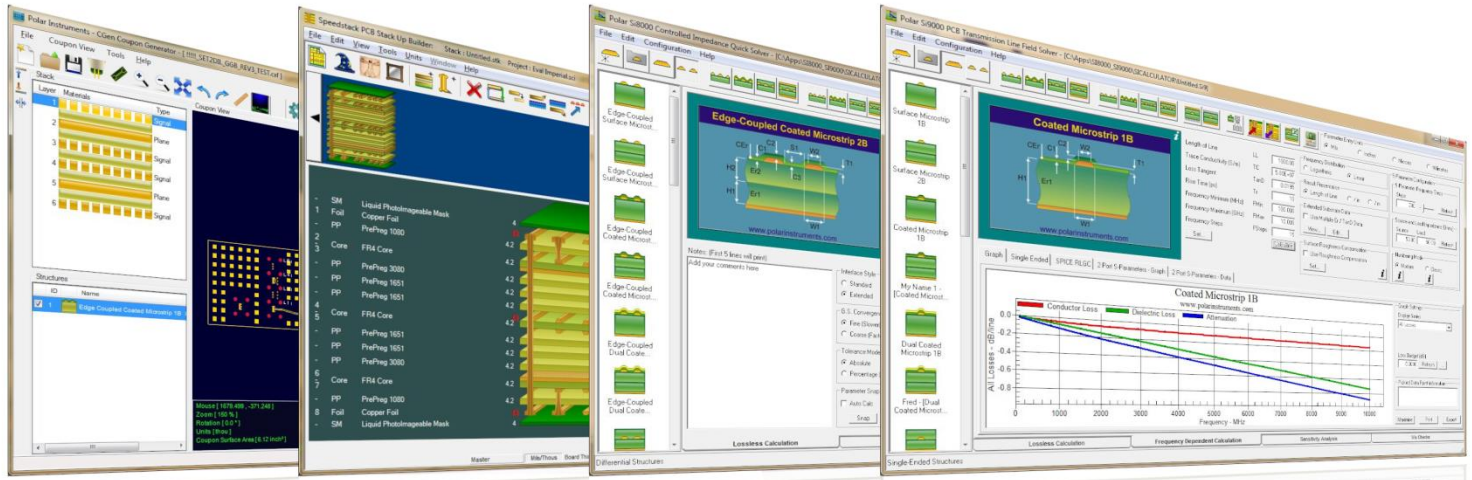






How is a PCB made ?
What determines impedance ?

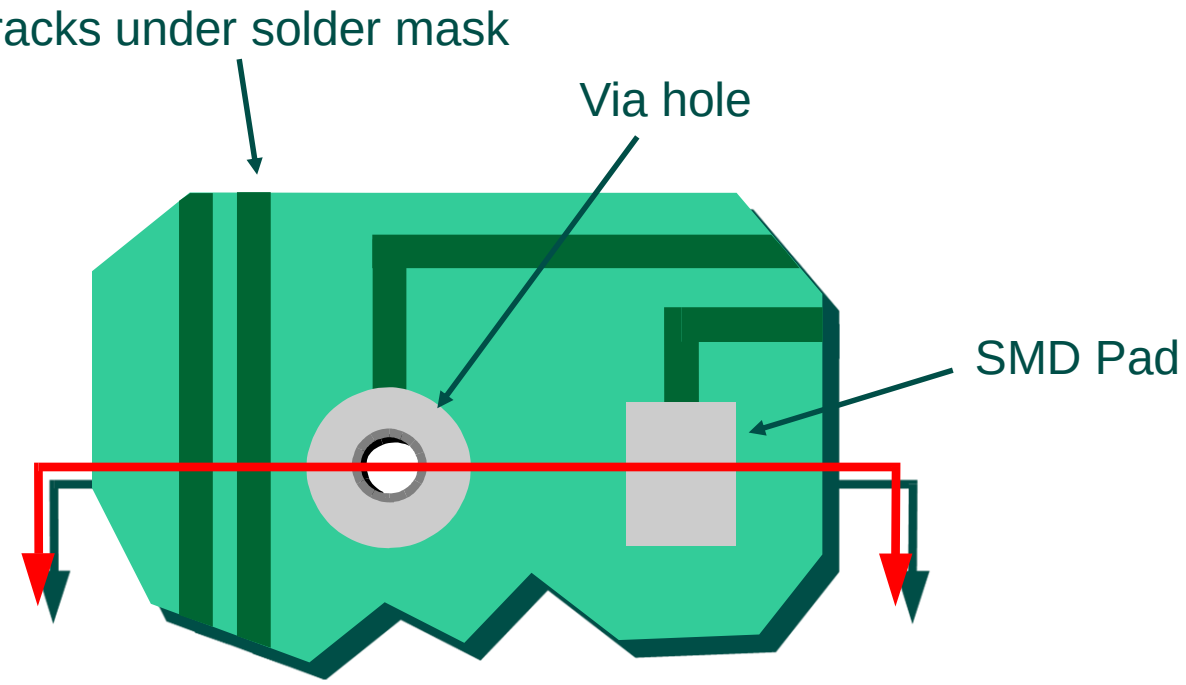
Martyn Gaudion – Jan 2023 (Rev 2A)



Manufacturing Processes for a Multi-layer PCB

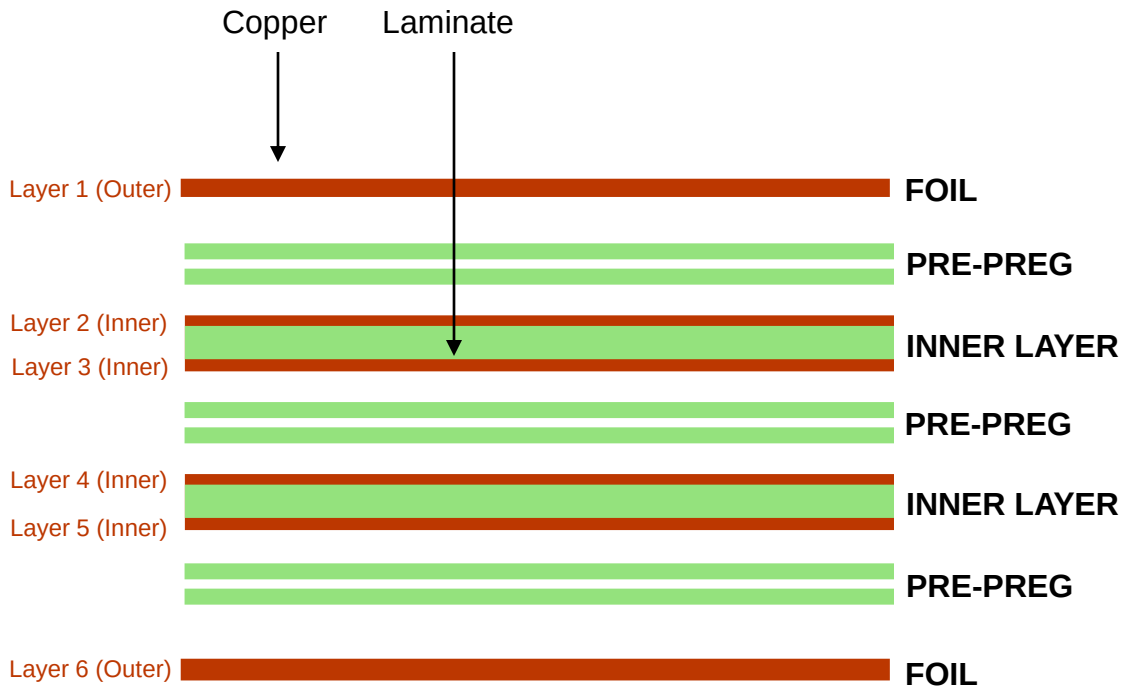
The following presentation covers the main processes during the production of a multi-layer PCB.

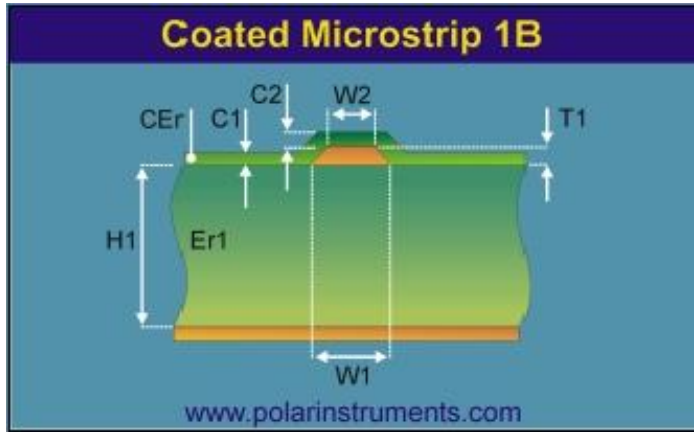
The diagrams which follow represent a section through a 6 layer PCB, as indicated in red.



Section through PCB

Typical Layer Construction - 6 Layer PCB

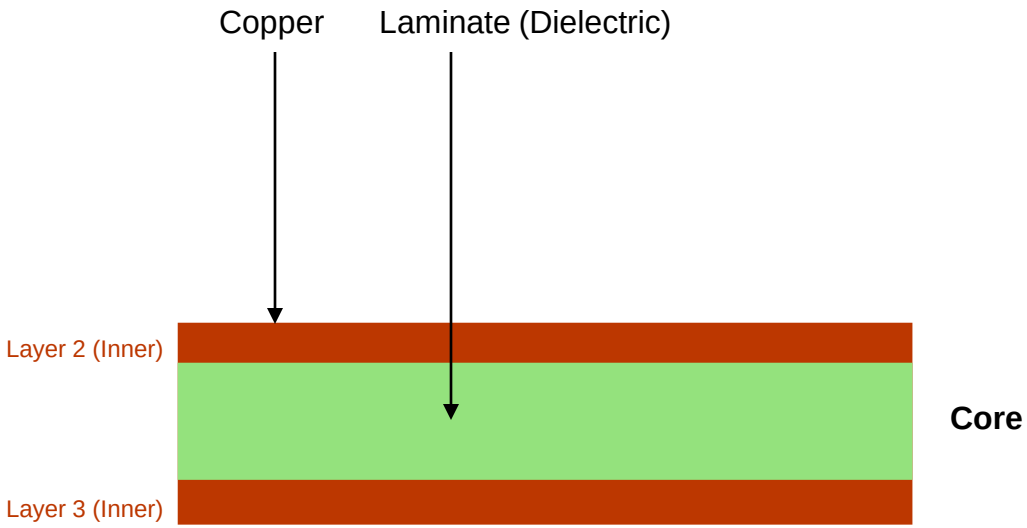


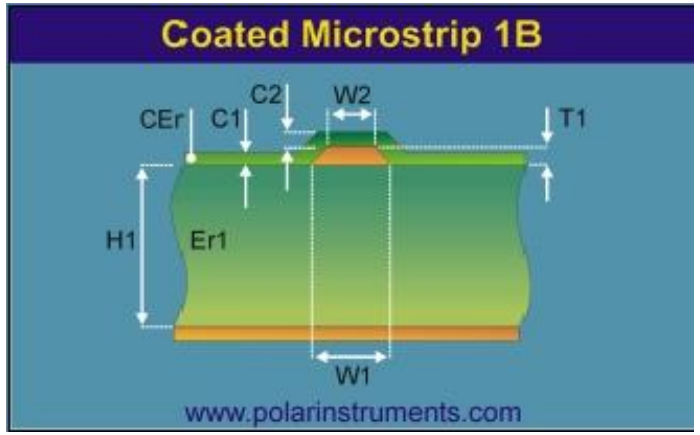


Impedance Considerations

- Layer build / stackup is one of the most important aspects of controlled impedance
- Many combinations of material thickness and copper weights can be used.
- PCB Fabricators manufacturing techniques vary

Inner Layer Processing – Material Selection



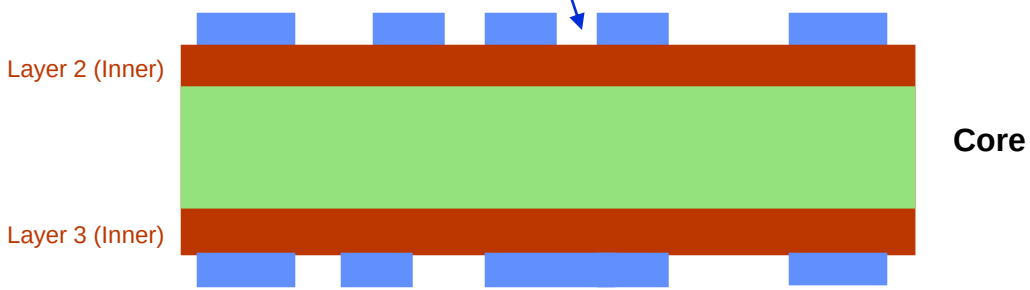


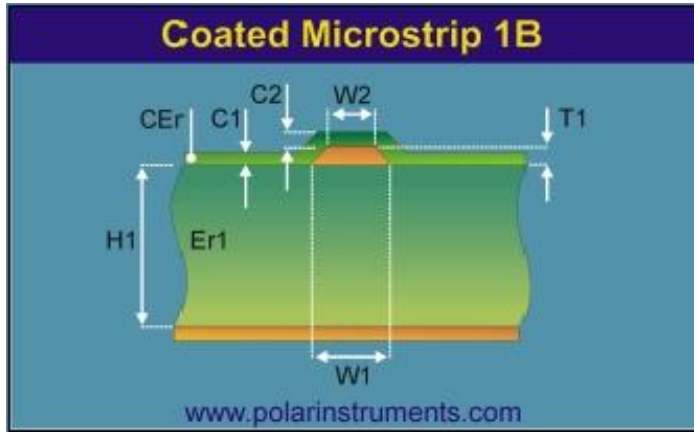
Impedance Considerations

- Selecting inner layer Core materials is very important when using embedded microstrip and offset stripline structures
- Inner layer Core materials are usually processed as “Layer pairs”

Laminating and Imaging of Internal Layers

UV sensitive film is laminated over top and bottom surfaces of the Core
Areas of the Core where no copper is required are left exposed

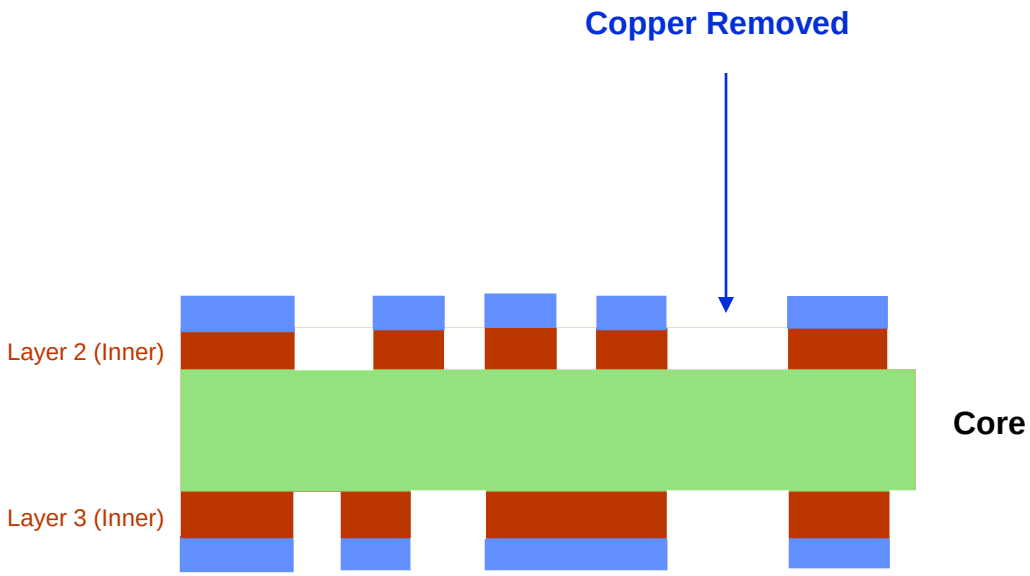


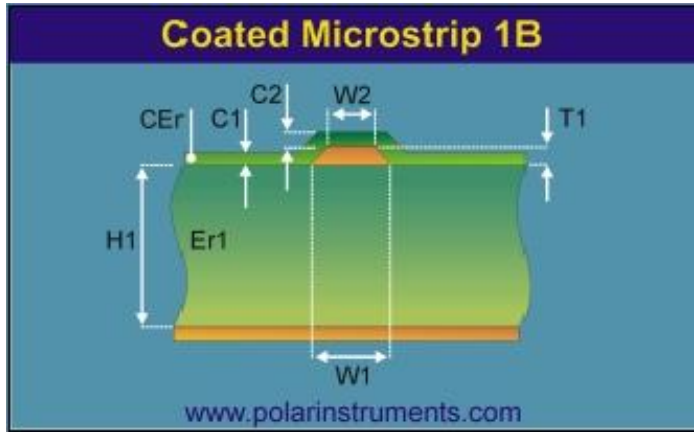


Impedance Considerations

- Does not effect impedance

Etch Process - Remove Exposed Copper

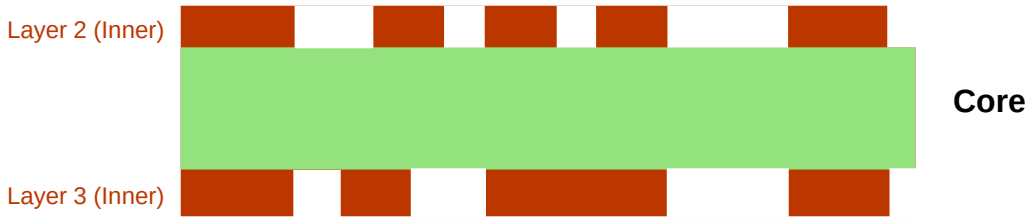


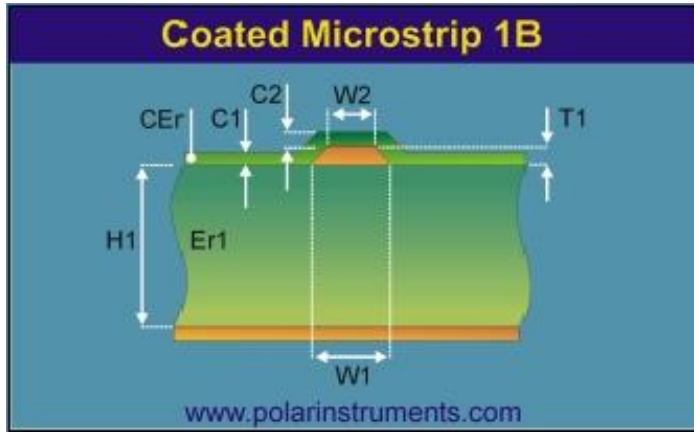


Impedance Considerations

- The etch process produces an ‘etch back’ or undercut of the tracks. This can be specified by the W_1 / W_2 parameters
- This means that tracks will end up approximately 0.025 mm (0.001”) thinner than the original design.

Remove Laminating Film





Impedance Considerations

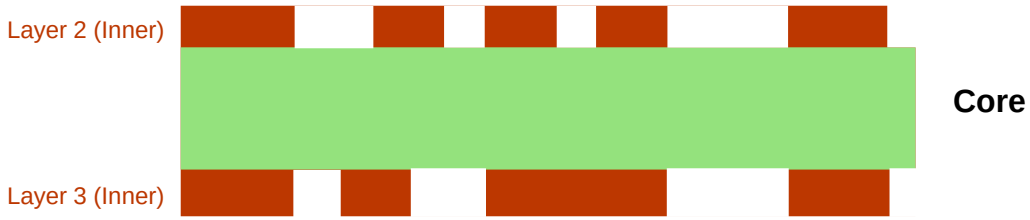
- Does not effect impedance

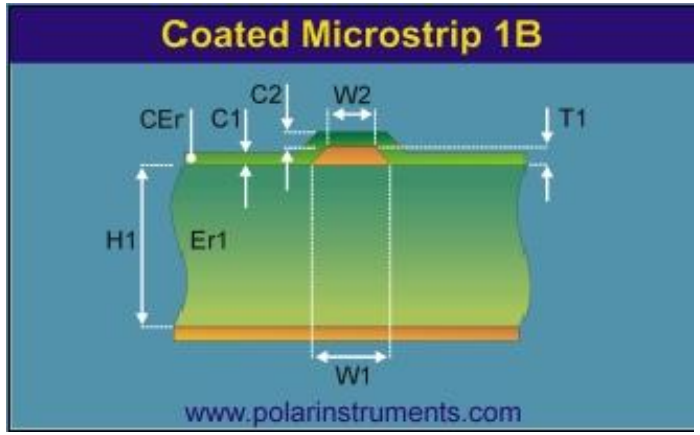
Completed Inner Layer Core

All inner layer Core materials are processed as "Layer Pairs" prior to Bonding

At this stage the Cores are inspected visually (AOI) and defective Cores rejected

Sometimes a surface treatment is applied to the Cores to aid with the Bonding process

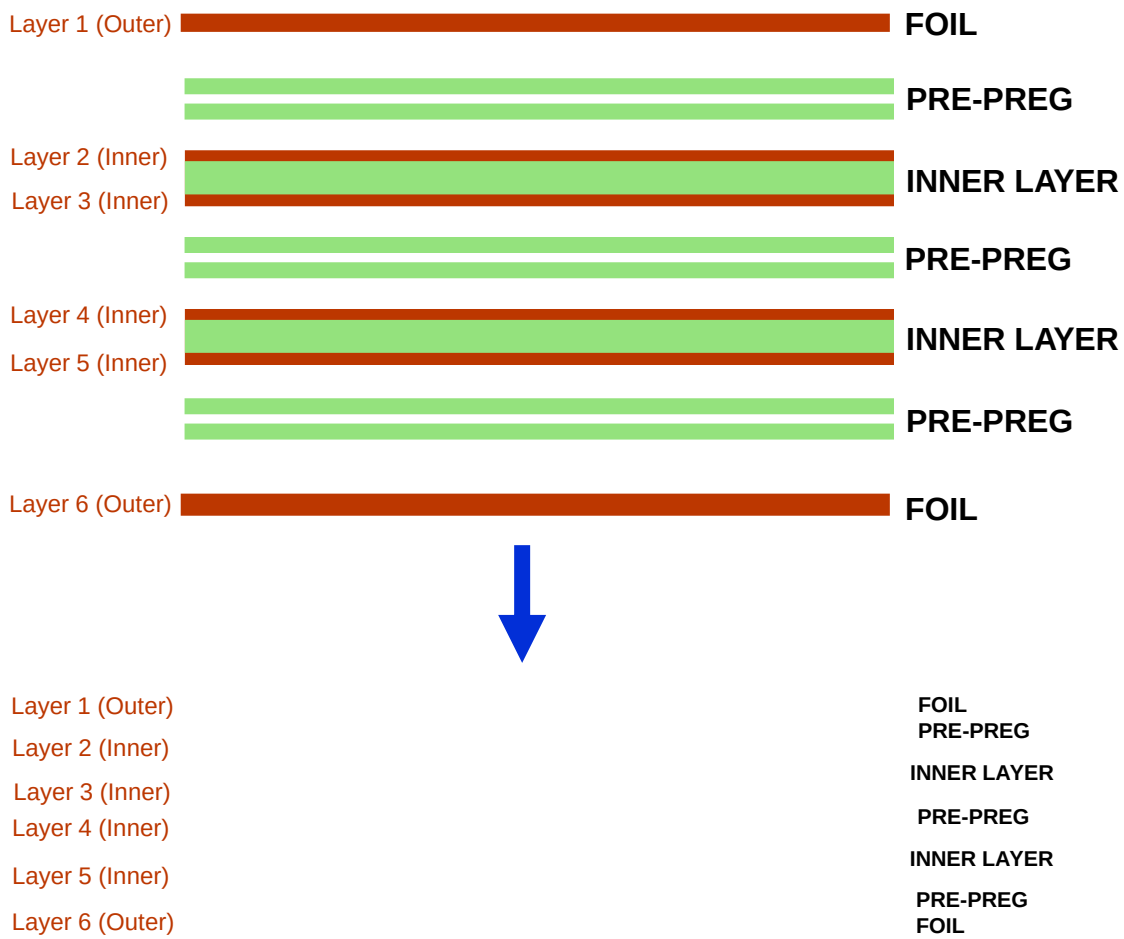


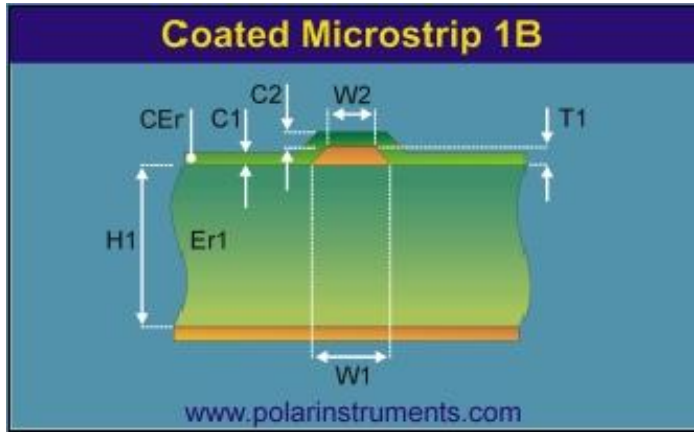


Impedance Considerations

- Does not effect impedance

Layer stackup

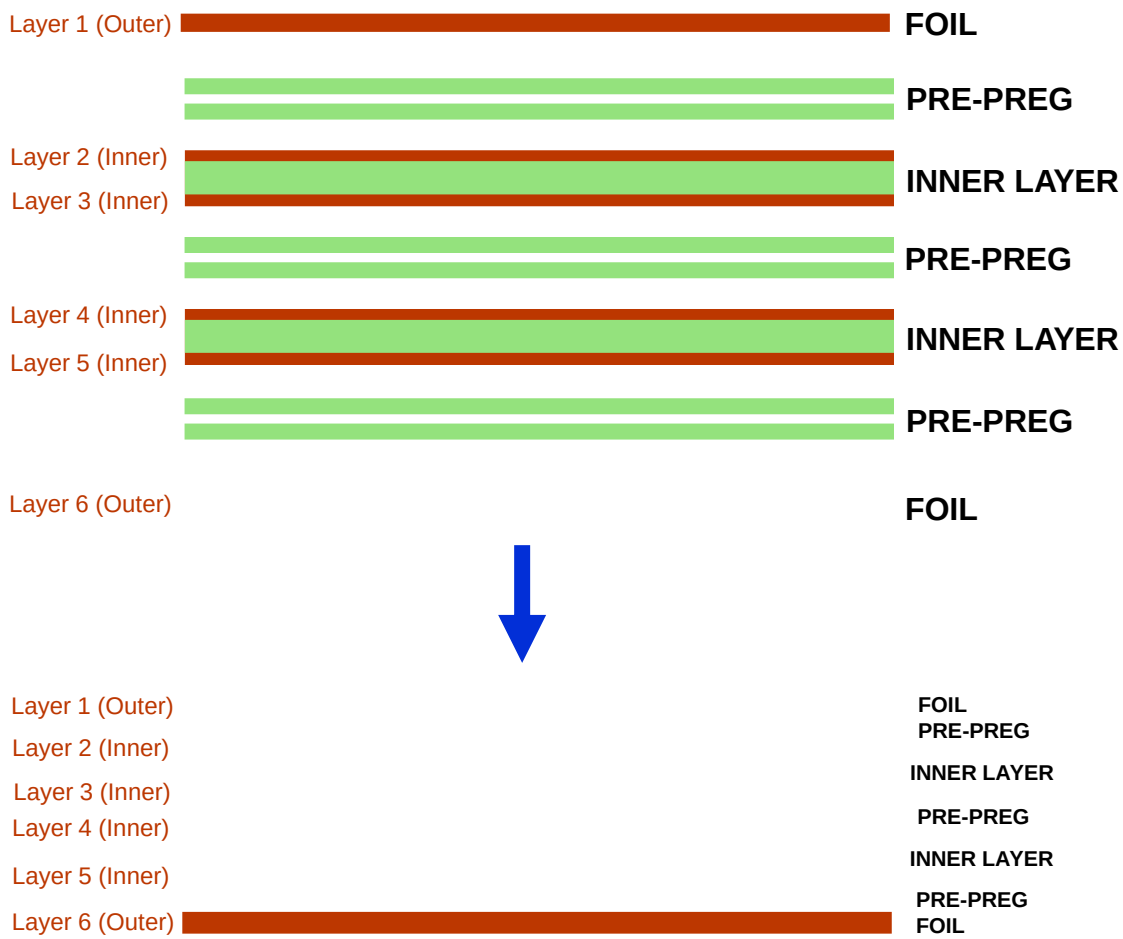


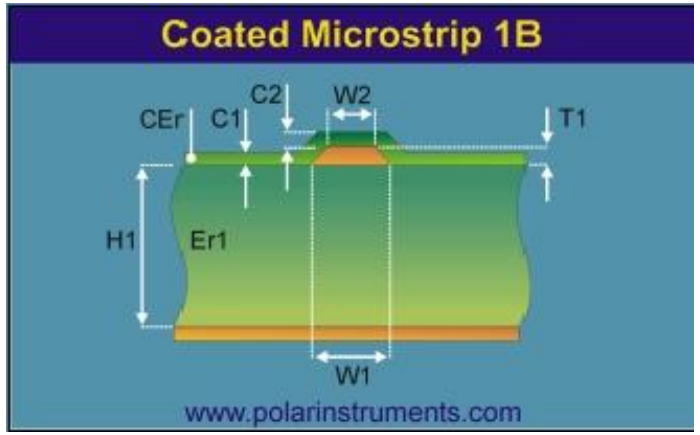


Impedance Considerations

- During the Bonding process press temperature and pressure have a great influence on substrate heights, which greatly affects impedance.
- It is important to use the Finished Post-Processed height when calculating Impedance

Layer stackup





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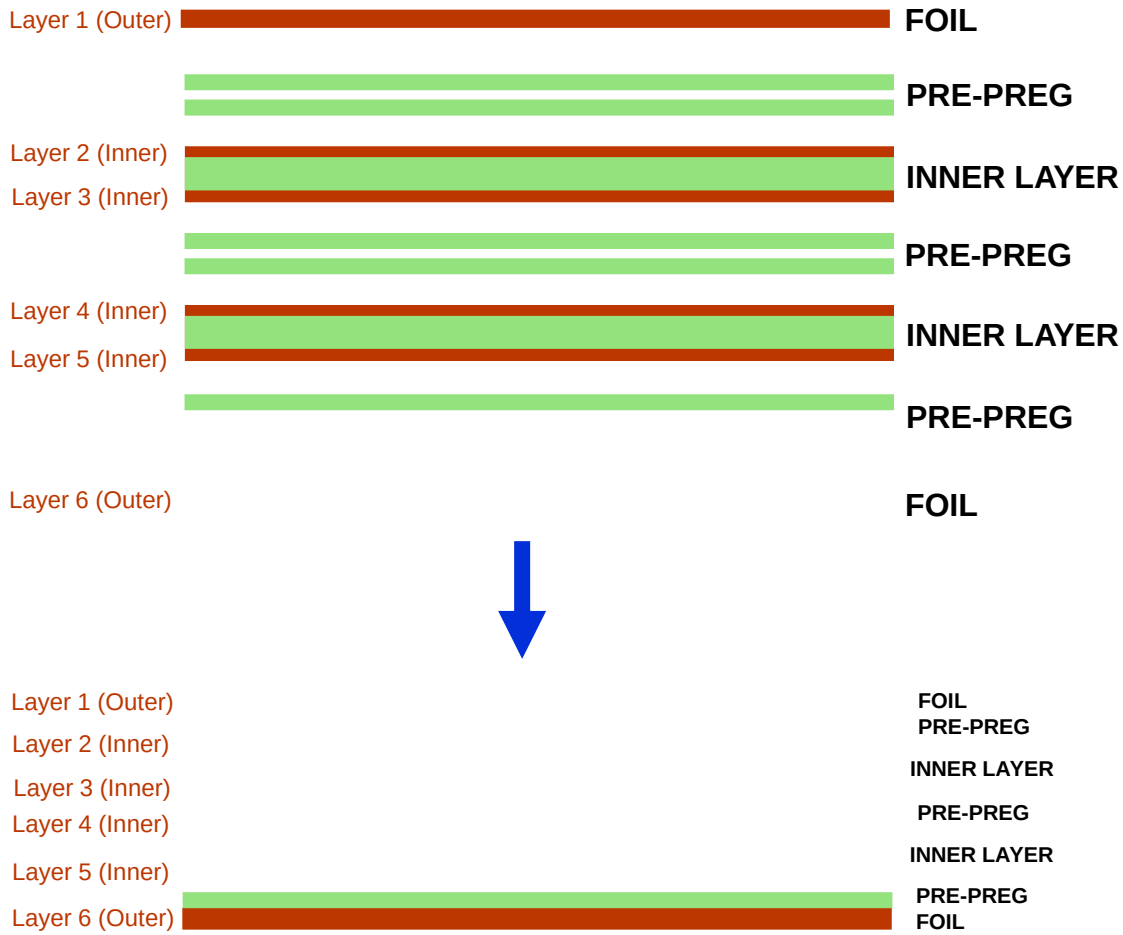

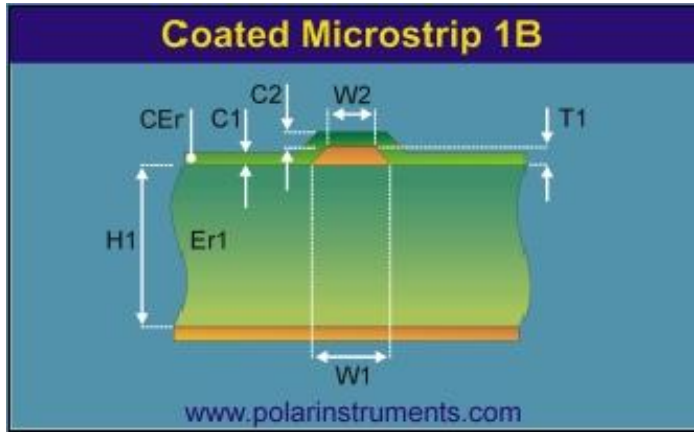

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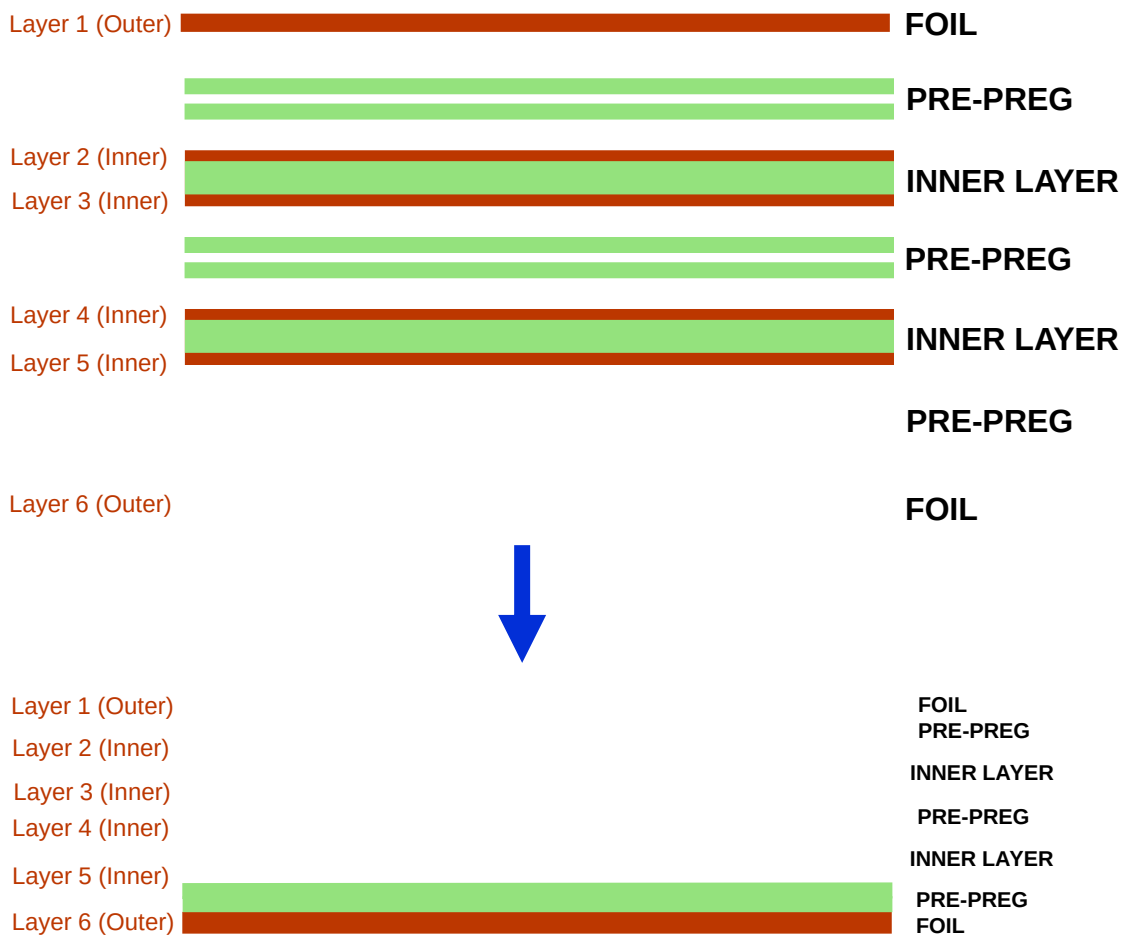

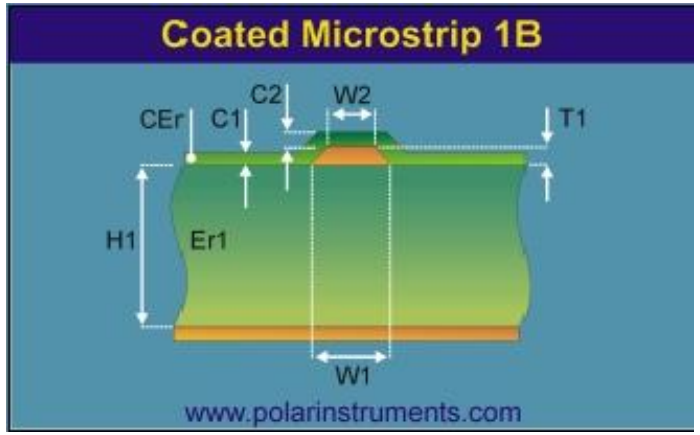

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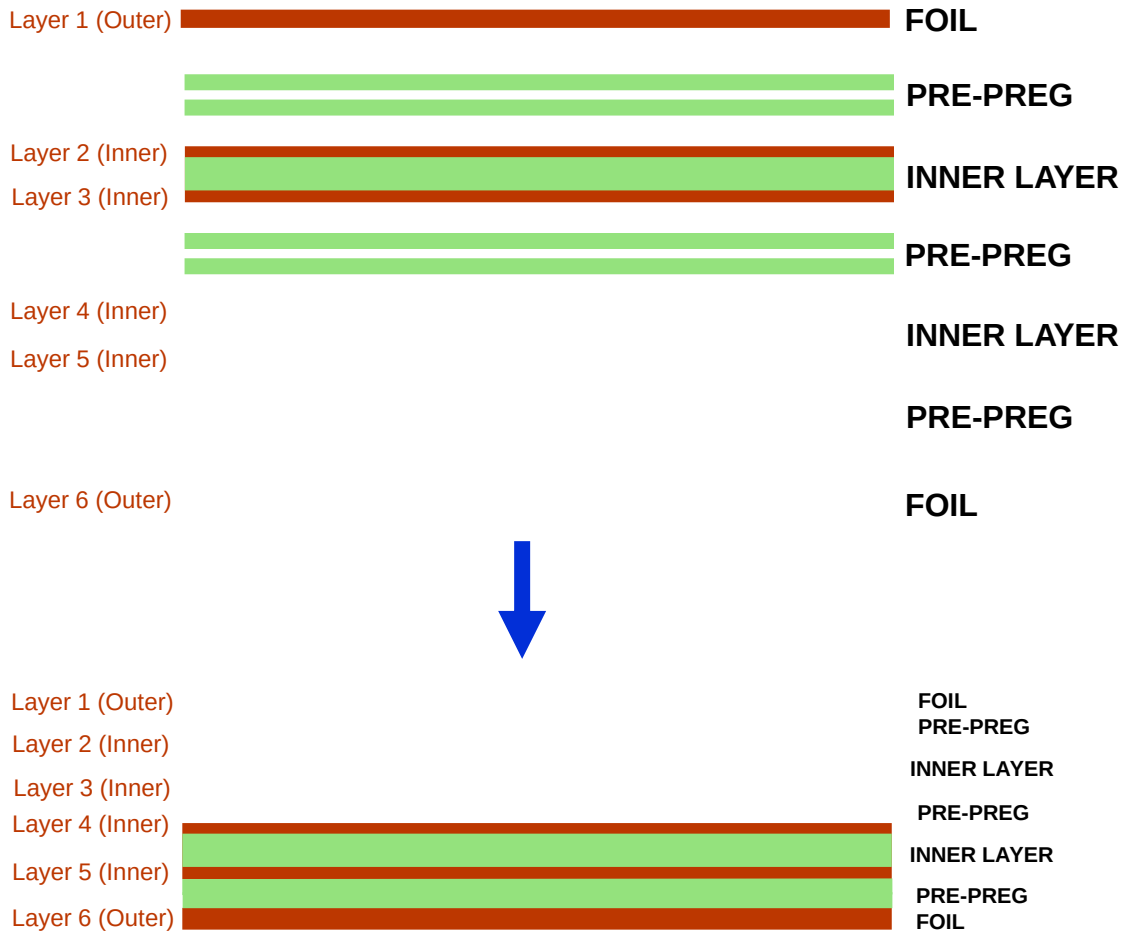

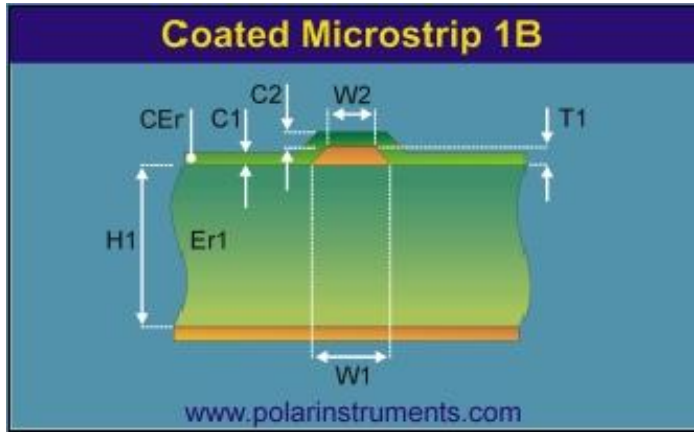

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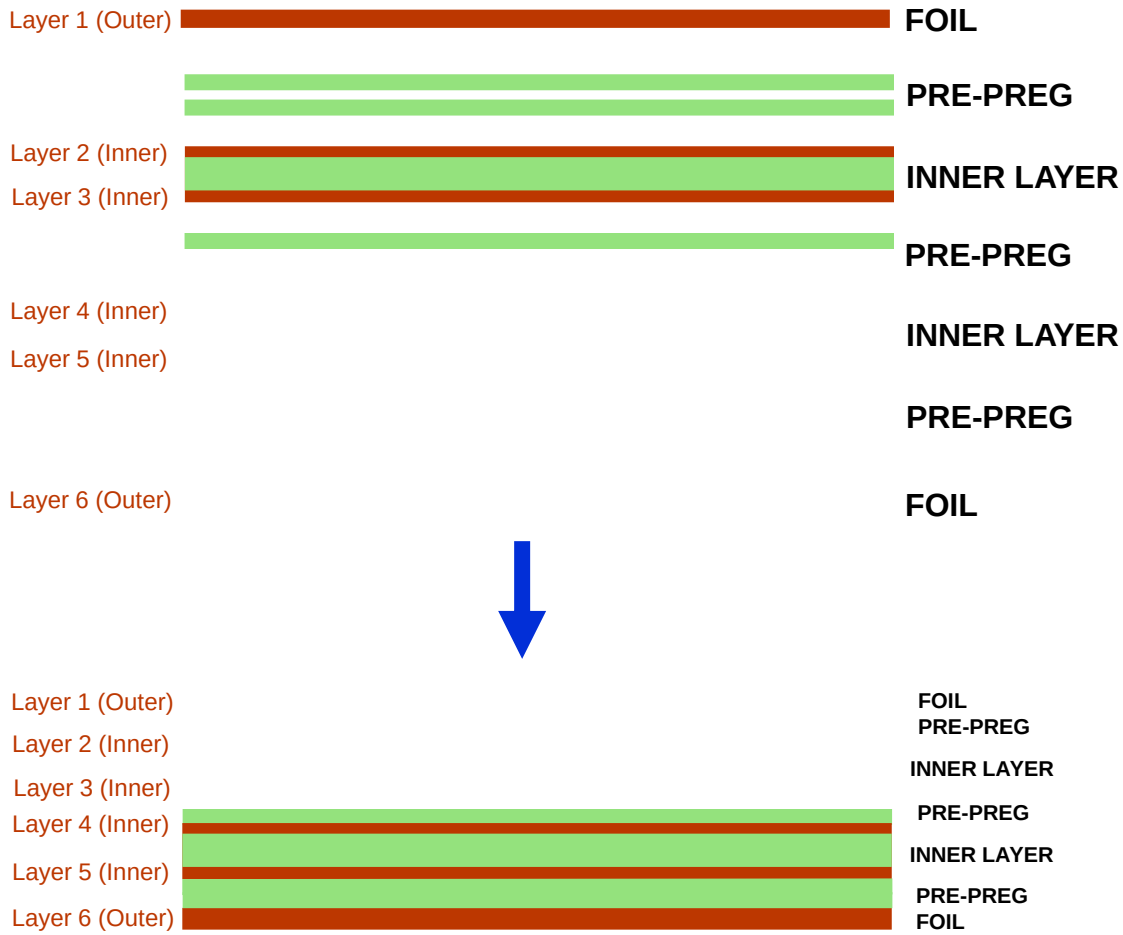

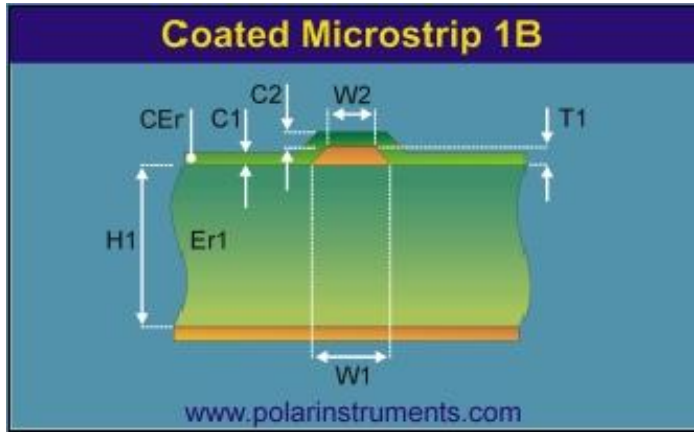

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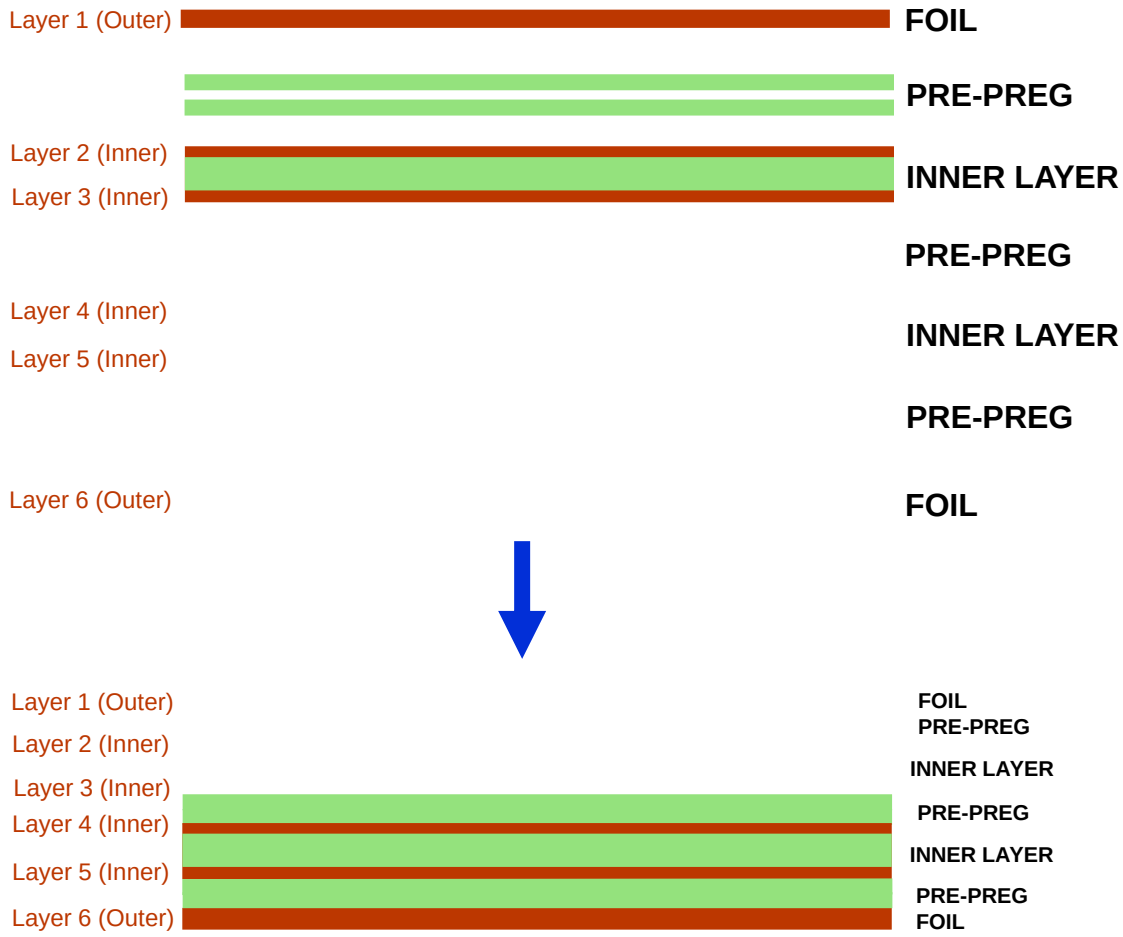

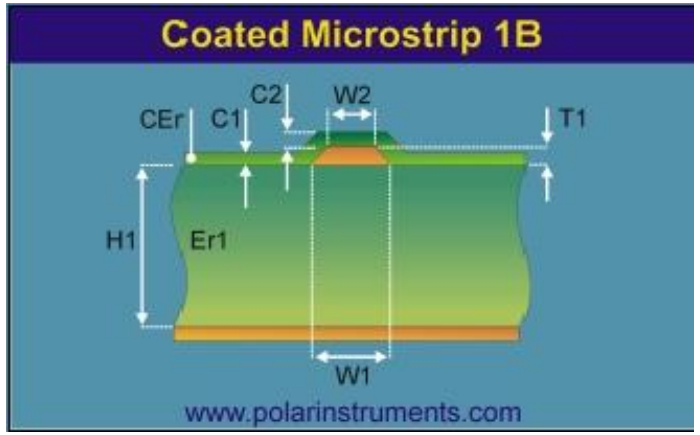

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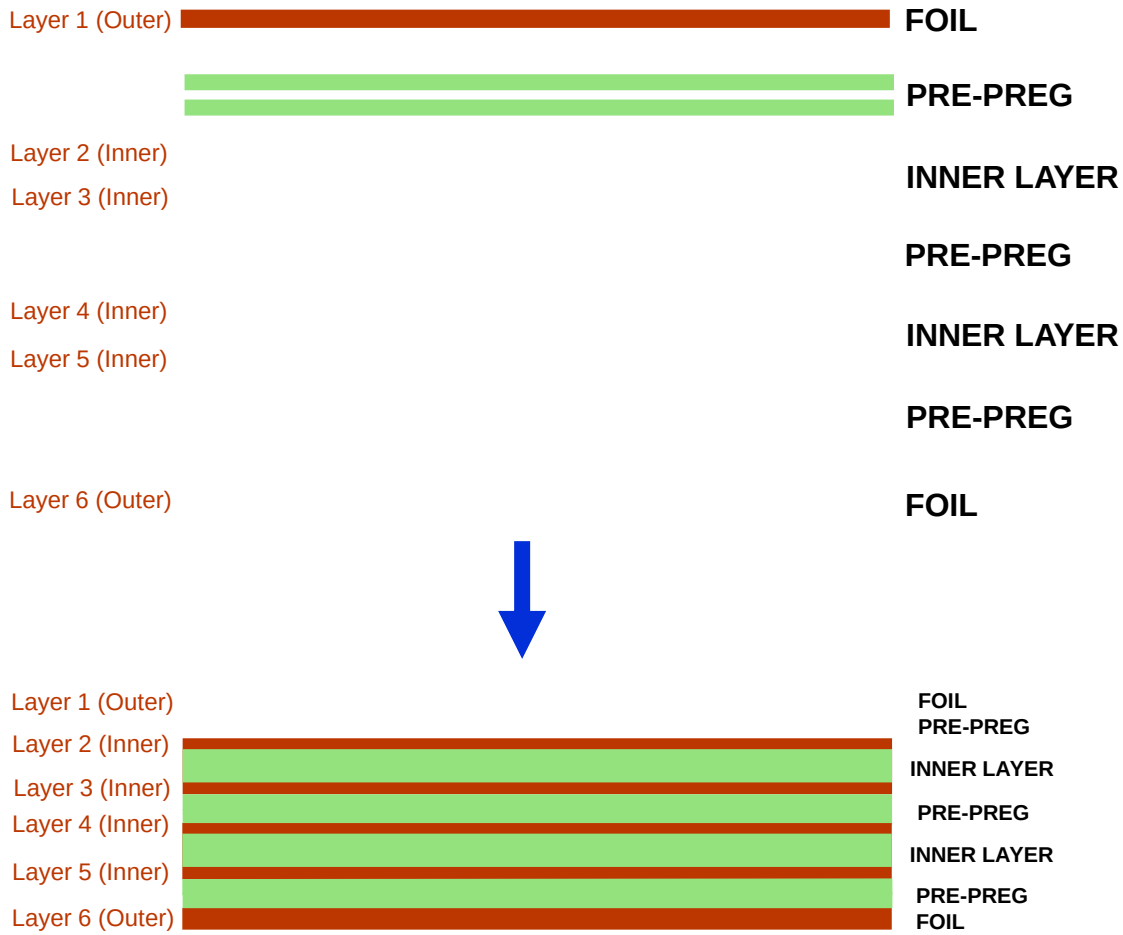

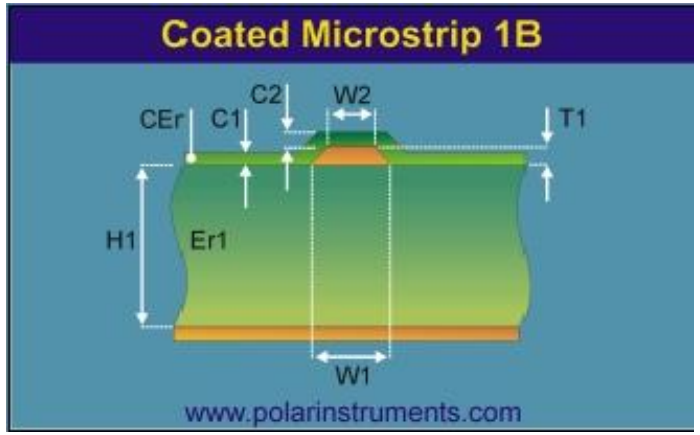

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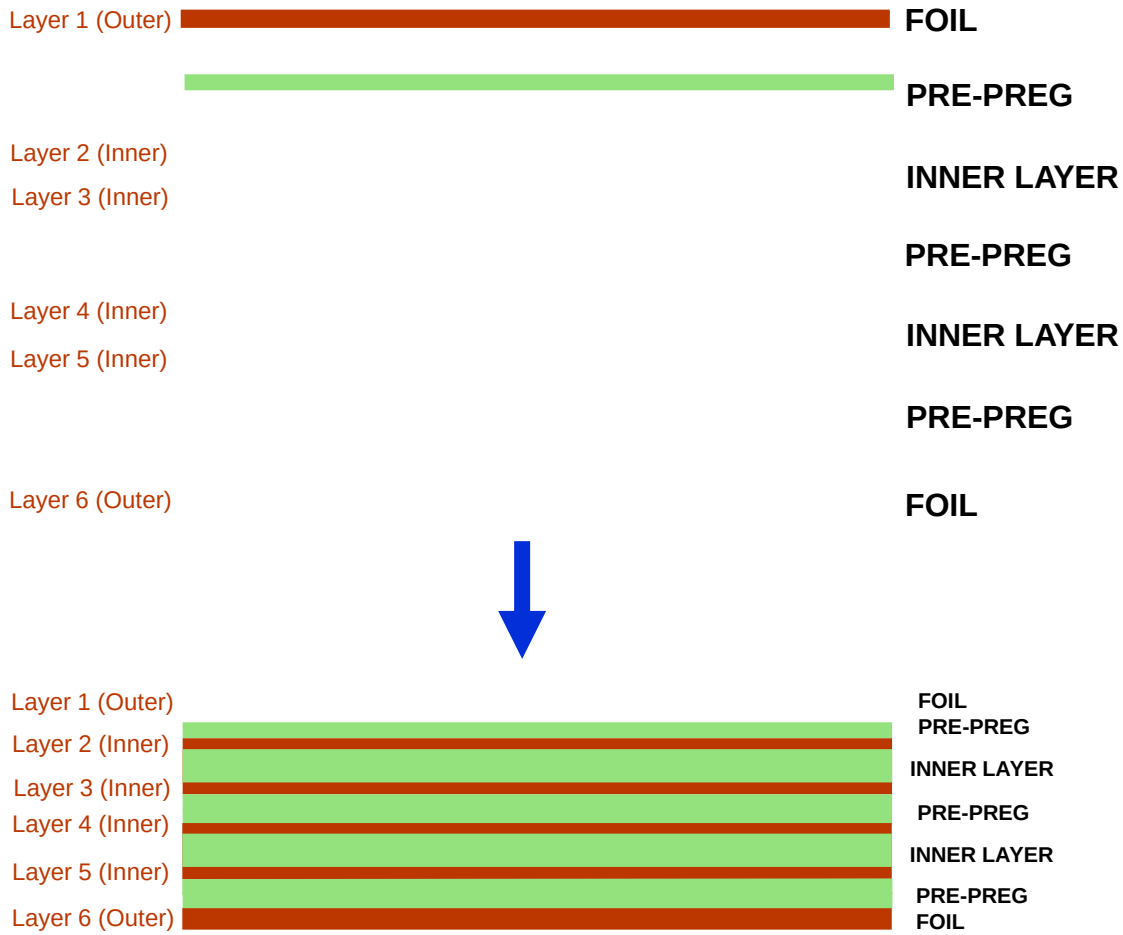

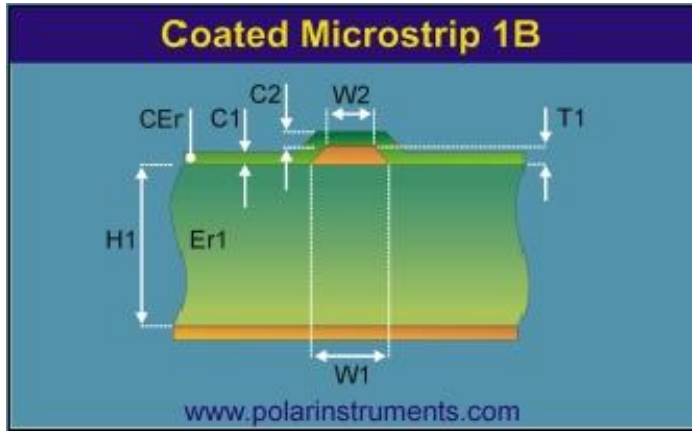

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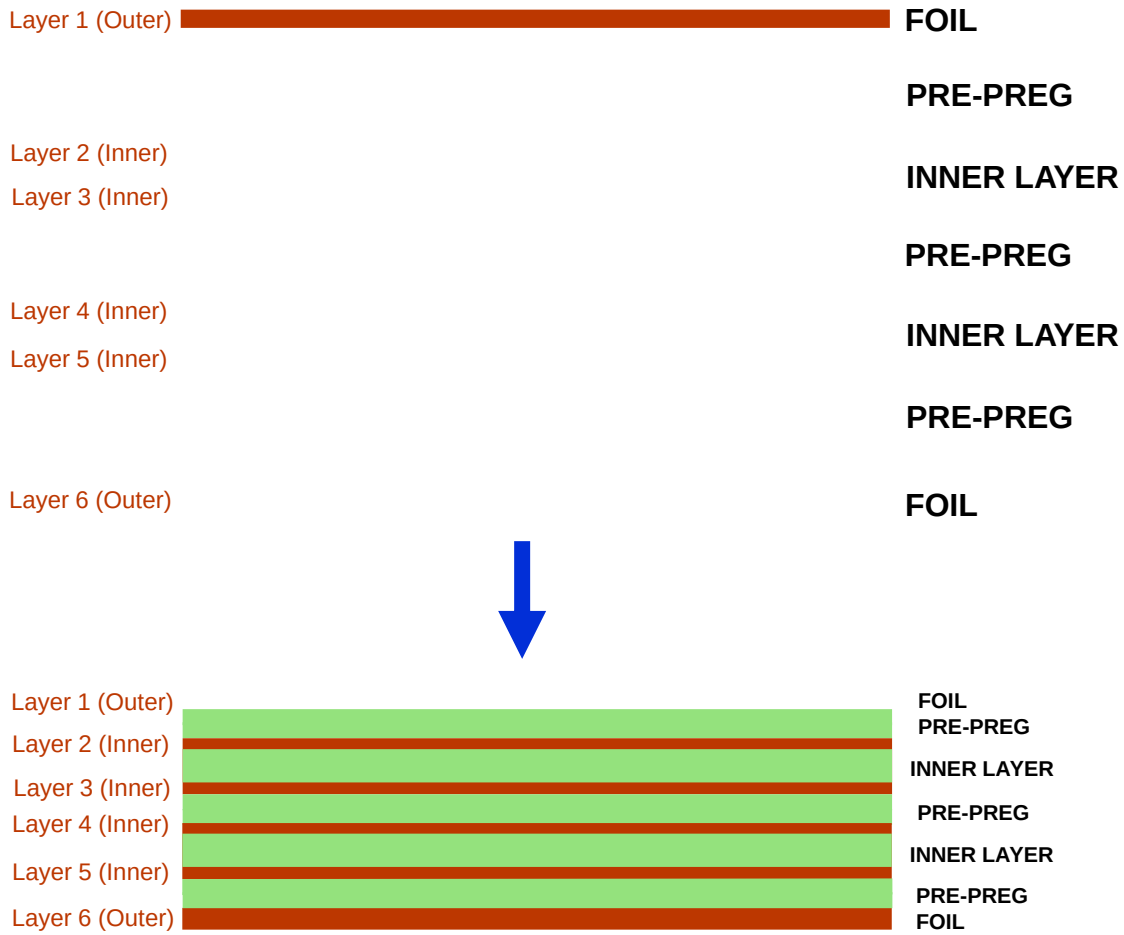

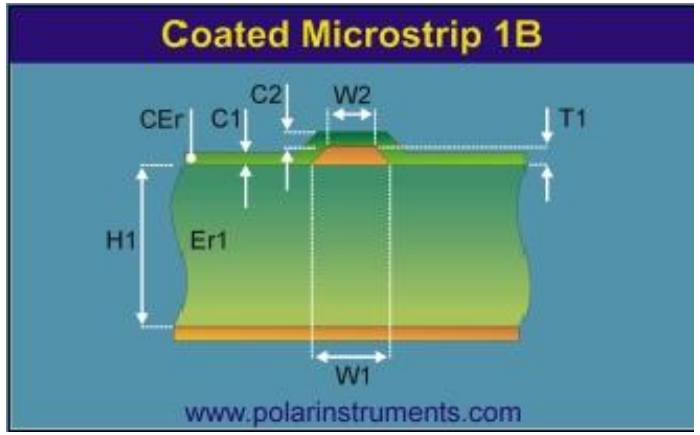

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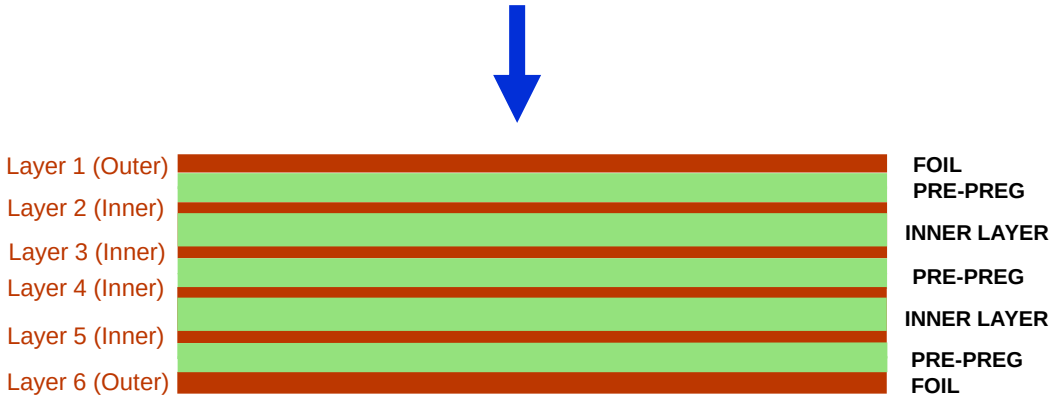
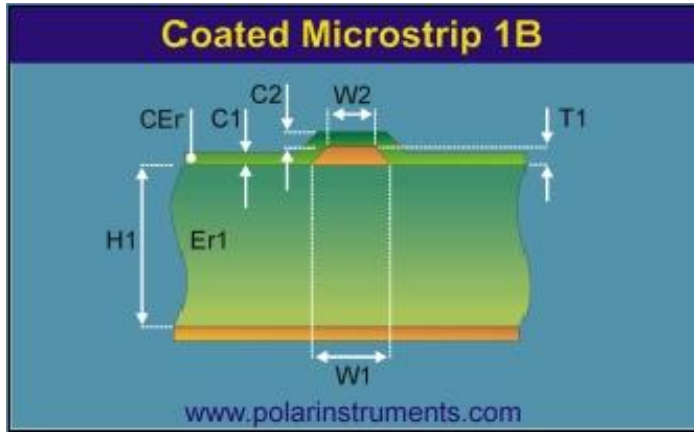
Layer stackup

Layer 1 (Outer)	FOIL
	PRE-PREG
Layer 2 (Inner)	INNER LAYER
Layer 3 (Inner)	
	PRE-PREG
Layer 4 (Inner)	INNER LAYER
Layer 5 (Inner)	
	PRE-PREG
Layer 6 (Outer)	FOIL



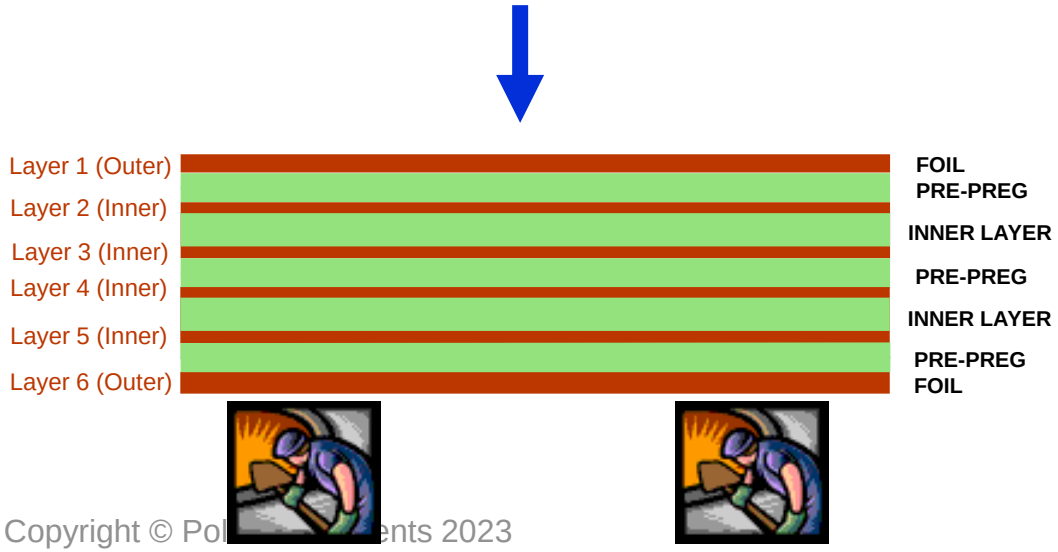


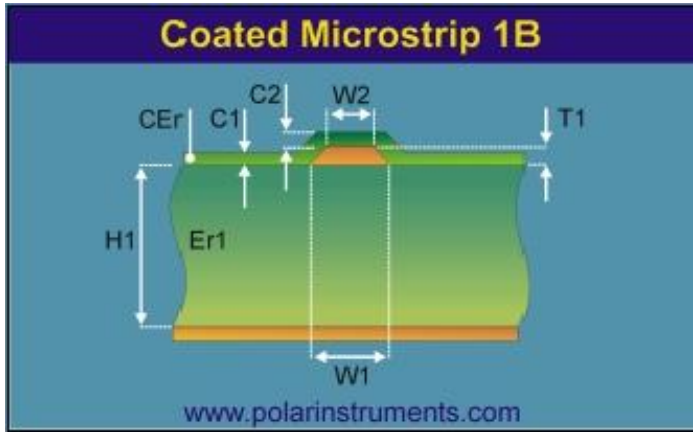
Impedance Considerations

- During the Bonding process, press temperature and pressure have a great influence on substrate heights, which greatly affects impedance.
- It is important to use the Finished Post-Processed height when calculating Impedance

Bonding – Heat

Layer 1 (Outer)	FOIL
	PRE-PREG
Layer 2 (Inner)	
Layer 3 (Inner)	INNER LAYER
	PRE-PREG
Layer 4 (Inner)	
Layer 5 (Inner)	INNER LAYER
	PRE-PREG
Layer 6 (Outer)	FOIL



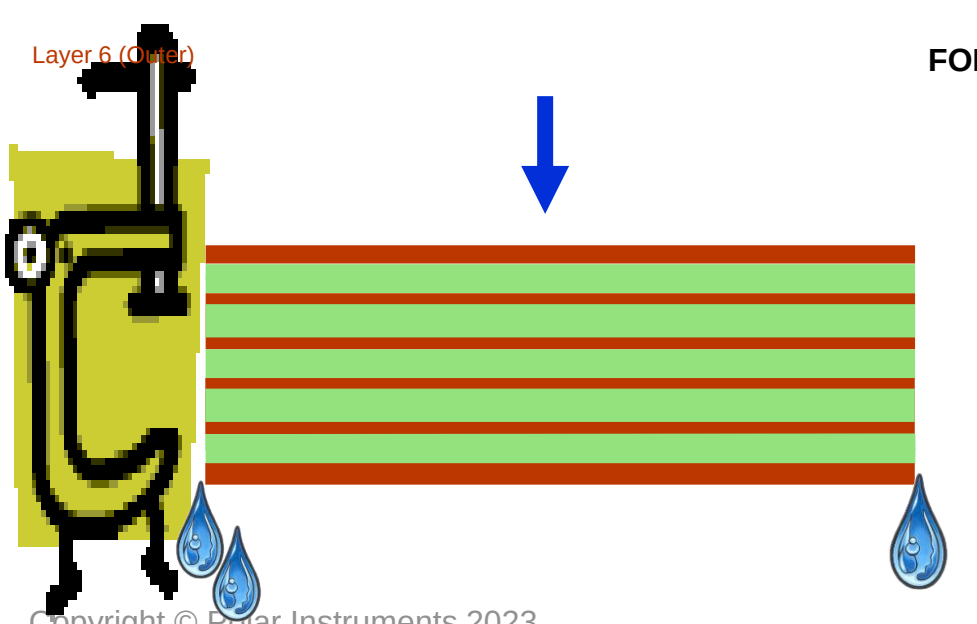


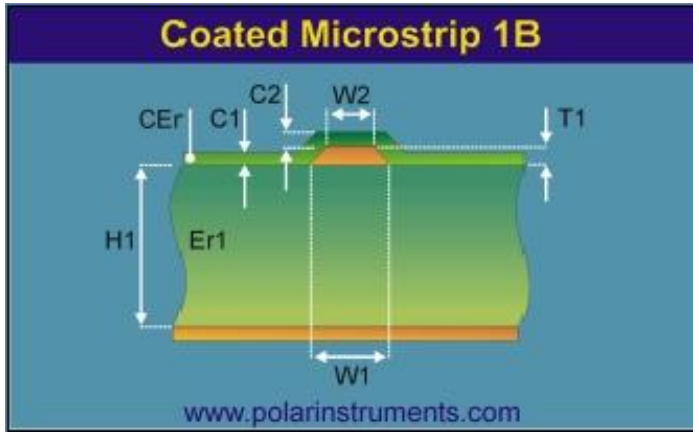
Impedance Considerations

- During the Bonding process, press temperature and pressure have a great influence on substrate heights, which greatly affects impedance.
- It is important to use the Finished Post-Processed height when calculating Impedance

Bonding – Multilayer Press

Layer 1 (Outer)	**FOIL**
	PRE-PREG
Layer 2 (Inner)	**INNER LAYER**
Layer 3 (Inner)	
	PRE-PREG
Layer 4 (Inner)	**INNER LAYER**
Layer 5 (Inner)	
	PRE-PREG
Layer 6 (Outer)	**FOIL**





Impedance Considerations

- During the Bonding process, press temperature and pressure have a great influence on substrate heights, which greatly affects impedance.
- It is important to use the Finished Post-Processed height when calculating Impedance

Bonding – Multilayer Press

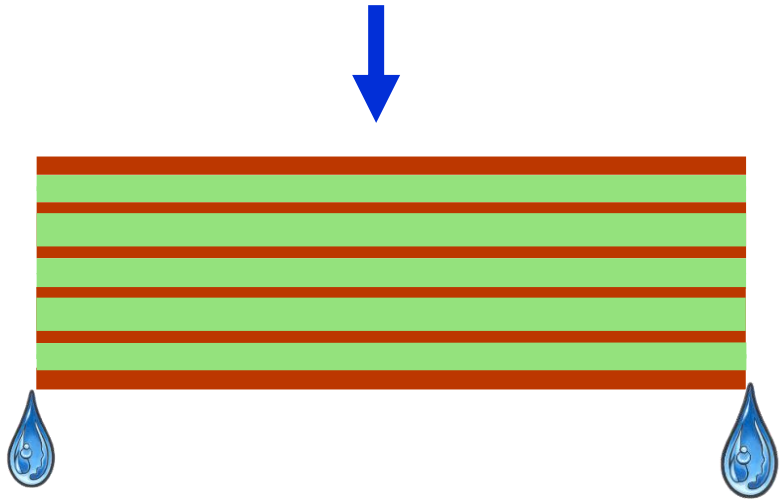
Layer 2 (Inner)

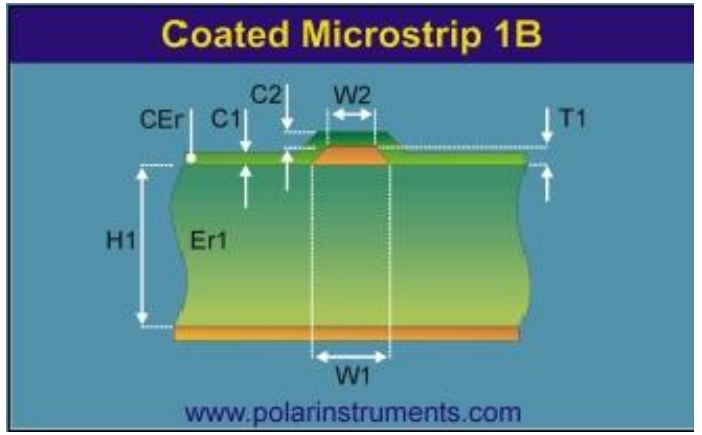
Layer 3 (Inner)

Layer 4 (Inner)

Layer 5 (Inner)

Layer 6 (Outer)





Impedance Considerations

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- It is important to use the Finished Post-Processed height when calculating Impedance

Bonding – Multilayer Press

Photo
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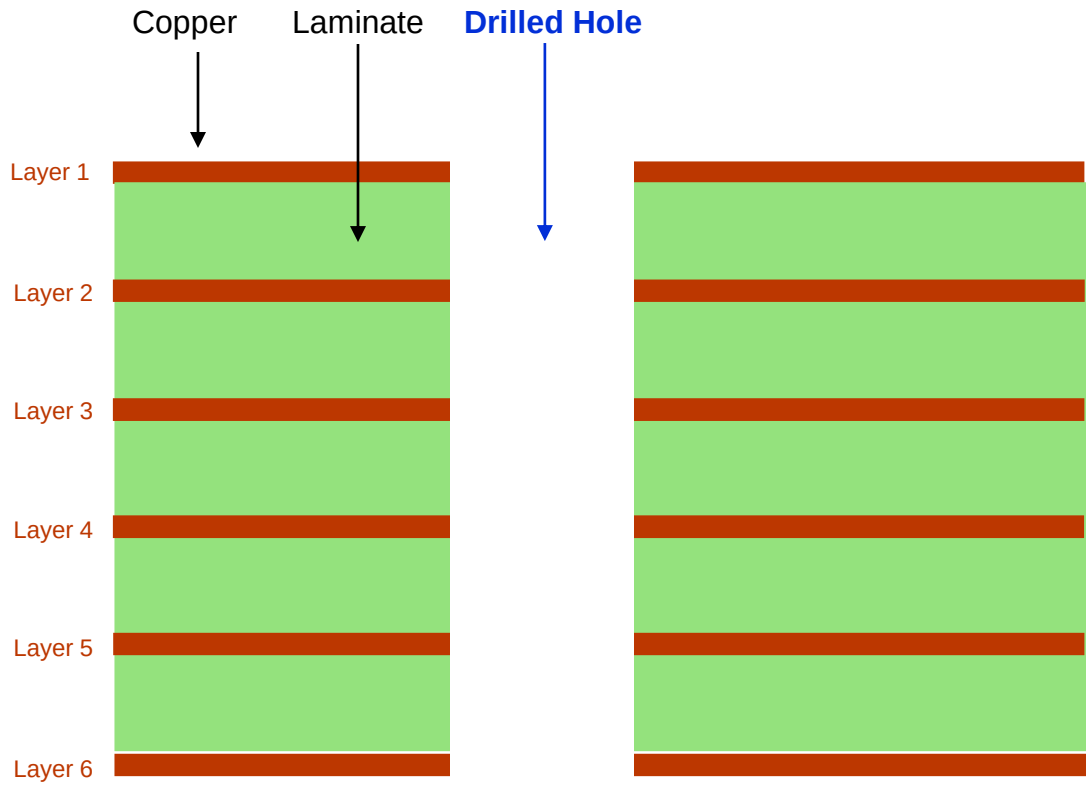
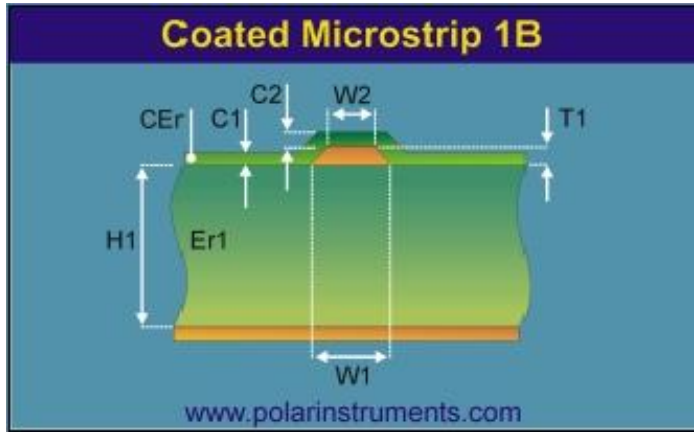
Drilling of Bonded Panel

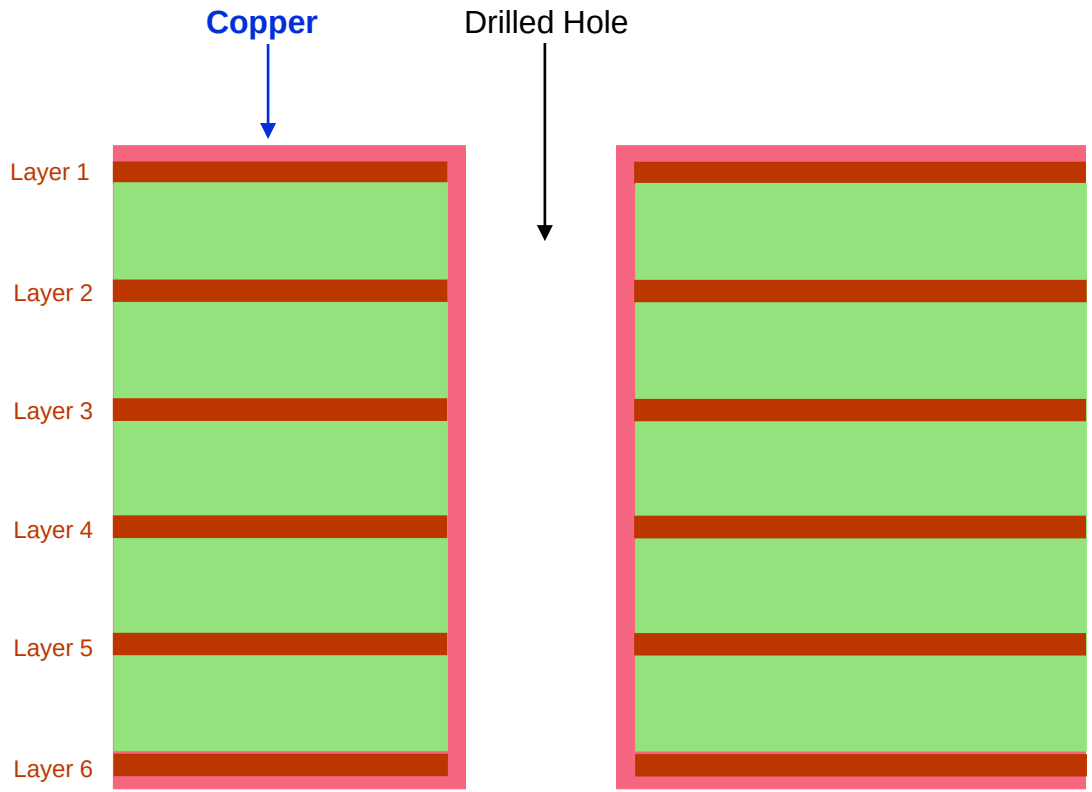


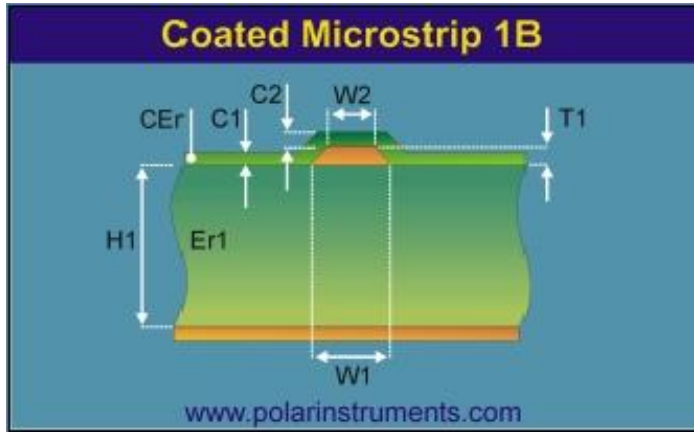


Impedance Considerations

- Drilling itself does not effect impedance

Electroless Copper Process
Addition of Copper to all Exposed Surfaces

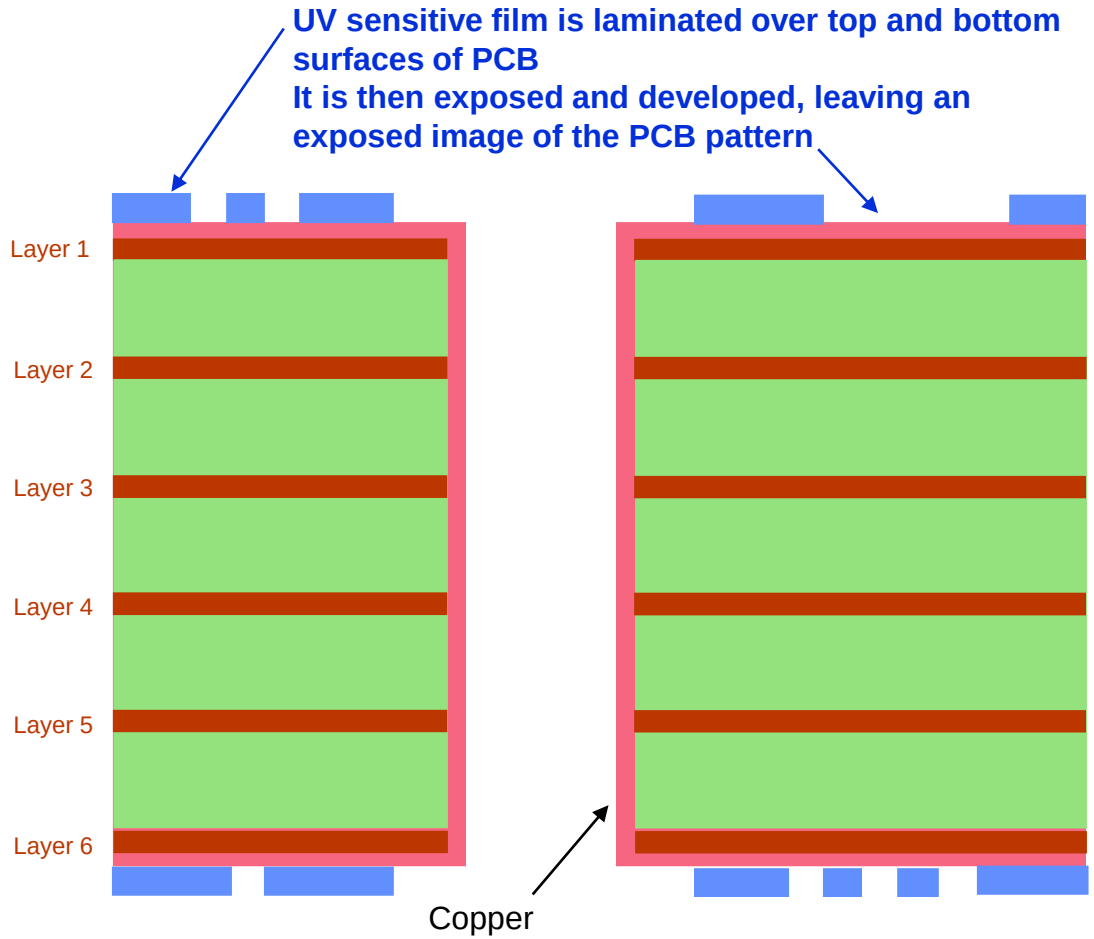


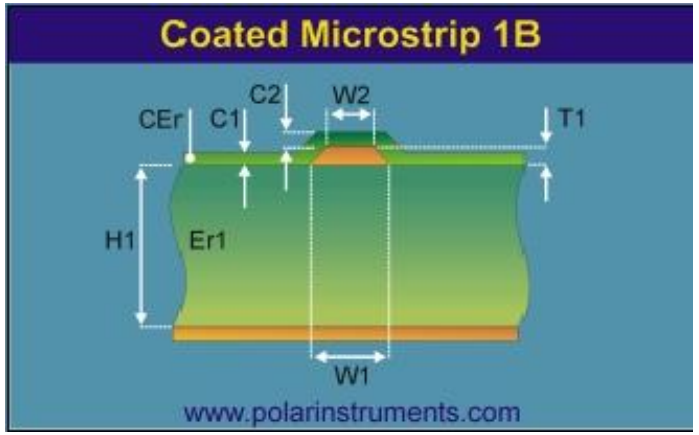


Impedance Considerations

- Electroless copper effects copper thickness on outer layers (T_1)
- Sometimes other solutions are used containing carbon, etc.

Laminating and Imaging of External Layers

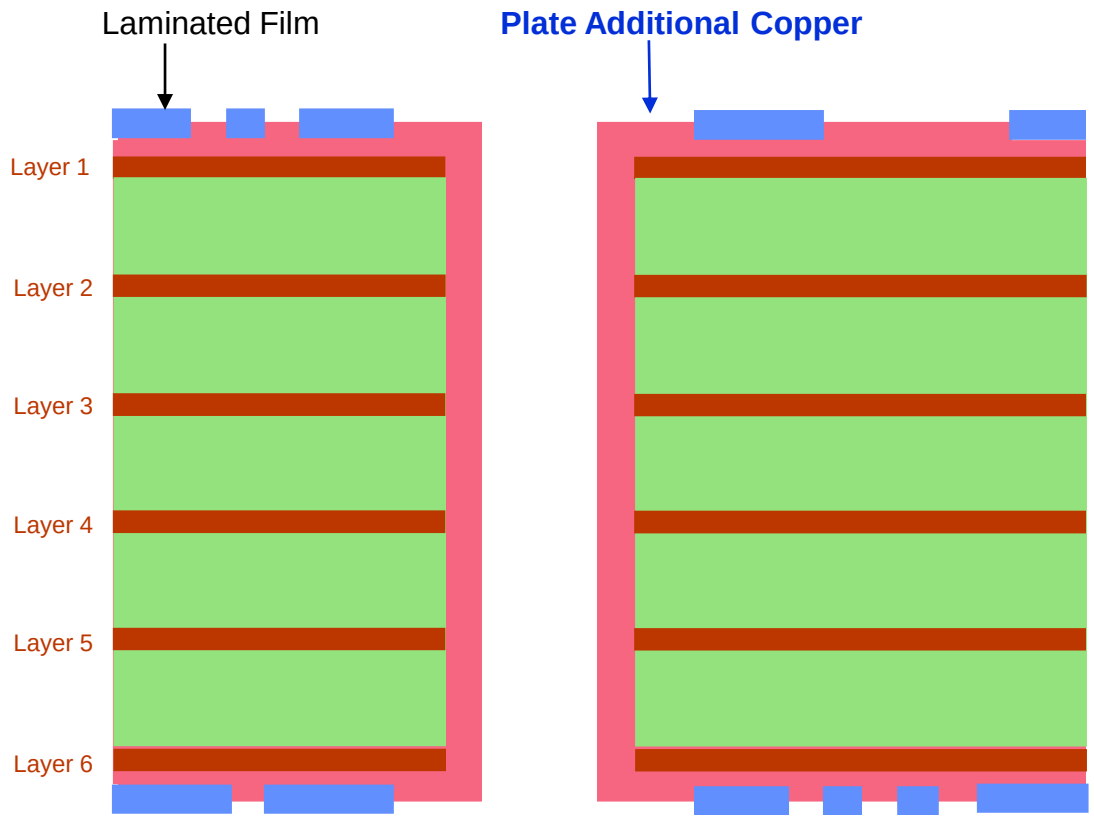


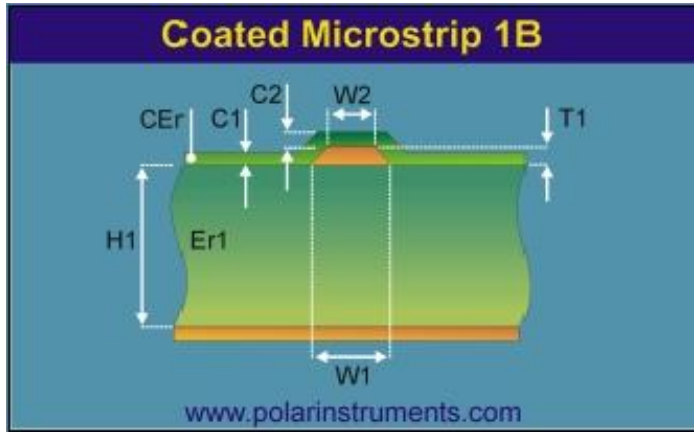


Impedance Considerations

- Does not effect impedance

Electro-plating Process 1
Additional Copper to all Exposed Surfaces

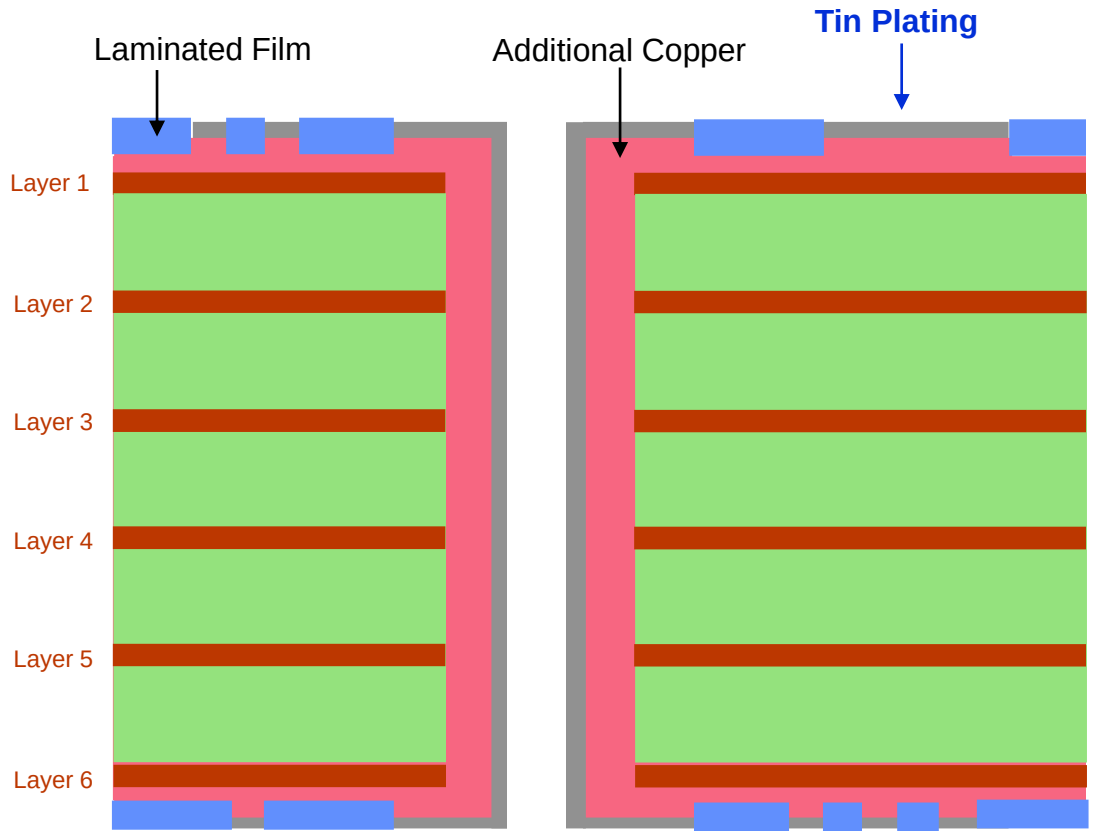


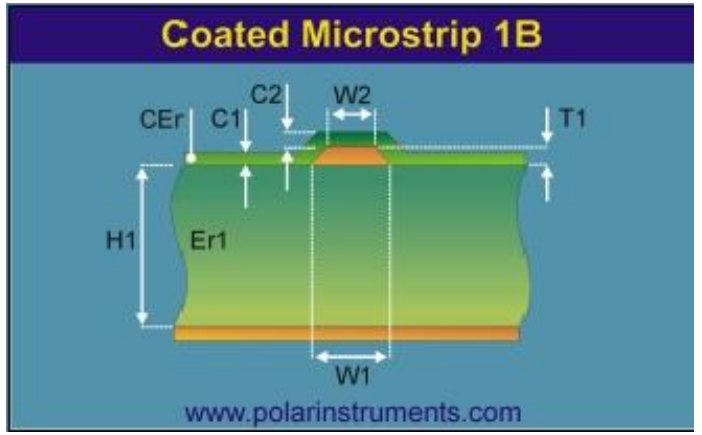


Impedance Considerations

- Electro-plating increases the copper thickness on outer layers (T_1)
- There will always be variations in the amount of copper added.
- This finished copper thickness should be used in structure calculations

Electro-plating Process 2
Add Tin over Exposed Copper Areas

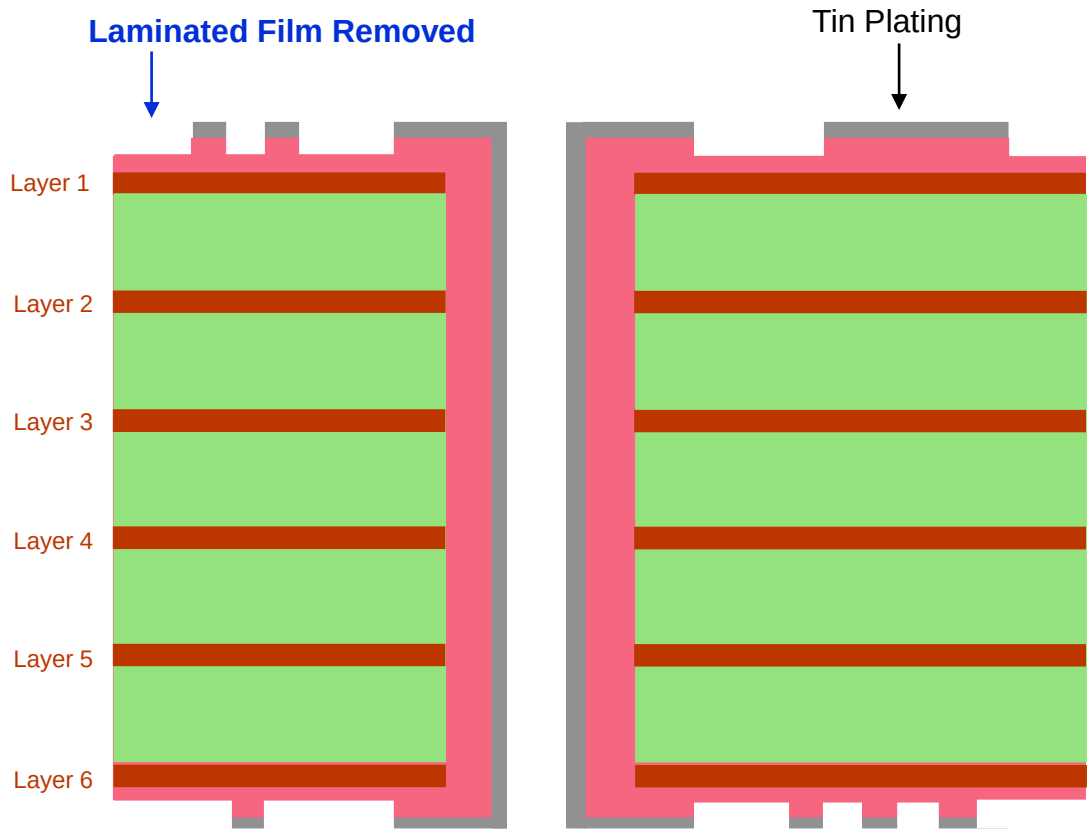


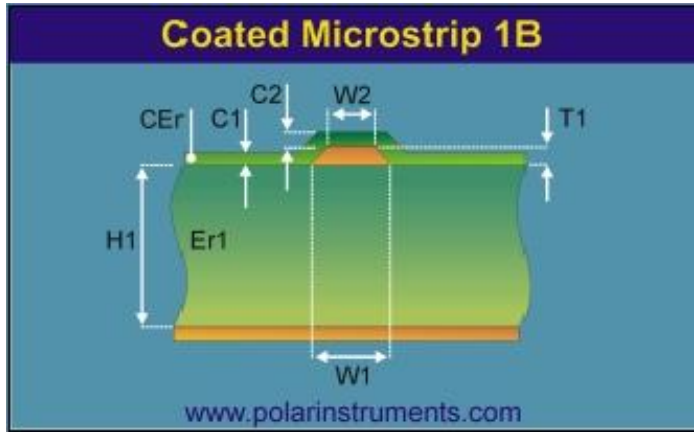


Impedance Considerations

- Does not effect impedance

Electro-plating Process 3
Remove Laminated Film

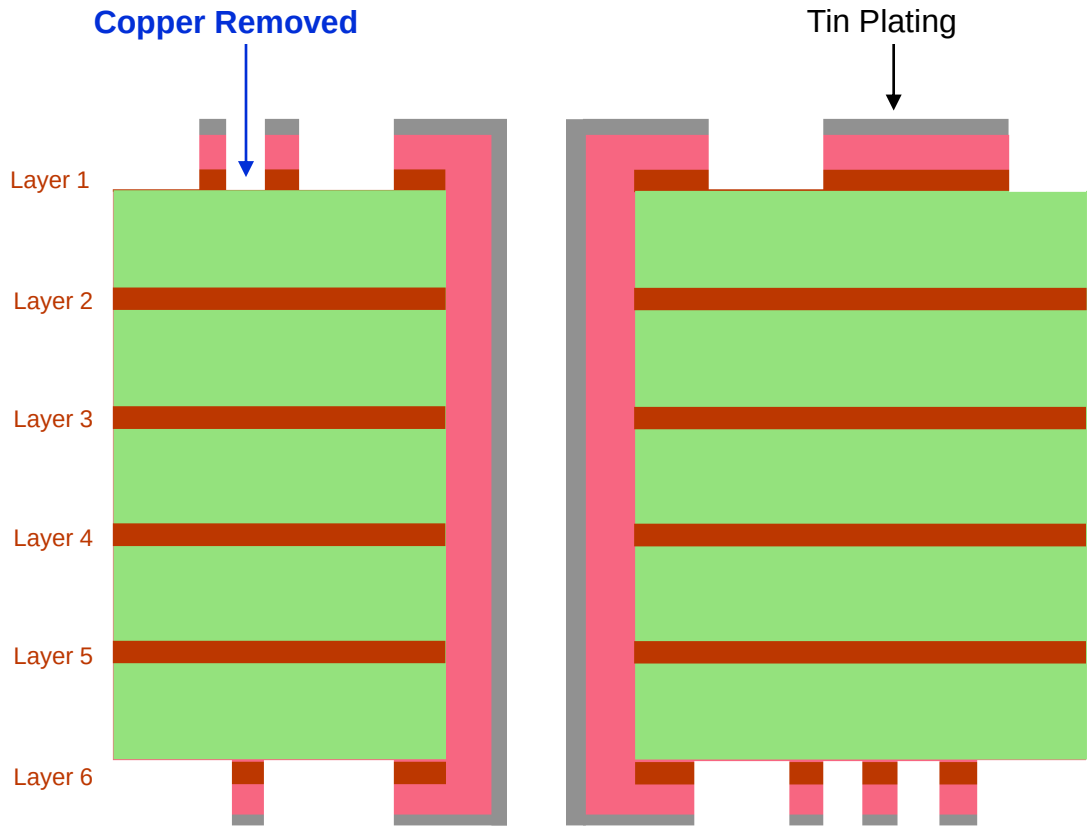


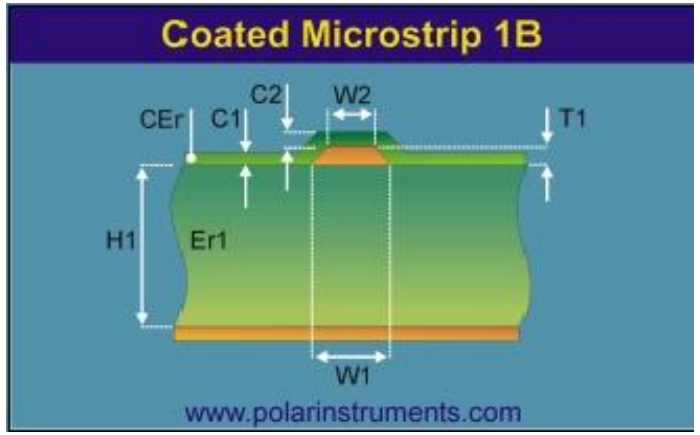


Impedance Considerations

- Does not effect impedance

Etch Process - Remove Exposed Copper

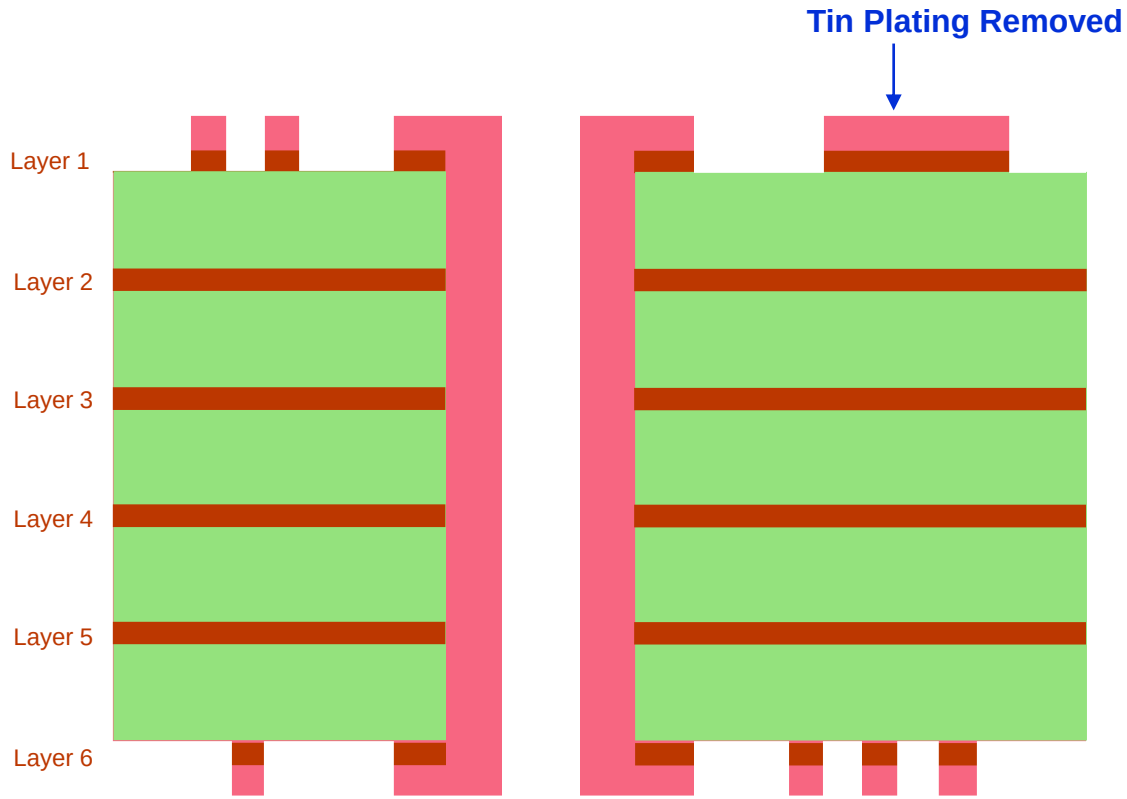


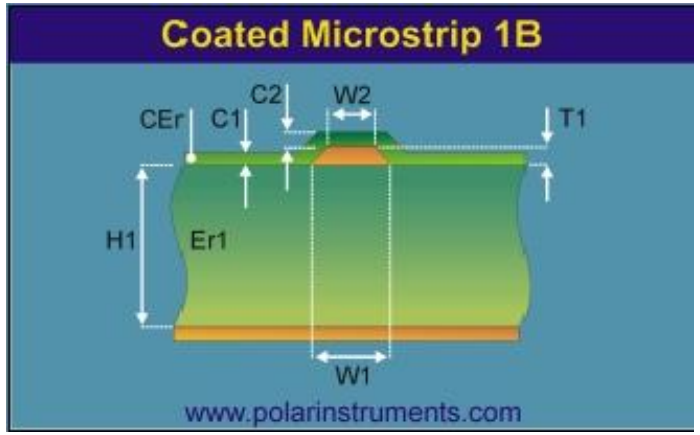


Impedance Considerations

- The etch process produces an ‘etch back’ or undercut of the tracks. This can be specified by the W_1 / W_2 parameters
- This means that tracks will end up approximately 0.025 mm (0.001”) thinner than the original design.

Tin Strip - Remove Tin Plating

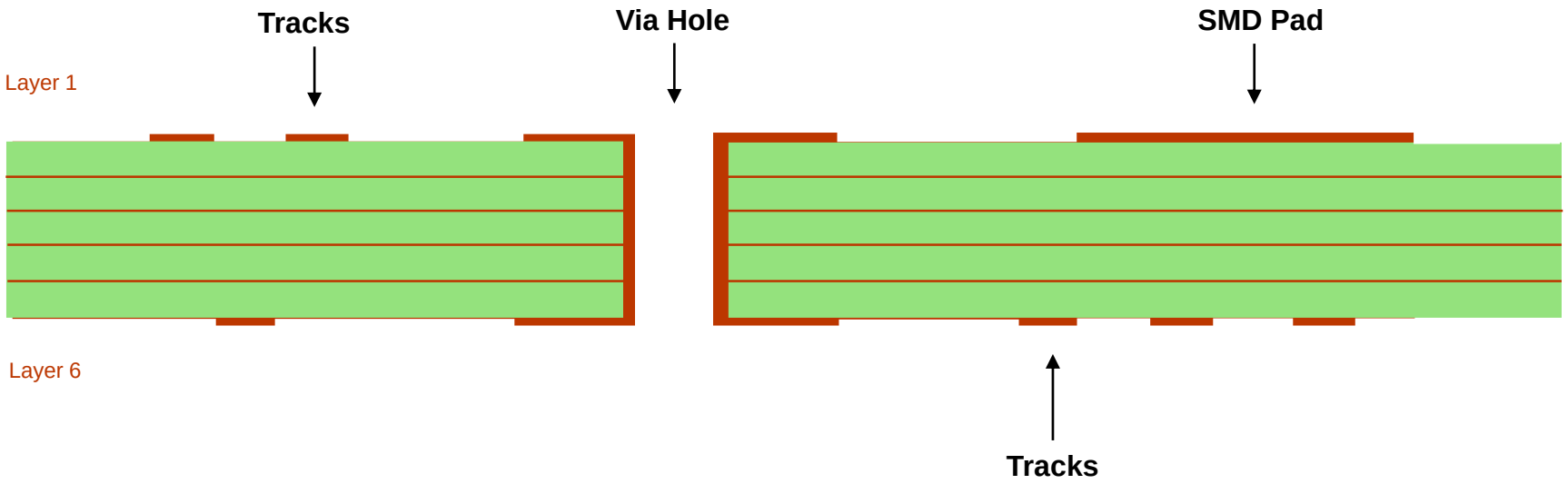




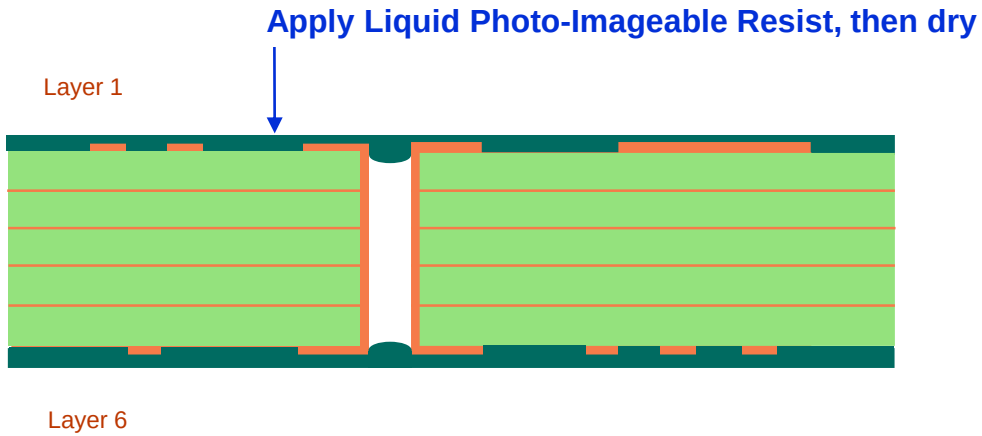
Impedance Considerations

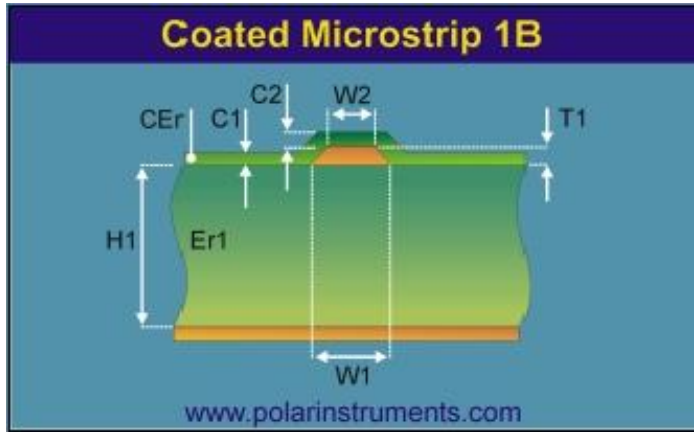
- The removal of tin will slightly reduce the copper thickness (T_1) on the outer layers

PCB is now complete except for surface finishes and panel routing



Solder Mask Application
- Curtain Coated Method

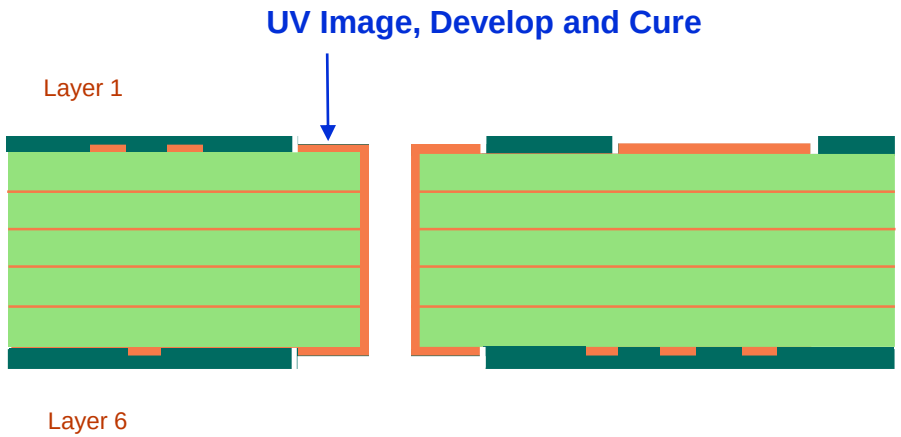


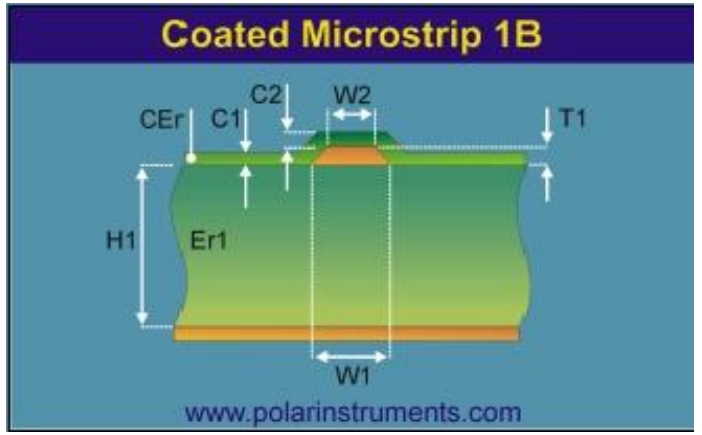


Impedance Considerations

- Some PCB fabricators chose to check the impedance before the solder mask is added
- Structures can be checked in Normal and Coated mode
- Thickness of solder mask should be specified using C_1 and C_2

Solder Mask Application
Image, Develop and Cure

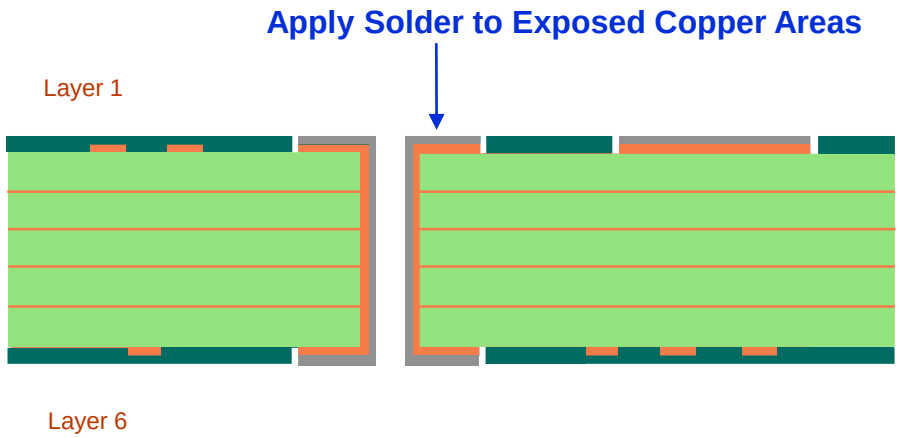


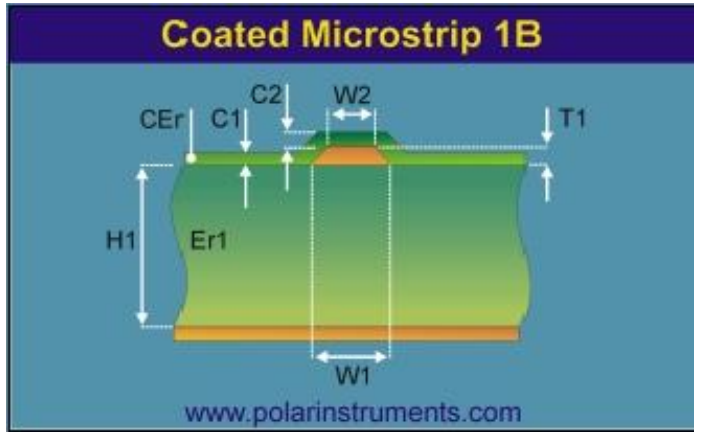


Impedance Considerations

- Does not effect impedance

Surface Finish Process

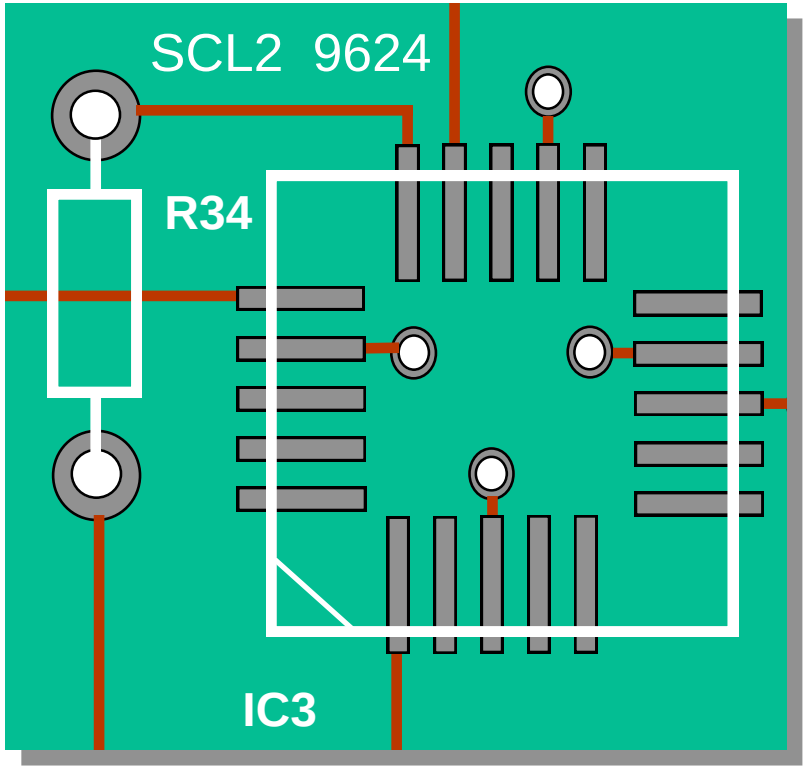


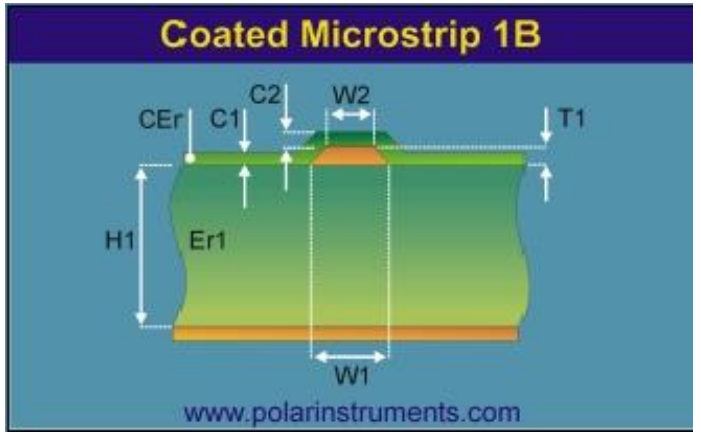


Impedance Considerations

- Surface Finish (Tin / Lead / Gold / Silver) is usually only added to pads
- If board has no solder mask the thickness of finish should be added to T_1.

Component Notation

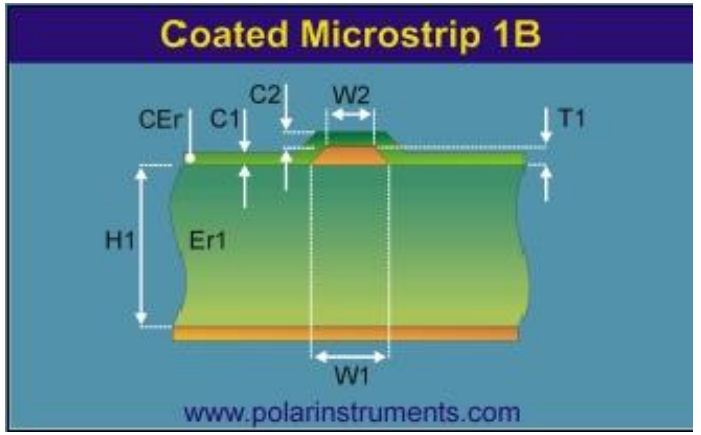




Impedance Considerations

- Does not effect impedance

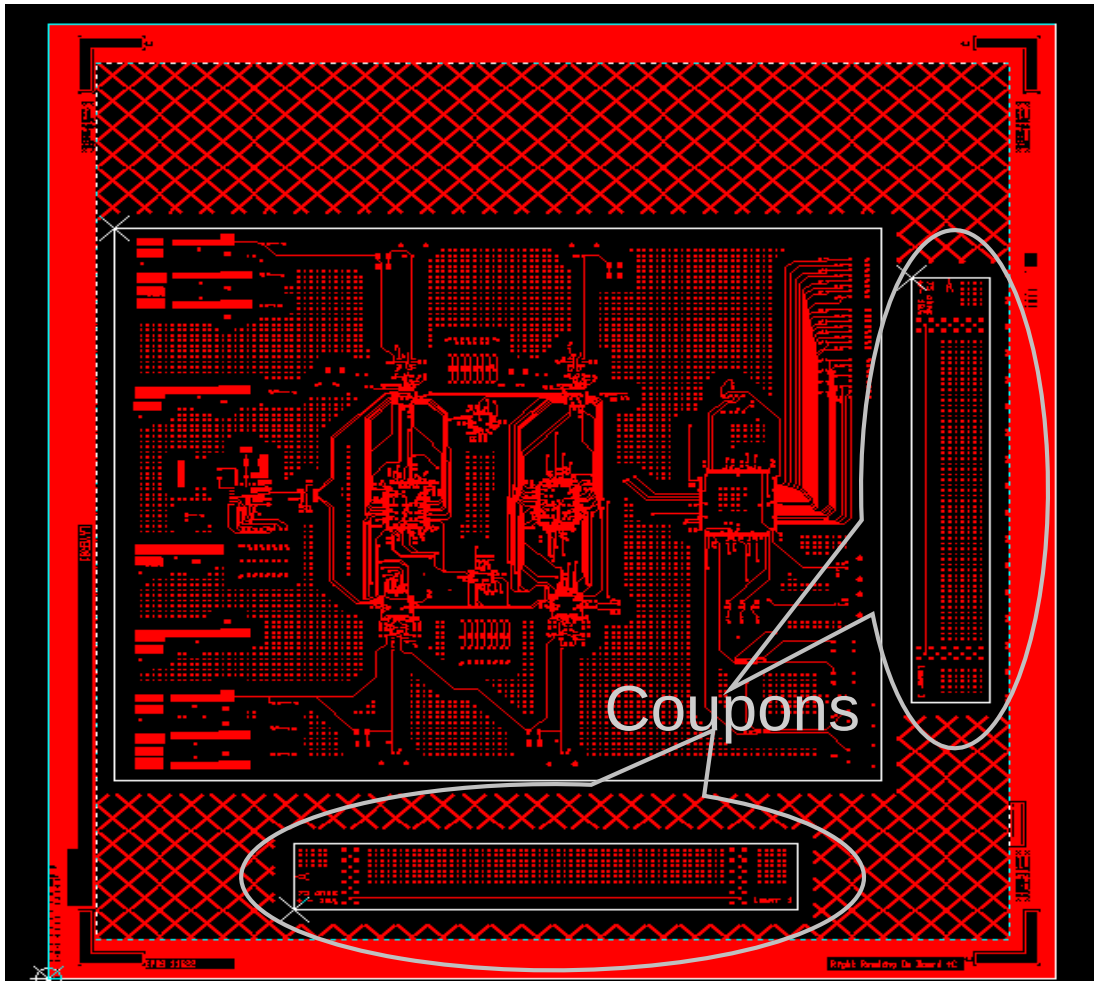
Routing (includes second stage drilling)

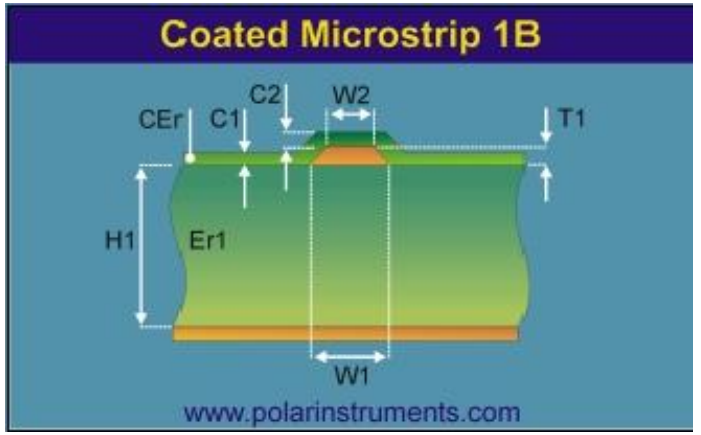


Impedance Considerations

- Controlled Impedance coupons are routed from the panel
- Good controls are necessary to ensure that coupons can be matched to manufacturing panels

Process finished PCB and coupons for testing

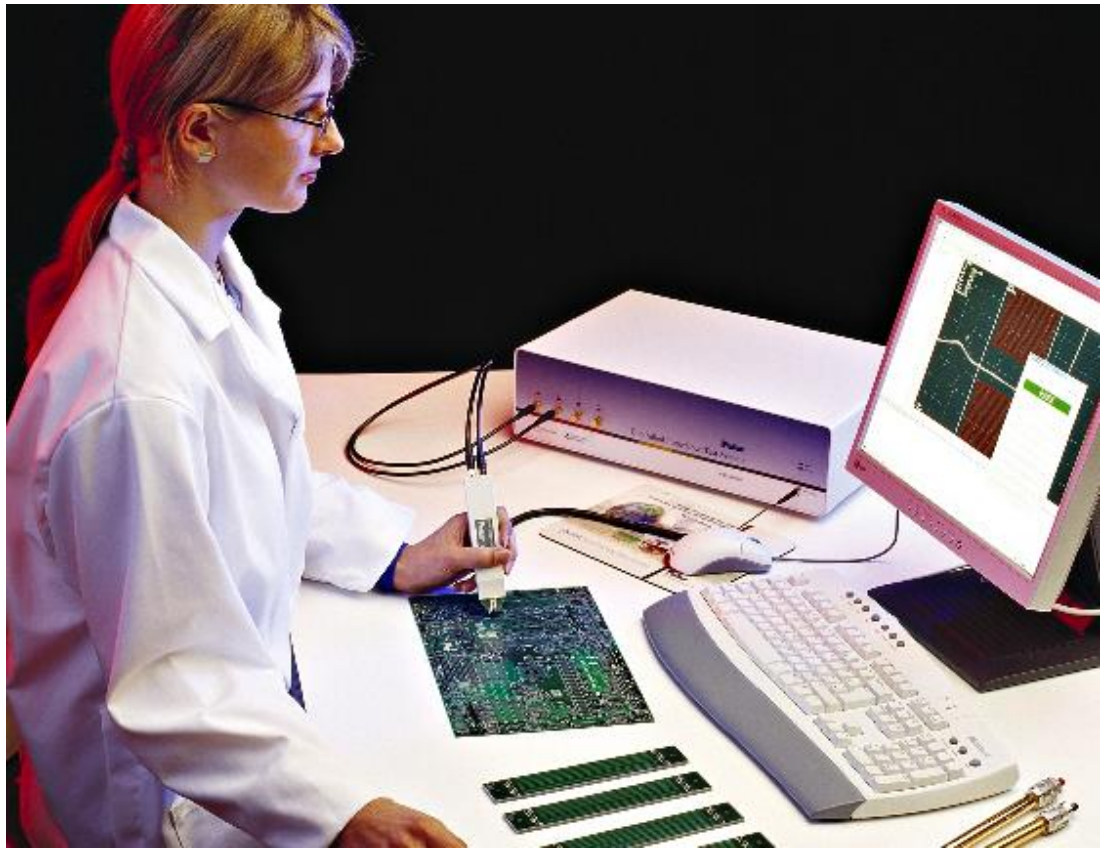


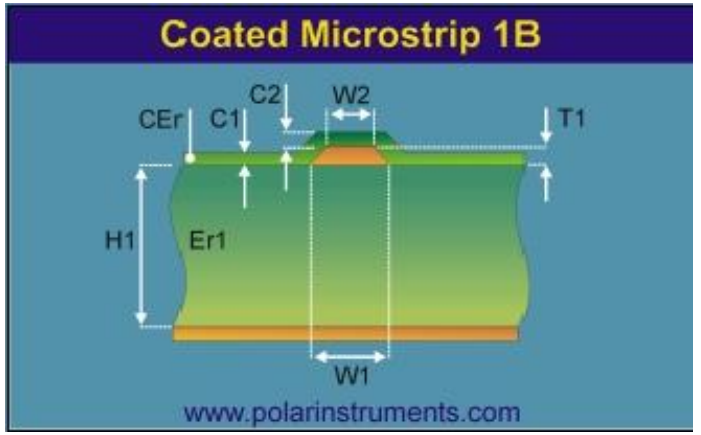


Impedance Considerations

- It is good practice to place TDR coupons in the “X” and “Y” axis of the manufacturing panel to ascertain any process variations due to spray patterns when using horizontal conveyorised equipment.

Process finished PCB and coupon for testing

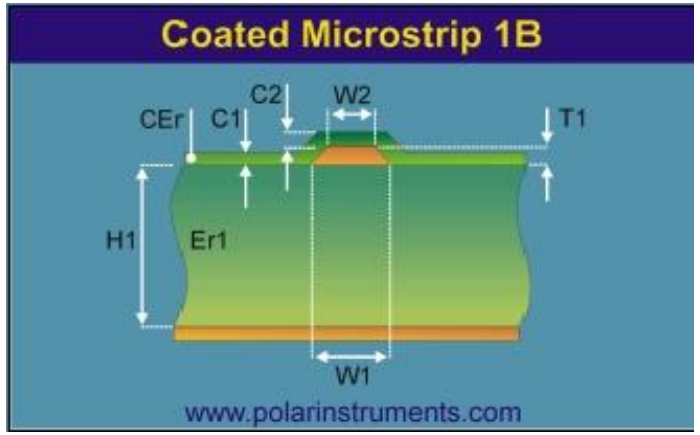




Impedance Considerations

- Controlled Impedance coupons are routed from the panel
- Controls are necessary to ensure that coupons can be matched to manufacturing panels — this should be performed on trial panels prior to production ramp up.

Why as a designer do you need to discuss your design with your PCB fabricator?



PCB manufacture is a process, it uses materials which are not “ideal”

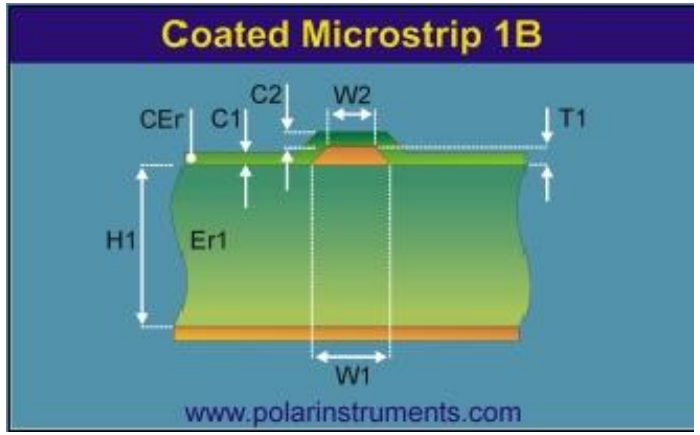
FR4 for example is a glass resin mix made of two substances with differing electrical properties.

PCB Manufacturers need to make small adjustments to designs to maximise yields

Impedance Considerations

- Glass Er 6
- Resin Er 3 (FR4)
- Resin Er < 3 (High performance laminates)

Why as a designer do you need to discuss your design with your PCB fabricator?



Process varies from one fabricator to another.

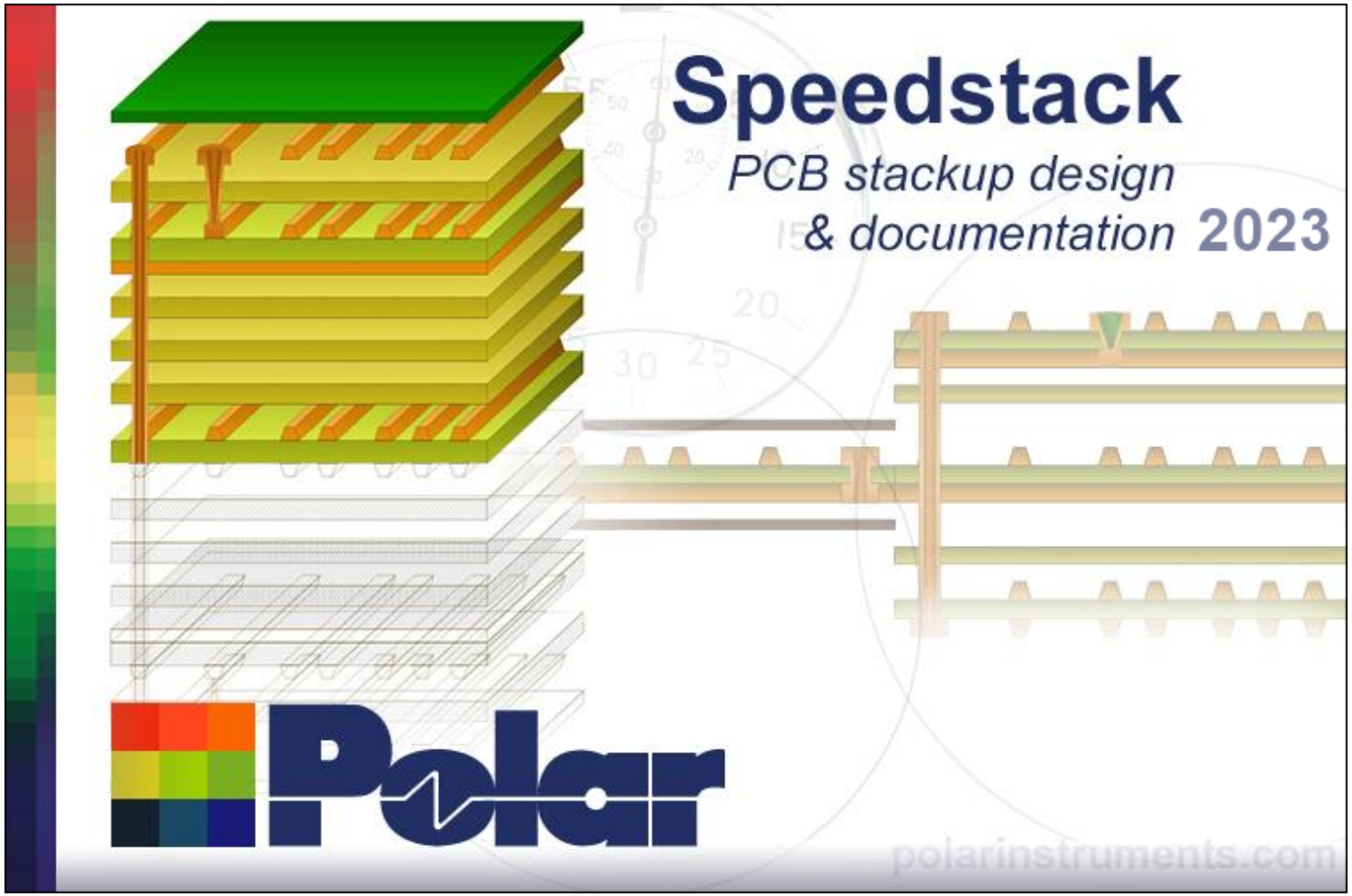
Press pressures temperatures may vary

Prepreg and core may vary from one supplier to another.

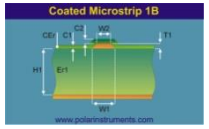
Impedance Considerations

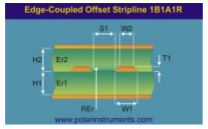
- Supplier variations

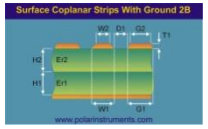
Polar tools to assist in layer stackup: Speedstack PCB Stackup design system

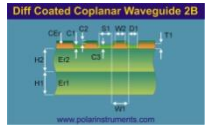


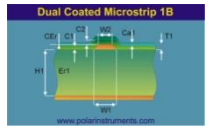
Polar tools to assist in impedance prediction: Si8000m Controlled impedance design system

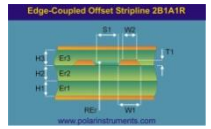


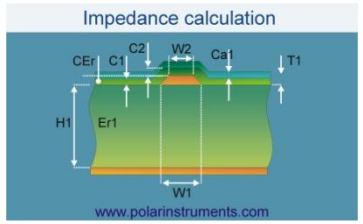


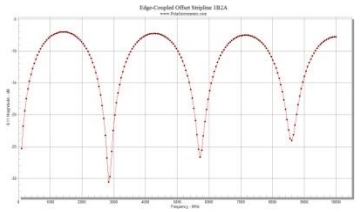


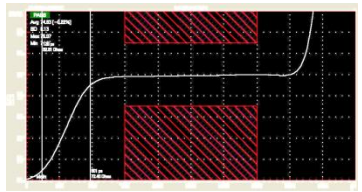


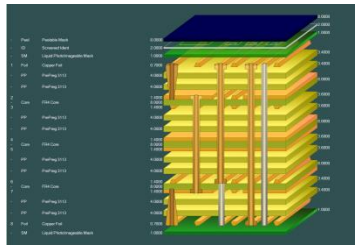


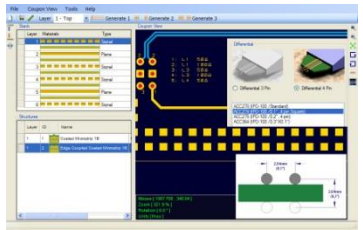












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