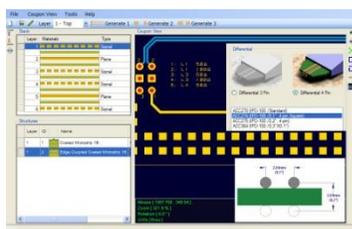
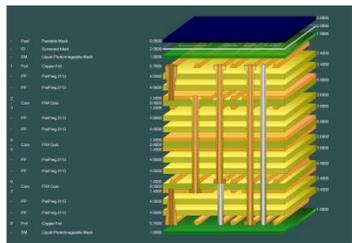
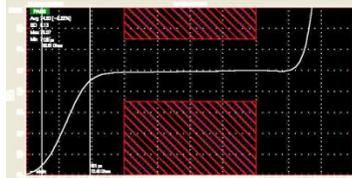
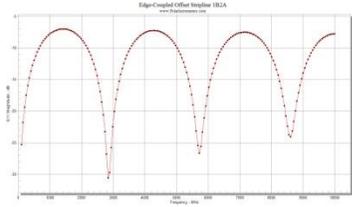
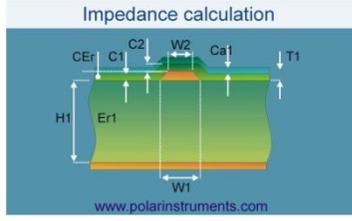


Getting Started with Speedstack

Richard Attrill - July 2016



Welcome to Speedstack

This Getting Started tutorial will familiarize you with the features and operation of Polar's Speedstack PCB Stackup Builder and guide you through the steps to create a Speedstack project (.sci) file. The completed project file is available as a free download from the Polar Instruments web site.

[Download](#) the project file for reference and help in creating your own projects.

Welcome to Speedstack

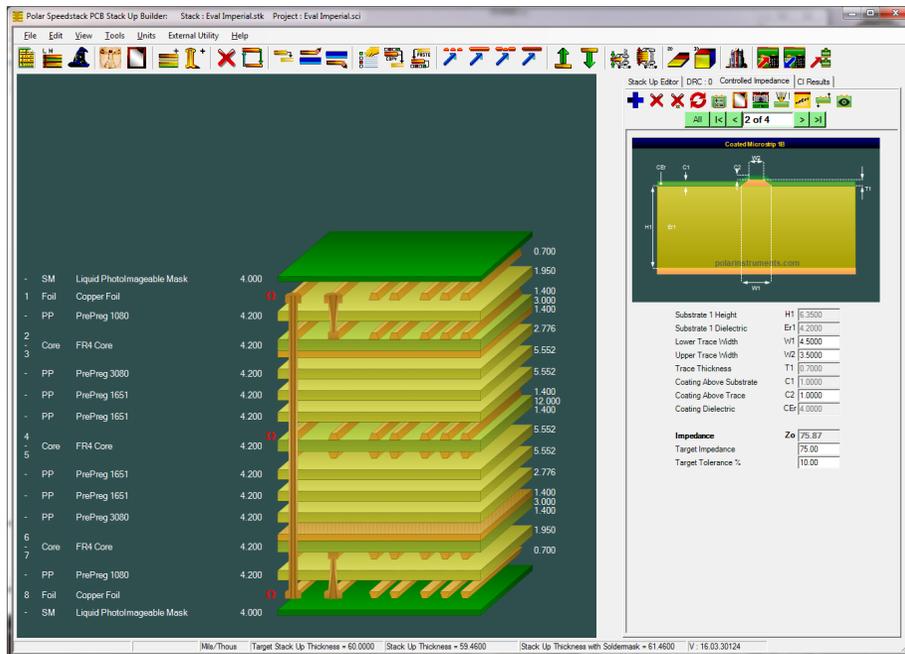
Speedstack is a comprehensive stack up design environment for pre-layout engineers, PCB fabricators and value-add PCB brokers. By collating libraries of materials, costs and suppliers with critical design data, such as transmission line specifications or impedance control, Speedstack lets you produce accurate build documentation.

Speedstack's end-to-end approach to stack up design allows you to create documents that can be shared at every stage of the PCB supply chain and drastically reduces the time you need to create, document and control PCB layer stack ups.

Speedstack links directly with the Si8000m Controlled Impedance and the Si9000e Transmission Line Design field solvers

Controlled Impedance and Insertion Loss Modelling

Speedstack



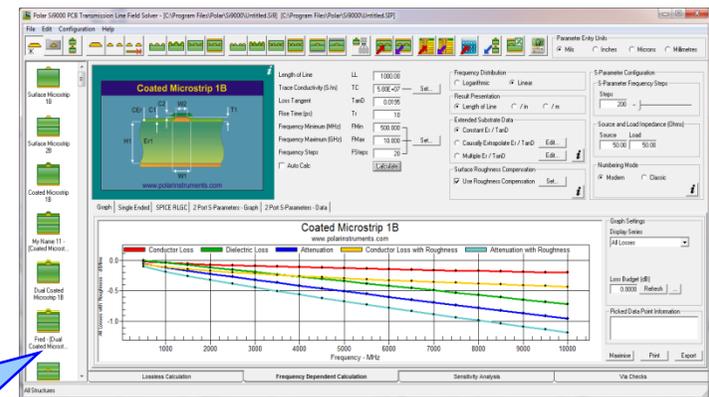
Si8000m Controlled Impedance System



Si8000m



Si9000e



Si9000e Loss Modelling System

Speedstack – Methods of creating stackups

Speedstack has two key methods to create stack ups:

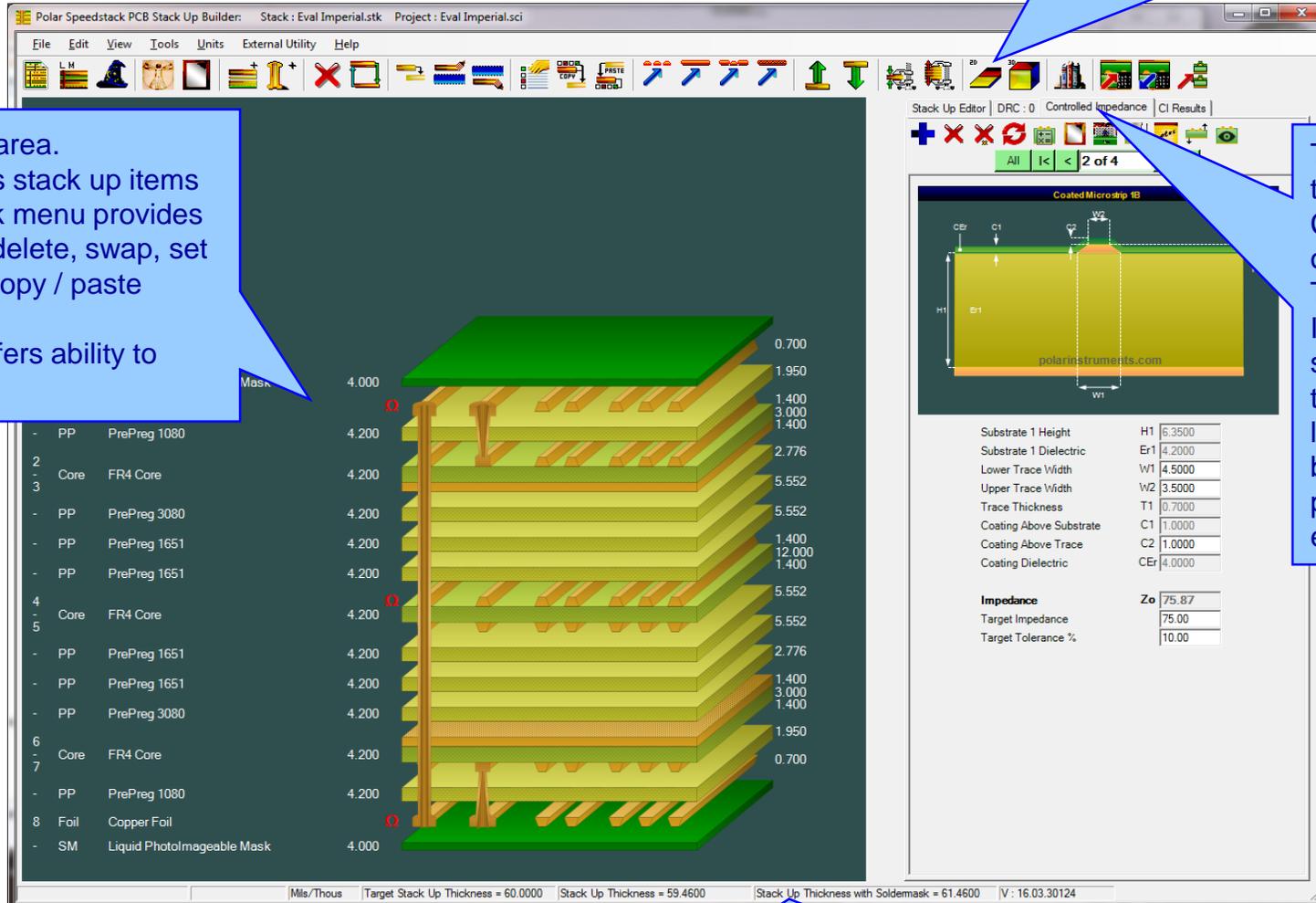
- Virtual Material Mode (VMM) – uses ‘virtual’ materials to generate stack ups. This is useful for exploring design options before committing to real materials.
- Material Library Mode – uses real materials to generate stack ups by referencing the Speedstack material library. This method provides an absolute definition of the stack up down to the exact materials used in the build.

The principle of building stack ups with Speedstack is the same regardless of the method used. The following slides will guide you through the process.

Speedstack – Introducing the interface

Toolbar provides access to commonly used functions included add, delete and swap materials.

Stack up editor area.
 Left-click selects stack up items (blue), right-click menu provides options to add, delete, swap, set properties and copy / paste materials.
 Mouse wheel offers ability to zoom in / out



Tabs provide access to Stack Up, DRC and Controlled Impedance options.
 The Controlled Impedance tab allows structures to be added to the stack on a per layer basis. The browser buttons provide access to each structure

Stack up thickness can be monitored via the status bar

Building a stack up from scratch

The following slides will guide you through the process of creating an 8 layer stack up. The stack has the following specification:

Units: Mils

Number of Layers: 8

Target Stack Up Thickness: 60 mils \pm 10%

Signal Layers: 1, 3, 6, 8 Plane Layers: 2, 4, 5, 7. Symmetrical build

Material: Standard FR4, nominal dielectric constant \sim 4.2

Preferred Core Thickness: 8 mils

Copper Thickness: All layers 1oz copper, 1.4 mils

Building a stack up from scratch (continued)

Solder Mask: Covering outer layers, 1 mil

PTH drill passes: layers 1 – 8

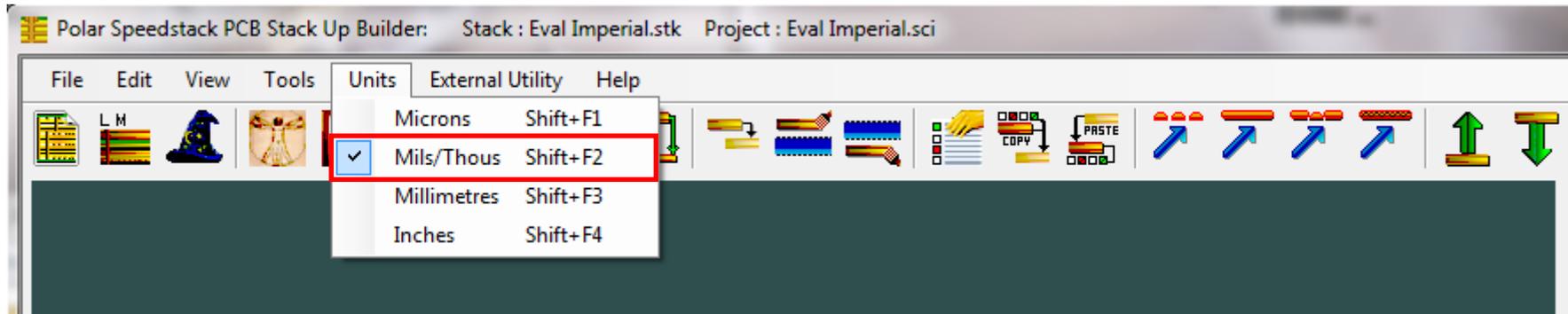
Laser microvia passes: layers 1 – 2, 8 – 7

Singled-ended impedance: 50 ohms \pm 10% on layers 1, 3, 6, 8

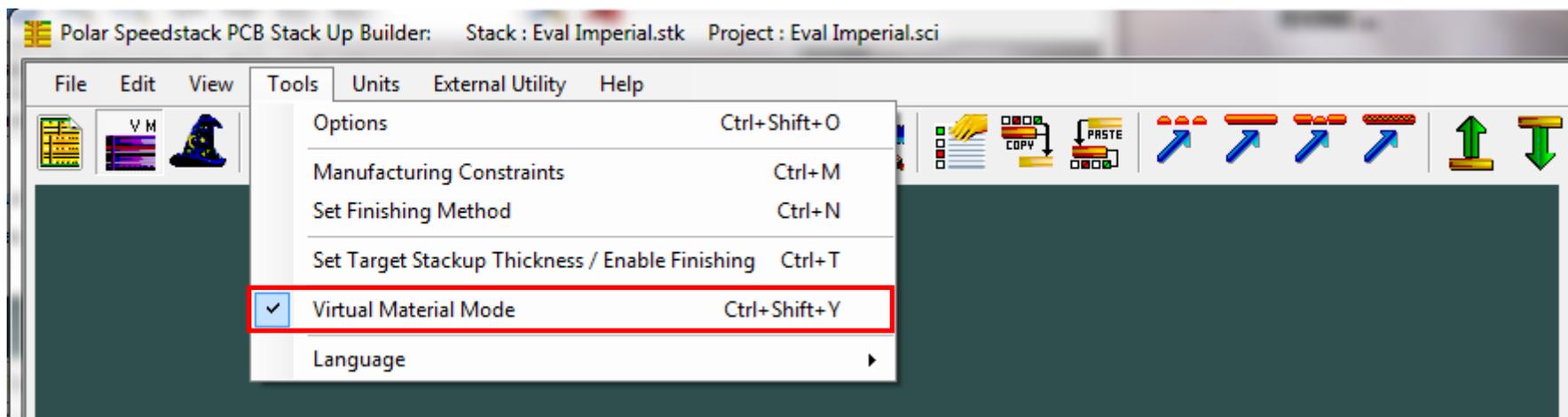
Differential impedance: 100 ohms \pm 10% on layers 1, 3, 6, 8

Step 1: Setting the Units and Virtual Material Mode

From the Units menu select the 'Mils/Thou' option



From the Tools menu select the 'Virtual Material Mode' option



Step 2: Using the Stack Up Wizard to rapidly build the stack up

Select the Stackup Wizard toolbar icon 

Stack Up Wizard (Virtual Material Mode)

Number of Layers	8	Nominal Dielectric Constant	4.2
Target Stack Up Thickness	60.0000	Solder Mask Top	<input checked="" type="checkbox"/>
Positive Tolerance %	10	Solder Mask Bottom	<input checked="" type="checkbox"/>
Negative Tolerance %	10	Solder Mask Dielectric Constant	4
Symmetrical	<input checked="" type="checkbox"/>	Solder Mask Thickness	1.0000
Plane Layers	Mixed Layers	Preferred Core Thickness	Select 8
1	1	Copper Thickness	1.4000
2	2		
3	3		
4	4		
5	5		
6	6		
7	7		
8	8		

Build Type

Foil Core Sequential/HDI

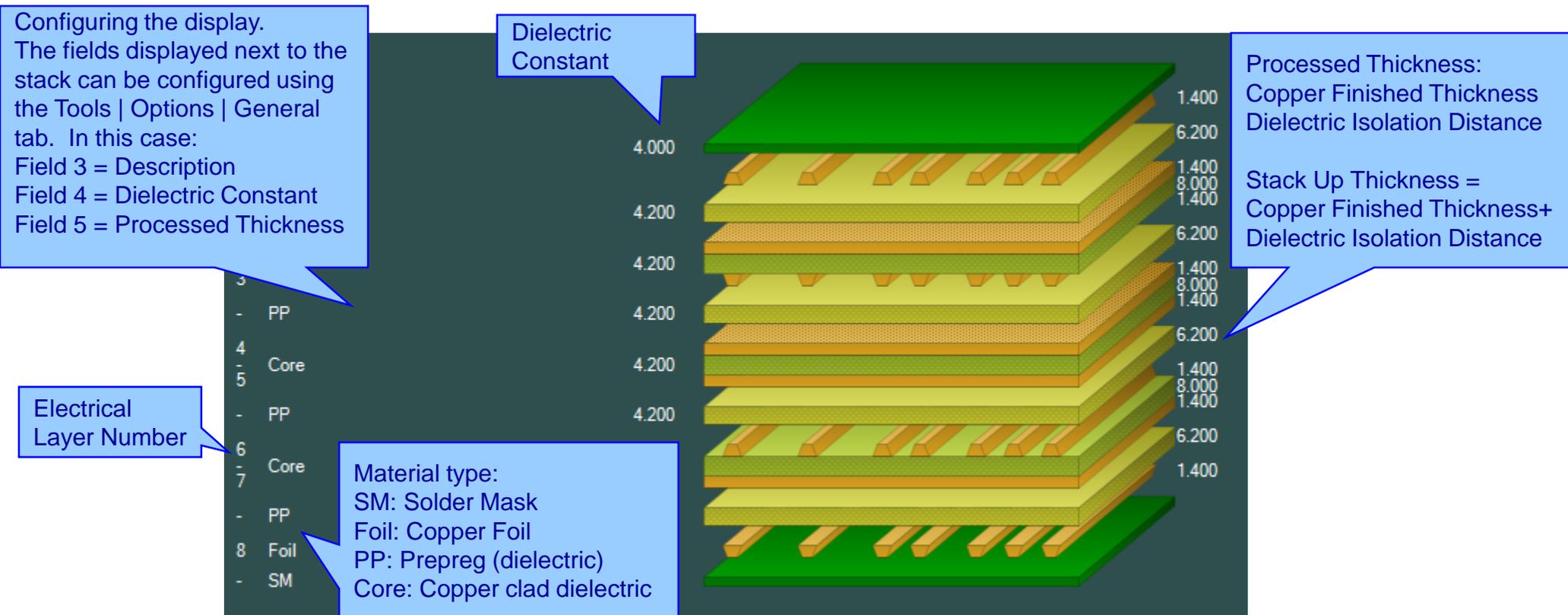
<Previous Next > Finish Cancel

- Enter the Basic Stack Data as previously described in the stack up specification
- The Number of Layers dropdown will populate the Plane Layers and Mixed Layers lists
- The Symmetrical checkbox setting will control how the Plane Layers are selected
- Once the fields are populated select the Finish button

Step 2: Using the Stack Up Wizard (continued)

An option to enter the Stack Up Properties can be skipped

The stack up created by the Wizard will now be displayed



Step 3: Saving the Speedstack project

Now that a stack has been created we can save it

Use the File | Save Project As menu option and specify a filename

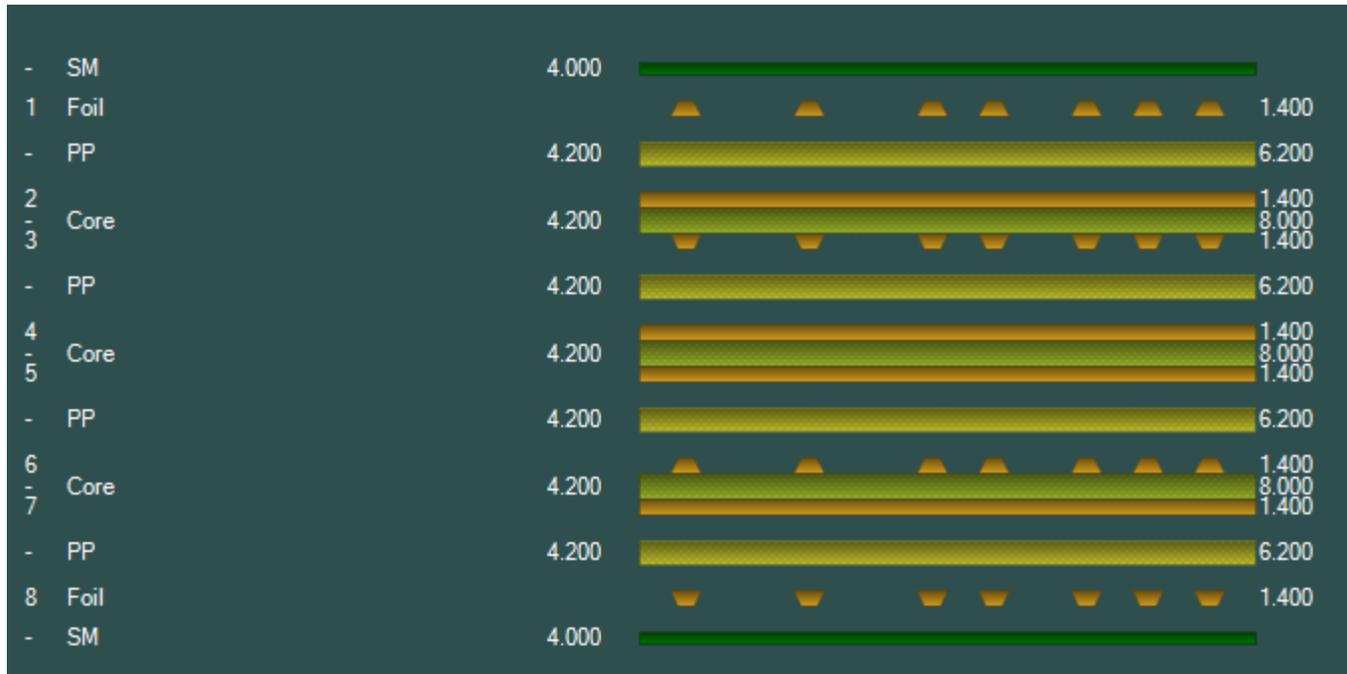
The filename will have a .SCI extension, recognisable by this icon 

Step 4: Switching between 3D and 2D display modes

It is sometimes easier to view stack up in 2D by selecting



This will result in the following stack up display



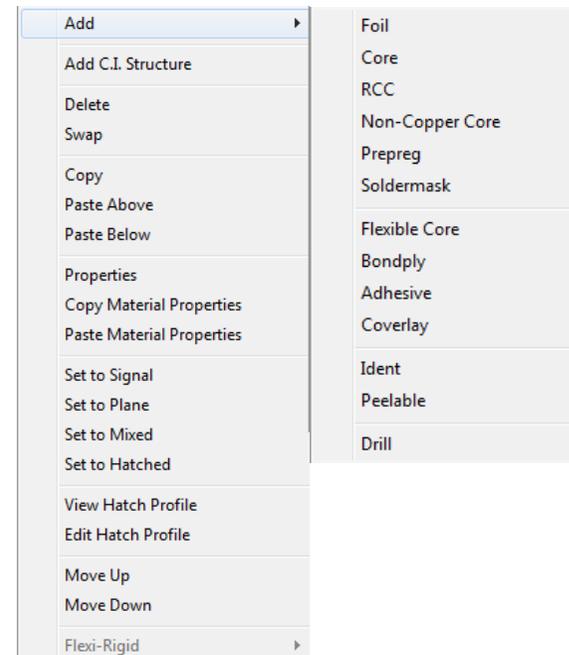
The 3D display mode can be activated by selecting



Step 4: Editing the stack up

Once the stack up has been created using the Wizard it is possible to make changes on a per material basis using the various editing functions

- Click on the material that you wish to edit
- Selected material will highlight in blue
- Use the right-click menu and select option or use toolbar icons



Step 4: Editing the stack up (continued)

Add: Adds the chosen material above or below the selected item



Delete: Removes the selected material



Swap: Swaps material with another of the same type



Copy: Copies the selected material to clipboard



Paste Above: Pastes the copied material above selected item



Paste Below: Pastes the copied material below selected item



Move Up: Move the selected material up one position



Move Down: Move the selected material down one position



Properties: Change the properties of the selected material



Step 4: Editing the stack up – electrical layers only

Signal: Set electrical layer to signal



Plane: Set electrical layer to plane



Mixed: Set electrical layer to mixed



Hatched: Set electrical layer to hatched (separately licensed)



Setting the electrical layer types on the stack up will allow Speedstack to guide you through the process of adding controlled impedance structures. It will suggest the appropriate structure based on the signal layer and plane layer positions within the stack. More details will be shown in Step 6.

Step 4: Editing the stack up – symmetrical mode

Many stack ups are symmetrical, so viewing from the centre the upper and lower sections of the stack up have exactly the same materials

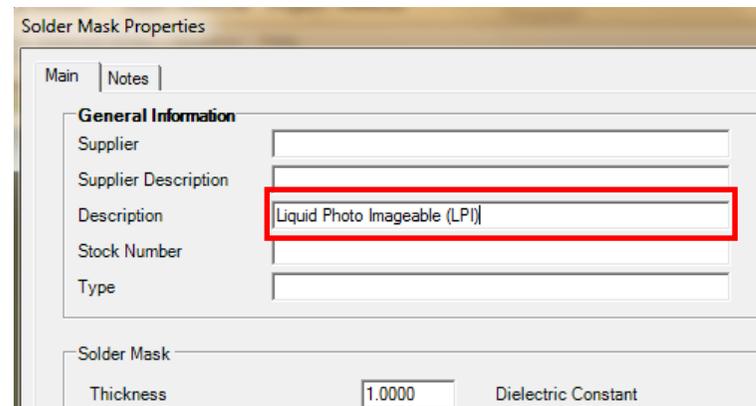
Speedstack allows you to work in symmetrical mode by selecting  This is a toggle function, selecting this option again disables this mode

When this mode is enabled the editing functions will process both the upper and lower materials of the stack simultaneously, saving significant time.

Step 4: Editing the stack up – change material properties

All the information about each material is stored in the material properties. To change properties of the stack created by the Wizard

- Enable symmetrical mode
- Select the top solder mask layer
- Select Properties
- Enter text in the Description field
- Select Apply to store information



Solder Mask Properties

Main | Notes

General Information

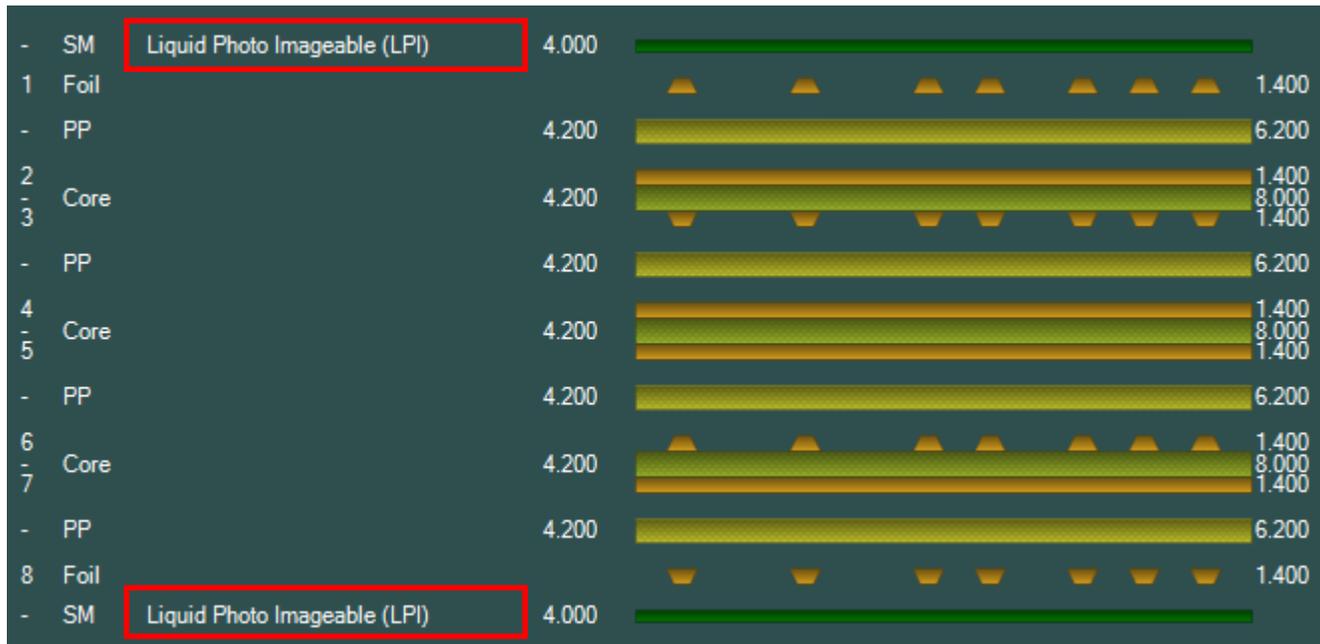
Supplier	<input type="text"/>
Supplier Description	<input type="text"/>
Description	<input type="text" value="Liquid Photo Imageable (LPI)"/>
Stock Number	<input type="text"/>
Type	<input type="text"/>

Solder Mask

Thickness	<input type="text" value="1.0000"/>	Dielectric Constant	<input type="text"/>
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Step 4: Editing the stack up – change material properties (cont'd)

The stack up will now display the solder mask description text



Step 4: Editing the stack up – change material properties (cont'd)

Repeat the process to set properties for the other materials

- Foil properties

Description	Copper Foil 1oz
-------------	-----------------

- Prepreg properties

Description	Prepreg Region
-------------	----------------

- Core properties

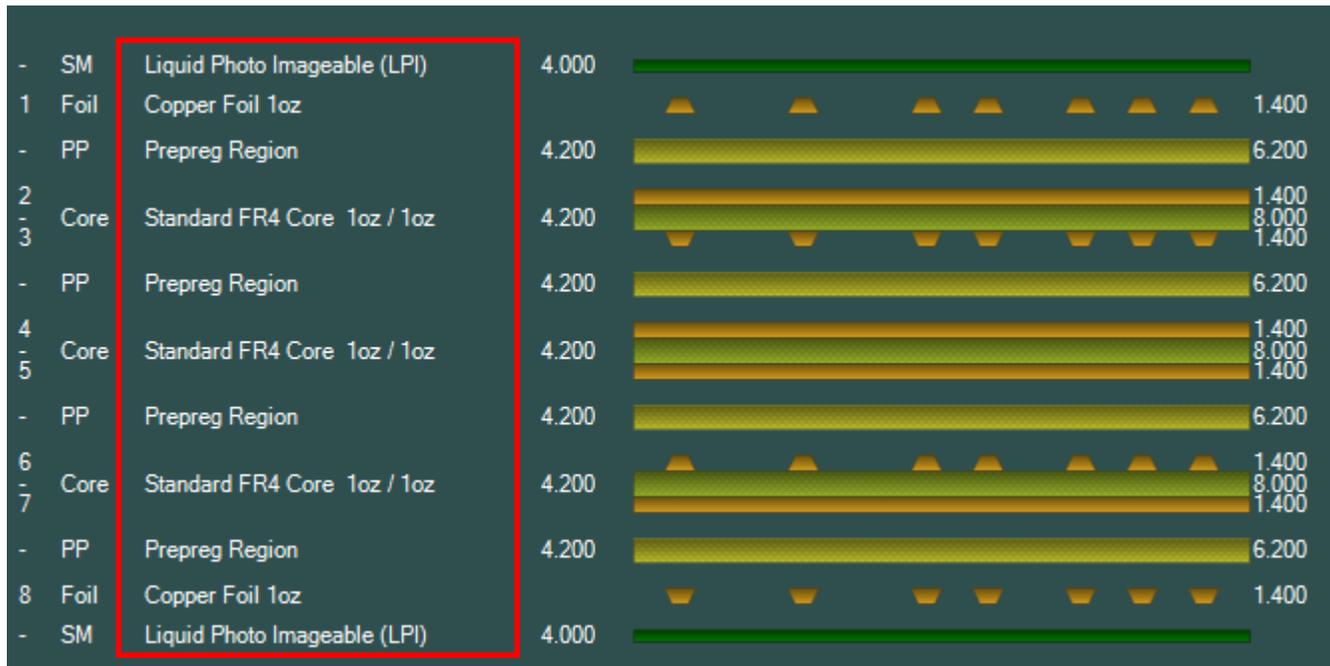
Description	Standard FR4 Core 1oz / 1oz
-------------	-----------------------------

- When complete
disable symmetrical
mode



Step 4: Editing the stack up – change material properties (cont'd)

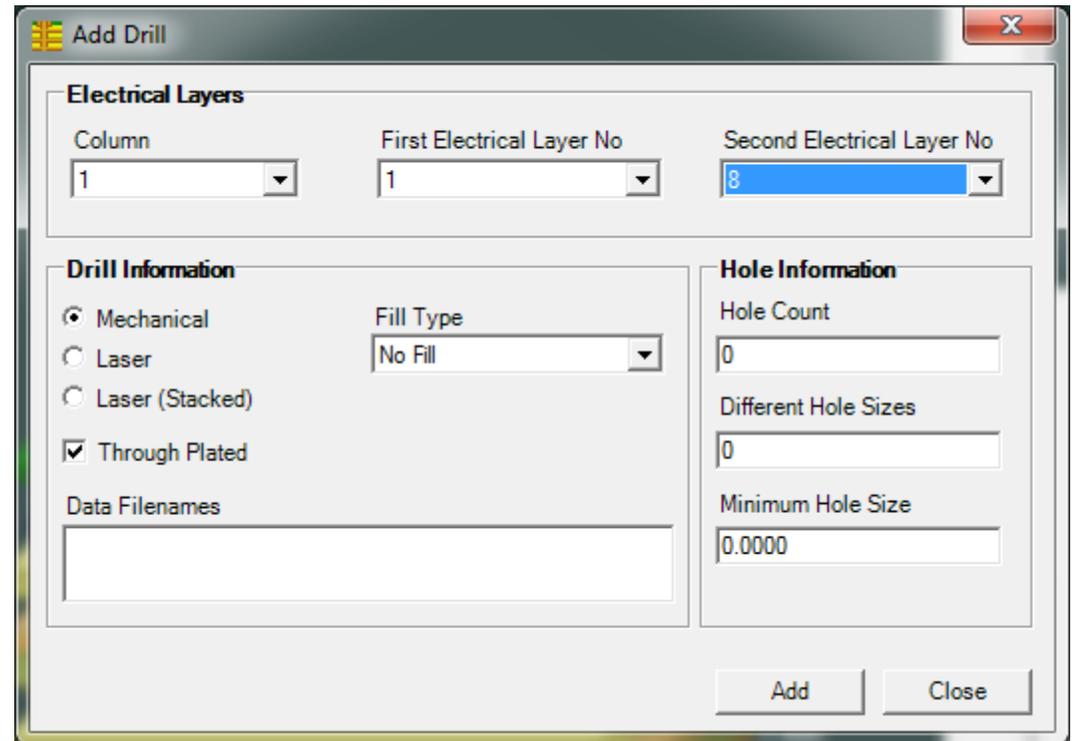
The stack up will now display description properties for all materials



Step 5: Adding drilling information

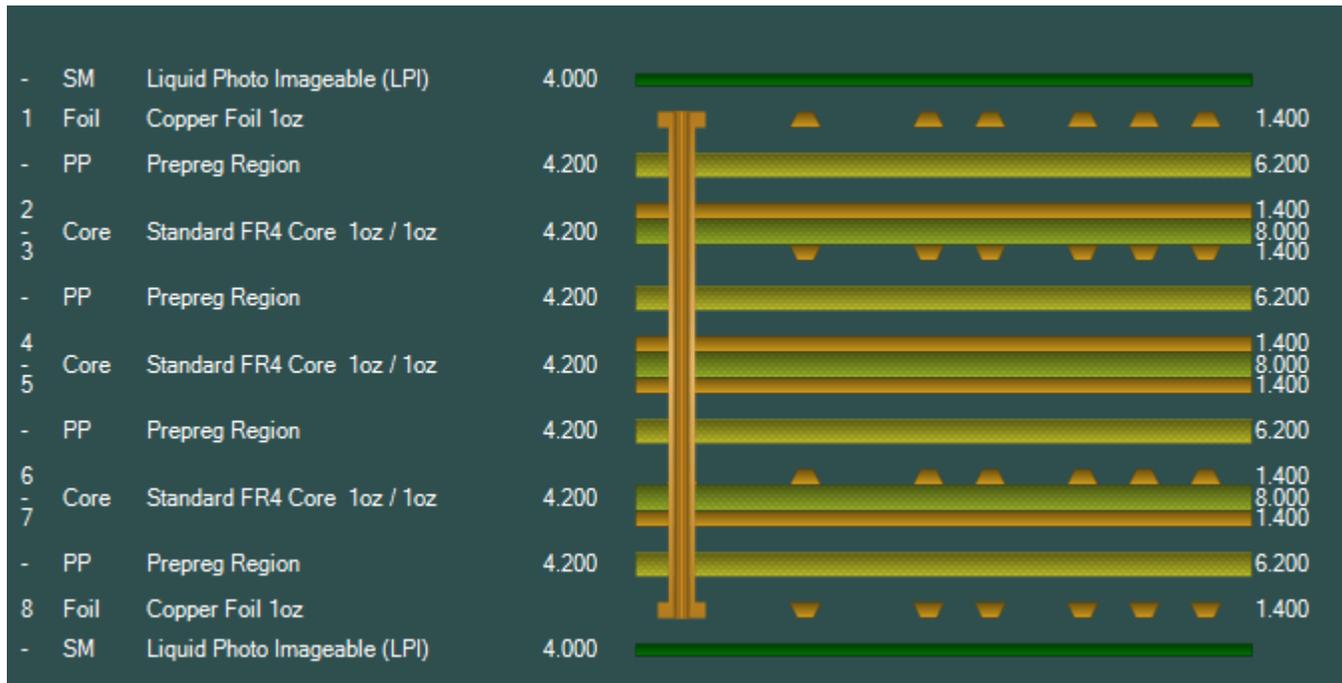
Select the Add Drill toolbar icon 

- Select the Column where the drill will be added to the stack. 1 is the left-most column.
- Set the First and Second Electrical Layer Numbers, in this case a PTH drill will start on layer 1 (top) and end on layer 8 (bottom)
- Select Add to add the drill



Step 5: Adding drilling information (continued)

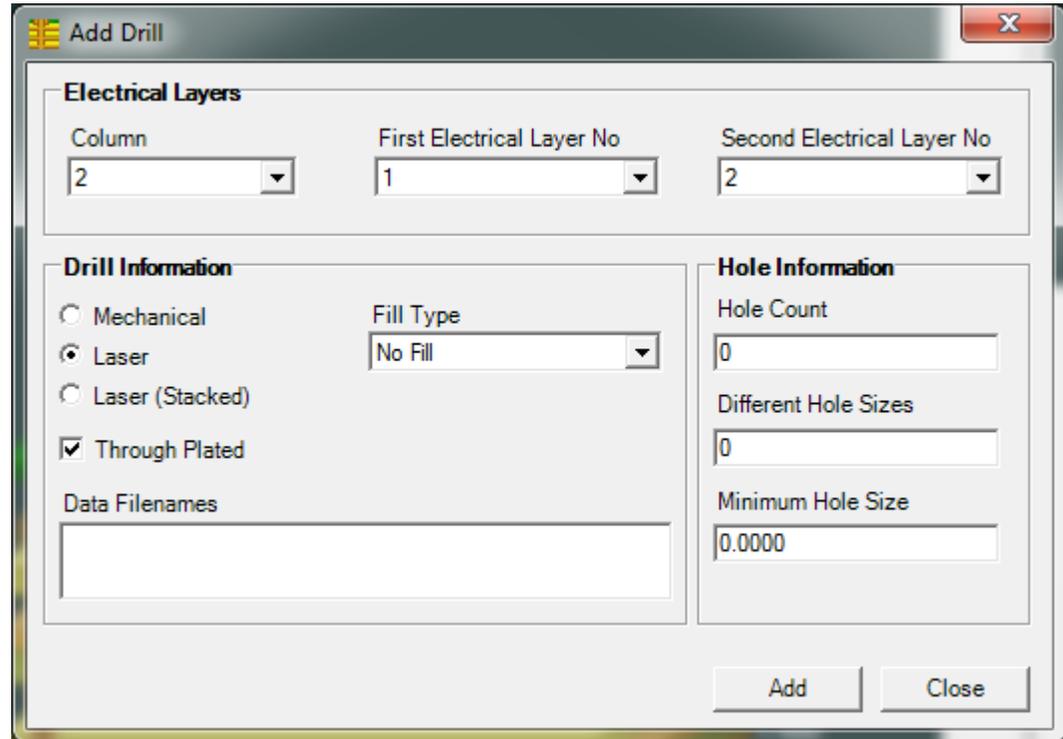
The stack up will now display the Plated Through Hole (PTH) drill



Step 5: Adding drilling information (continued)

Now we will add the laser microvias. Select the Add Drill toolbar 

- Select Column = 2
- Set the First and Second Electrical Layer Numbers, in this case the drill will start on layer 1 and end on layer 2
- Select Laser
- Select Add to add the drill
- Repeat the process, Column = 2, First = 8, Second = 7, select Laser
- Select Add to add the drill



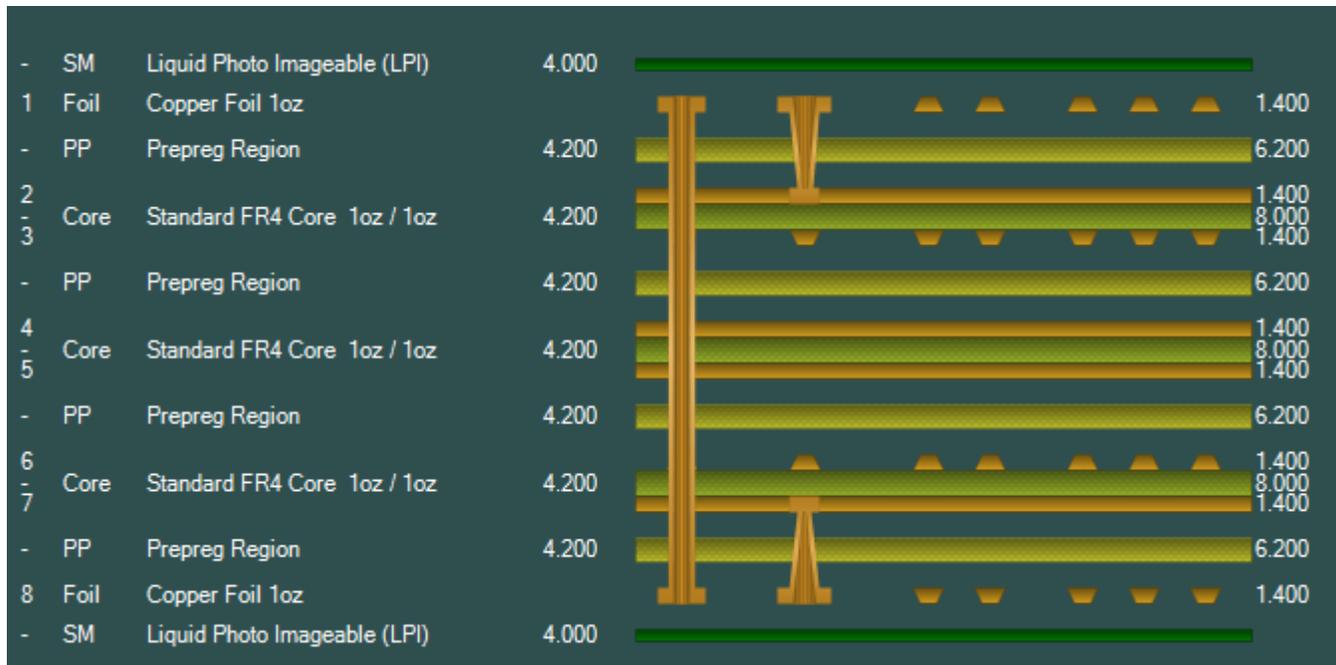
The screenshot shows the 'Add Drill' dialog box with the following settings:

- Electrical Layers:**
 - Column: 2
 - First Electrical Layer No: 1
 - Second Electrical Layer No: 2
- Drill Information:**
 - Mechanical
 - Laser
 - Laser (Stacked)
 - Through Plated
 - Fill Type: No Fill
 - Data Filenames: (empty text box)
- Hole Information:**
 - Hole Count: 0
 - Different Hole Sizes: 0
 - Minimum Hole Size: 0.0000

Buttons: Add, Close

Step 5: Adding drilling information (continued)

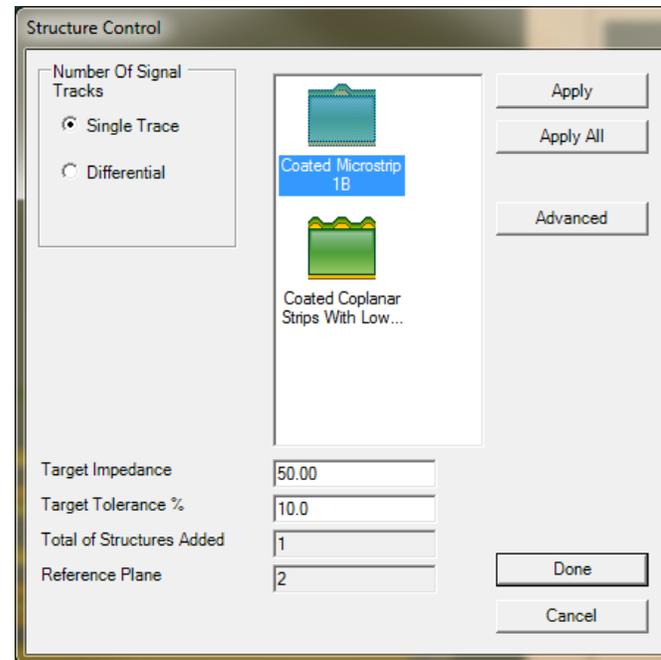
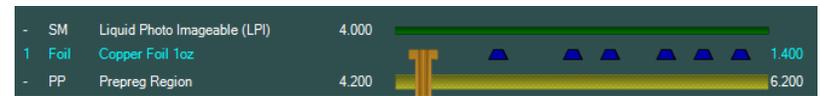
At this stage the stack up will display all the required drilling information



This is an appropriate stage to save the stack up project as described in Step 3.

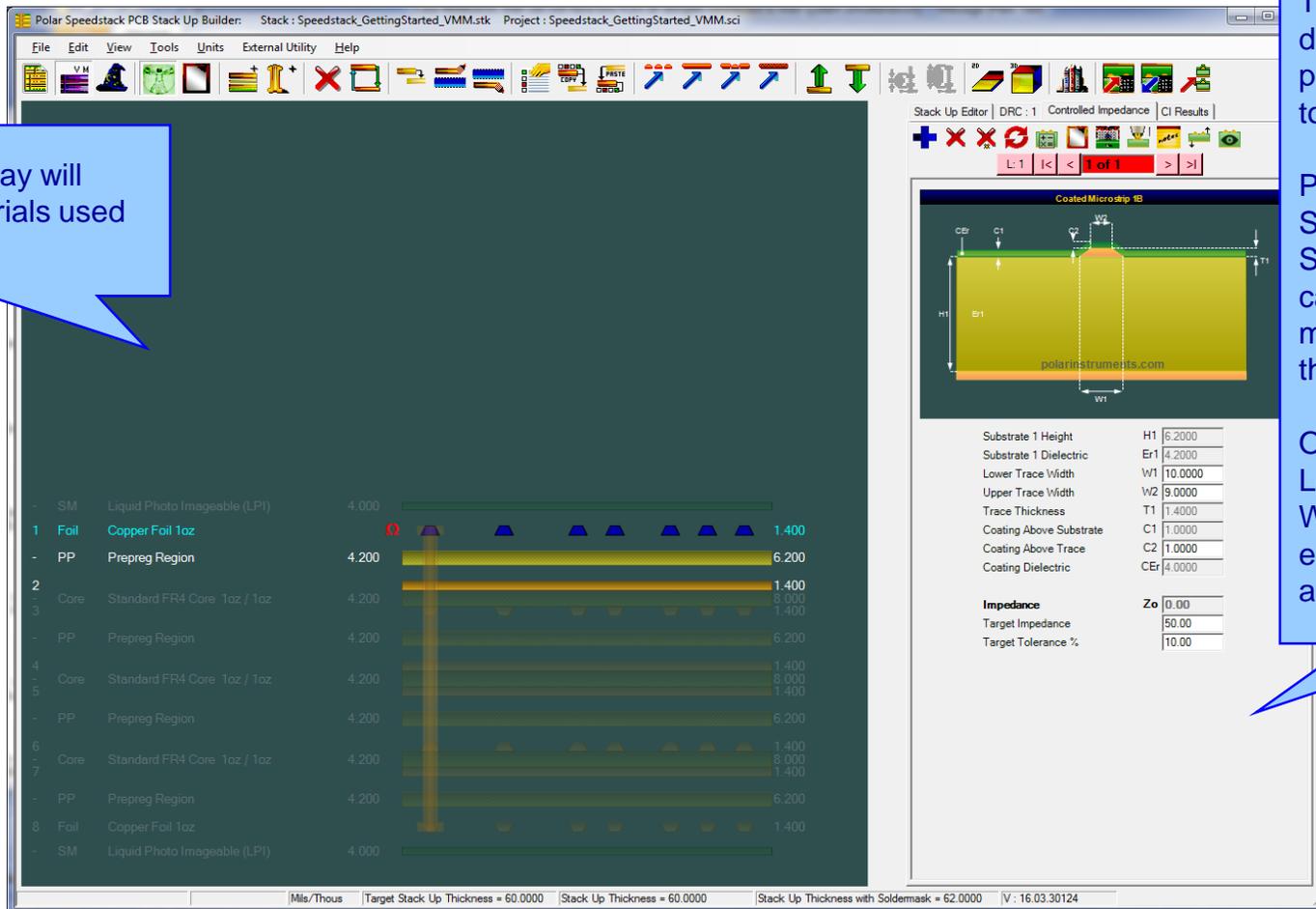
Step 6: Adding impedance structures

- Select the Controlled Impedance tab
- Click on the signal layer of the stack where the structure is to reside, in this case layer 1
- Select  to add a structure, the Structure Control dialog will be displayed. Only structures appropriate to layer 1 will be offered.
- Enter Target Impedance and Tolerance as shown, select 'Coated Microstrip 1B' icon, Apply and then Done to dismiss dialog



Step 6: Adding impedance structures (continued)

The new structure will appear on the controlled impedance tab



The stack up display will highlight the materials used by the structure

The structure image is displayed together with the parameters that are required to calculate the impedance.

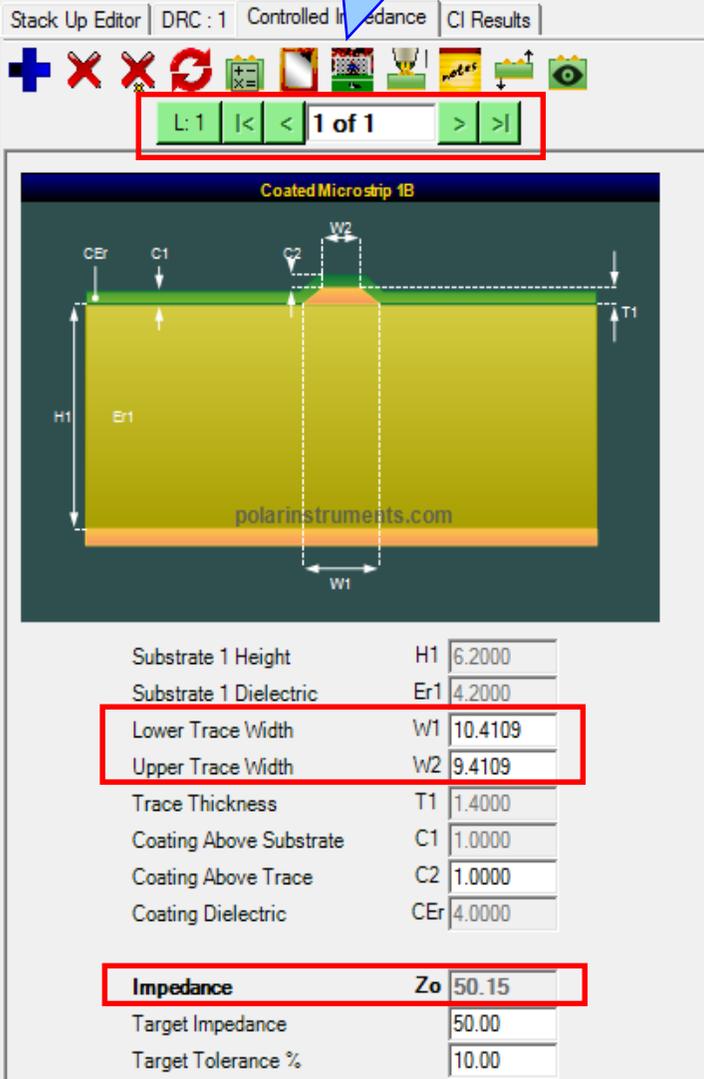
Parameters such as Substrate Height (H1) and Substrate Dielectric (Er1) are calculated from the stack up materials used. Therefore, they are read-only.

Other parameters such as Lower and Upper Trace Widths (W1 / W2) may be entered by the user, these are read/write fields.

Step 6: Adding impedance structures (continued)

- Key in the desired trace widths
- Click on the  to Rebuild and Calculate the impedance structures
- Notice that the Impedance (Z_0) result updates
- Use the  option to Goal Seek parameter(s) in order that the Target Impedance is met. Select 'W1 / W2 only' and watch Speedstack adjust these parameters to achieve the 50 ohms Target Impedance
- Notice that the trace widths (W1/W2) and the impedance results (Z_0) updates
- Green indicator denotes within tolerance

Goal Seek option



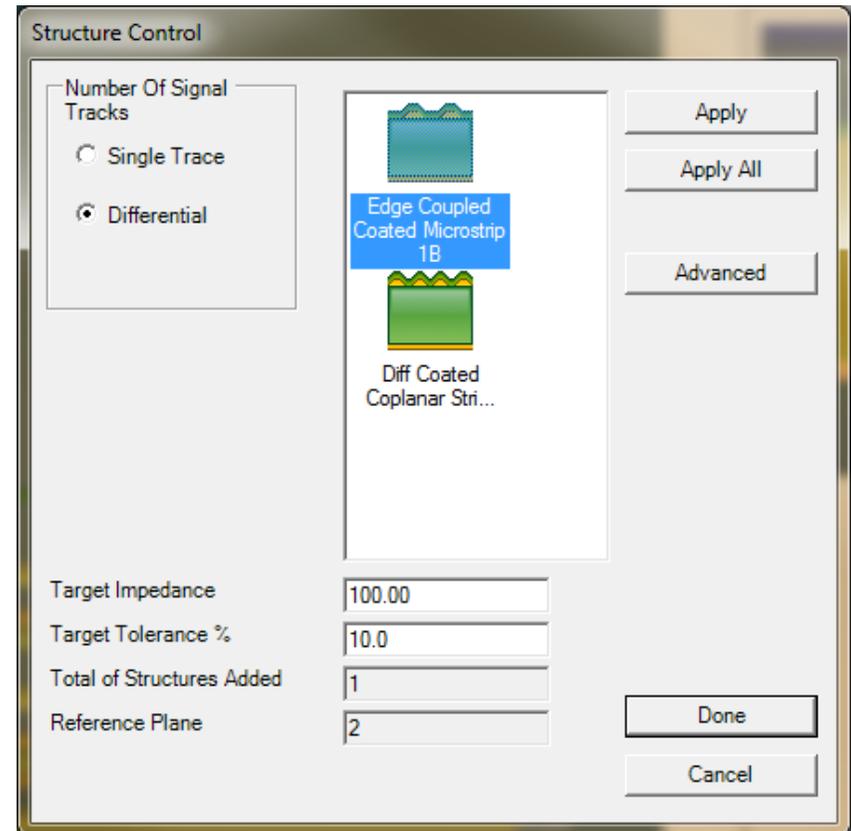
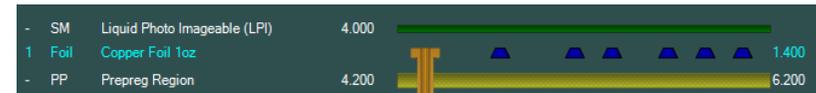
The screenshot shows the 'Stack Up Editor' interface for a 'Controlled Impedance' design. A callout points to the 'Goal Seek option' icon in the toolbar. The main view displays a cross-section of a 'Coated Microstrip 1B' with parameters labeled: C_{Er} , C_1 , C_2 , W_2 , H_1 , E_{r1} , T_1 , and W_1 . Below the diagram is a table of parameters:

Substrate 1 Height	H1	6.2000
Substrate 1 Dielectric	Er1	4.2000
Lower Trace Width	W1	10.4109
Upper Trace Width	W2	9.4109
Trace Thickness	T1	1.4000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Dielectric	CEr	4.0000
Impedance	Zo	50.15
Target Impedance		50.00
Target Tolerance %		10.00

The 'Lower Trace Width' (W1) and 'Upper Trace Width' (W2) rows in the table are highlighted with a red box. The 'Impedance' (Zo) row is also highlighted with a red box, showing a value of 50.15, which is within the 10% target tolerance of 50.00.

Step 6: Adding impedance structures - differential

- Click on layer 1 of stack
- Select **+** to add a structure, select Differential, enter Target Impedance and Tolerance as shown, choose 'Edge Coupled Coated Microstrip 1B', Apply and then Done to dismiss dialog
- The differential structure will be added to the stack. Notice that this is structure 2 of 2.



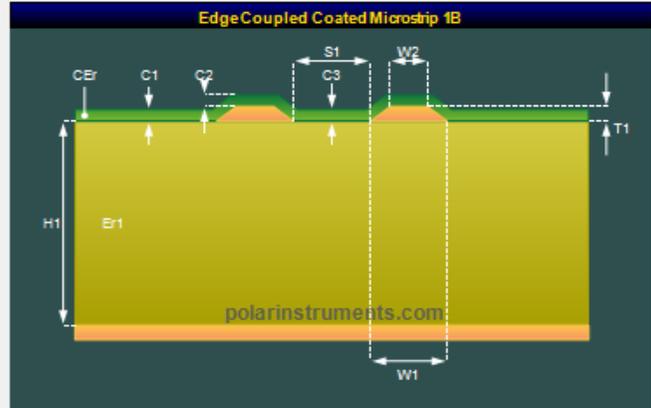
Step 6: Adding impedance structures - differential

- Key in the desired trace widths / separation
- Use the  option to Goal Seek parameter(s) in order that the Target Impedance is met. Select 'W1 / W2 constant pitch' and watch Speedstack adjust these parameters to achieve the 100 ohms Target Impedance
- Notice that the trace widths and separation (W1 / W2 / S1) and the impedance results (Zd) updates
- Green indicator denotes within tolerance

Stack Up Editor | DRC : 1 | Controlled Impedance | CI Results

L: 1 | < | > | 2 of 2

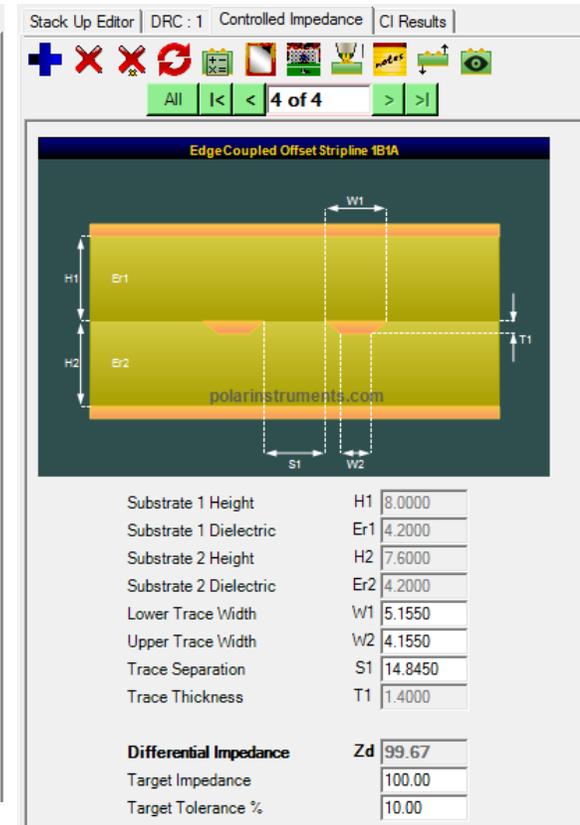
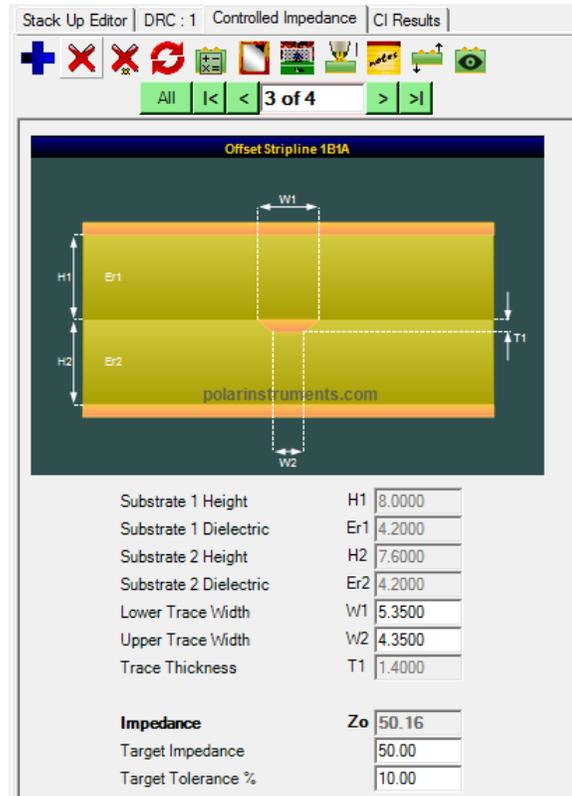
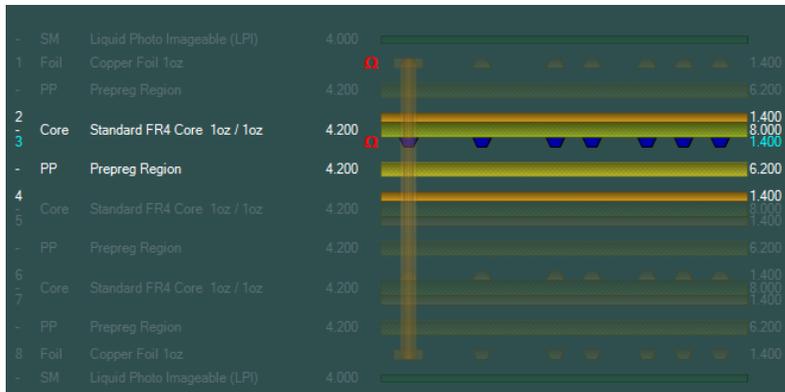
Edge Coupled Coated Microstrip 1B



Substrate 1 Height	H1	6.2000
Substrate 1 Dielectric	Er1	4.2000
Lower Trace Width	W1	8.5685
Upper Trace Width	W2	7.5685
Trace Separation	S1	11.4315
Trace Thickness	T1	1.4000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Between Traces	C3	1.0000
Coating Dielectric	CEr	4.0000
Differential Impedance	Zd	100.04
Target Impedance		100.00
Target Tolerance %		10.00

Step 6: Adding impedance structures – layer 3

Follow the same process to add single-ended 50 ohms and differential 100 ohms structures to layer 3.



Step 6: Adding impedance structures

At this point we have four structures, two on layer 1, two on layer 3

The screenshot shows the Polar Speedstack PCB Stack Up Builder interface. The main window displays a stack up editor with a table of layers and a detailed view of an edge-coupled offset stripline structure.

Omega (Ω) symbol placed next to layers that contain structures

Layer	Material	Thickness	Structure
-	SM Liquid Photo Imageable (LPI)	4.000	
1	Foil Copper Foil 1oz	1.400	Ω
-	PP Prepreg Region	4.200	
2	Core Standard FR4 Core 1oz / 1oz	1.400	
-	PP Prepreg Region	4.200	
3	Core Standard FR4 Core 1oz / 1oz	1.400	Ω
-	PP Prepreg Region	4.200	
4	Core Standard FR4 Core 1oz / 1oz	1.400	
-	PP Prepreg Region	4.200	
5	Core Standard FR4 Core 1oz / 1oz	1.400	
-	PP Prepreg Region	4.200	
6	Core Standard FR4 Core 1oz / 1oz	1.400	
-	PP Prepreg Region	4.200	
7	Core Standard FR4 Core 1oz / 1oz	1.400	
-	PP Prepreg Region	4.200	
8	Foil Copper Foil 1oz	1.400	
-	SM Liquid Photo Imageable (LPI)	4.000	

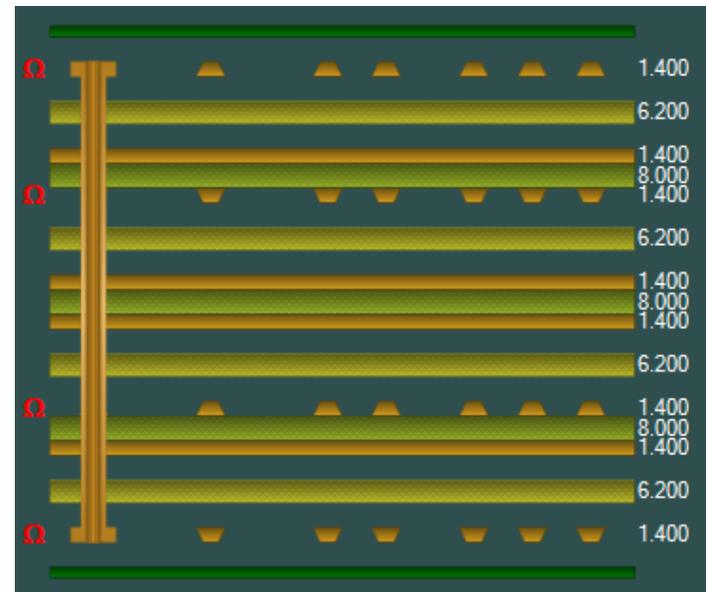
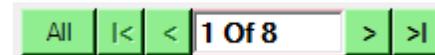
The structure browse control shows four structures

Edge Coupled Offset Stripline 1B1A

Substrate 1 Height	H1	8.0000
Substrate 1 Dielectric	Er1	4.2000
Substrate 2 Height	H2	7.6000
Substrate 2 Dielectric	Er2	4.2000
Lower Trace Width	W1	5.1740
Upper Trace Width	W2	4.1740
Trace Separation	S1	14.8260
Trace Thickness	T1	1.4000
Differential Impedance	Zd	99.51
Target Impedance		100.00
Target Tolerance %		10.00

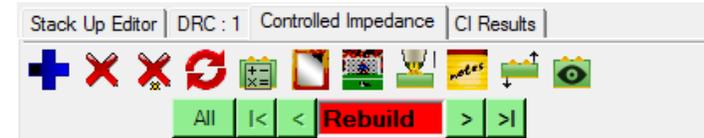
Step 6: Adding impedance structures – mirroring structures

- As the stack is symmetrical, selecting ‘Mirror Structures’ will place four more structures on the lower half of the stack
- At this point the structure browse control will display eight structures in total
- The Ω symbol is now placed next to layers 1, 3, 6, 8
- This is an appropriate stage to save the stack up project as described in Step 3.



Step 6: Impedance structures – other information

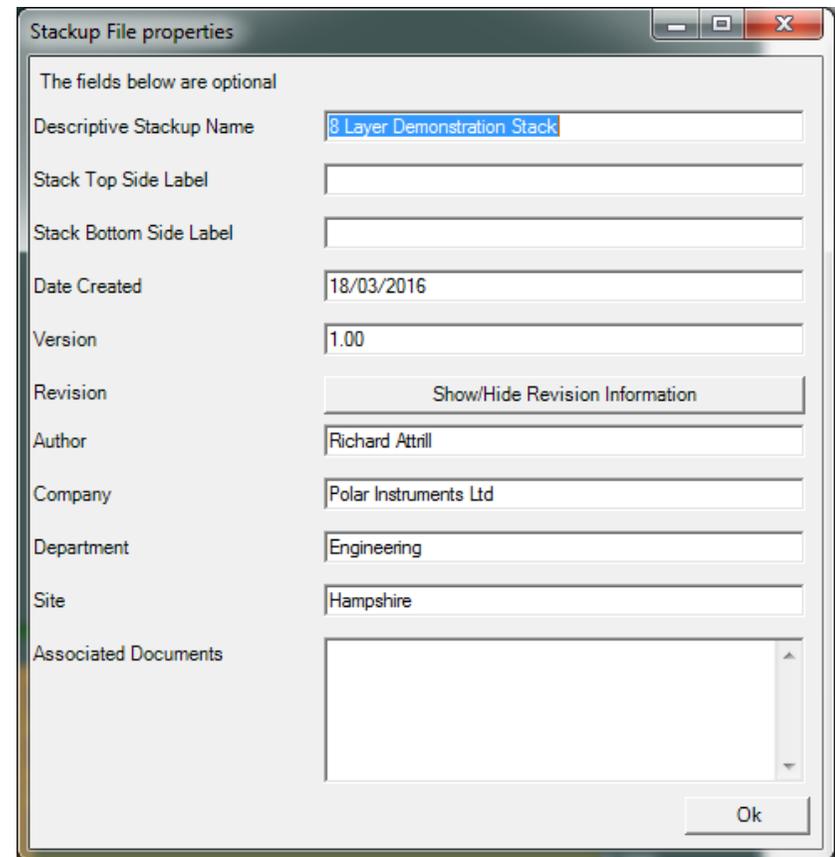
- If changes are made to the stack up that effect the impedance structures, a ‘Rebuild’ warning is displayed
- Click on the  to rebuild the structures with the latest stack up information and re-calculate the impedance results
- If the structure browse control indicator displays red it denotes a structure impedance result outside tolerance. In this case structure 2 of 8. This usually can be resolved by using the Goal Seeking function to adjust trace widths / separation



Step 7: Printing a technical report

The 8 layer stack up with its drilling and impedance structure information is now complete, the final step is to generate a technical report

- Use the File | Properties option to add useful information about the stack up, such as descriptive stack up name, date created, author and company information
- Load the Technical Report option by using the File | Print | Technical Report



Stackup File properties

The fields below are optional

Descriptive Stackup Name	8 Layer Demonstration Stack
Stack Top Side Label	
Stack Bottom Side Label	
Date Created	18/03/2016
Version	1.00
Revision	Show/Hide Revision Information
Author	Richard Attrill
Company	Polar Instruments Ltd
Department	Engineering
Site	Hampshire
Associated Documents	

Ok

Step 7: Printing a technical report (continued)

Stack up image with drilling information

Stack up information, with customisable columns

Stack up thickness info

Impedance information, with customisable columns

Stack up property info

Company logo goes here

Layer	Stack up	Description	Processed Thickness	Mask Thickness	cr	Impedance ID
1		Liquid Photo Imageable (LPI)		1.000	4.000	
2		Copper Foil 1oz	1.400			1, 2
3		Prepreg Region	6.200	4.200		
4		Standard FR4 Core 1oz / 1oz	1.400	8.000	4.200	3, 4
5		Prepreg Region	6.200	4.200		
6		Standard FR4 Core 1oz / 1oz	1.400	8.000	4.200	5, 6
7		Prepreg Region	6.200	4.200		
8		Copper Foil 1oz	1.400			7, 8
		Liquid Photo Imageable (LPI)		1.000	4.000	

Notes

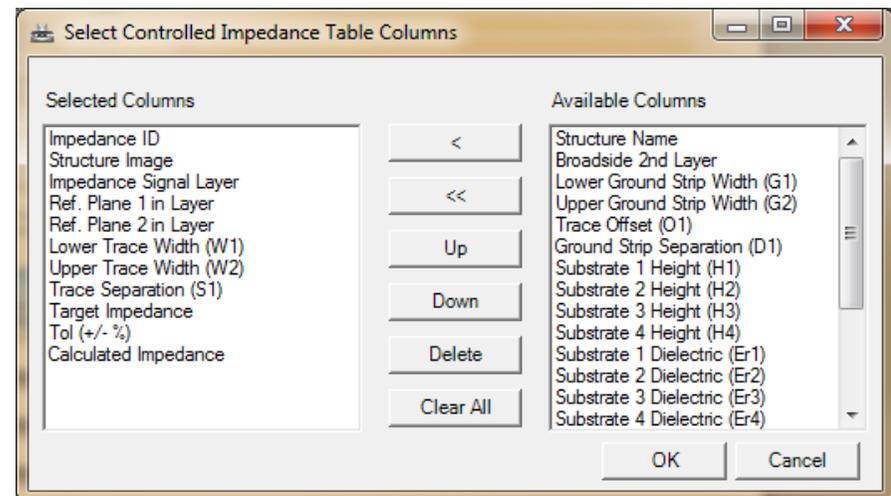
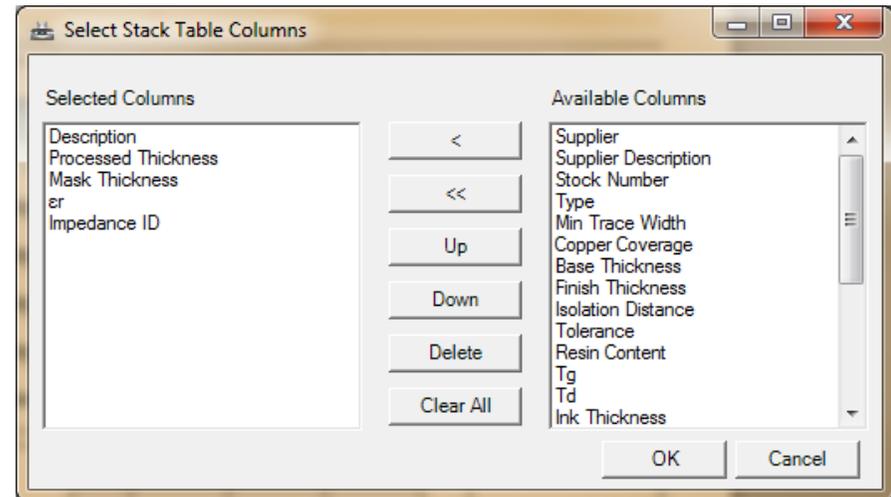
Impedance ID	Structure Image	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Target Impedance	Tol (+/- %)	Calculated Impedance
1		1	2	0	10.438	9.438	0.000	50.000	10.000	50.080
2		1	2	0	8.583	7.583	11.417	100.000	10.000	99.950
3		3	2	4	5.375	4.375	0.000	50.000	10.000	50.060
4		3	2	4	5.174	4.174	14.826	100.000	10.000	99.510
5		6	5	7	5.375	4.375	0.000	50.000	10.000	50.060

StackName: 8 Layer Demonstration Stack | Version: 1.00 | Revision: | Modification: | Date of Revision: | Editor: | Page 1/X

Date: 18/03/2016 | Associated Documents: | Author: Richard Attrill | Department: Engineering | Site: Hampshire | Copyright: | www.polar.com

Step 7: Printing a technical report (continued)

- Use the  Select Stack Data Columns option to select the fields that you wish to print next to the stack up graphic
- Use the  Select Impedance Data Columns option to configure the impedance structure table



Step 7: Printing a technical report (continued) – sample output

C:\Users\Richard Atrill\Desktop\Projects\Speedstack Getting Started Guide\Speedstack GettingStarted_VMM_CI.atk
Units: Mils


Layer	Stack up	Description	Processed Thickness	Mask Thickness	er	Impedance ID
1		Liquid Photo Imageable (LPI)		1.000	4.000	
		Copper Foil 1oz	1.400			1, 2
2		Prepreg Region	6.200	4.200		
		Standard FR4 Core 1oz / 1oz	1.400			
3		Standard FR4 Core 1oz / 1oz	8.000	4.200		3, 4
		Prepreg Region	1.400			
4		Prepreg Region	6.200	4.200		
		Standard FR4 Core 1oz / 1oz	1.400			
5		Standard FR4 Core 1oz / 1oz	8.000	4.200		
		Prepreg Region	1.400			
6		Prepreg Region	6.200	4.200		
		Standard FR4 Core 1oz / 1oz	1.400			5, 6
7		Standard FR4 Core 1oz / 1oz	8.000	4.200		
		Prepreg Region	1.400			
8		Prepreg Region	6.200	4.200		
		Copper Foil 1oz	1.400			7, 8
		Liquid Photo Imageable (LPI)		1.000	4.000	

Copper Thickness = 11.200 | Dielectric Thickness = 48.800 | Solder Mask Thickness = 2.000 | Stack Up Thickness = 60.000 | Stack Up Thickness with Soldermask = 62.000 | Stack Up Cost = 0.00 |

Notes

Impedance ID	Structure Image	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Target Impedance	Tol (+/- %)	Calculated Impedance
1		1	2	0	10.438	9.438	0.000	50.000	10.000	50.080
2		1	2	0	8.583	7.583	11.417	100.000	10.000	99.950
3		3	2	4	5.375	4.375	0.000	50.000	10.000	50.060
4		3	2	4	5.174	4.174	14.826	100.000	10.000	99.510
5		6	5	7	5.375	4.375	0.000	50.000	10.000	50.060

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Summary

Thanks for completing the Getting Started tutorial.

I hope it proved a useful introduction to the stack up creation process using Speedstack and that you enjoyed using it.

If you have any questions please feel free to contact your local Polar office at:

www.polarinstruments.com/distrib/international_offices.html

or contact us at polarcare@polarinstruments.com

Thanks again for using Speedstack.

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