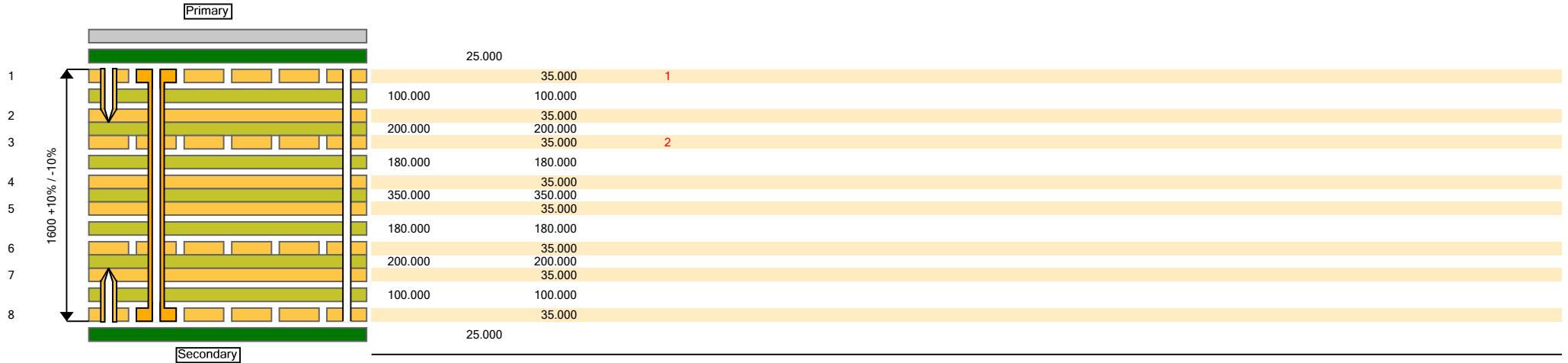


Layer	Stack up	Isolation Distance	Mask Thickness	Processed Thickness	Impedance ID
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Impedance ID	Structure Name	Impedance Signal Layer	Target Impedance	Calculated Impedance	Lower Trace Width	Upper Trace Width
1	Coated Microstrip 1B	1	50.000	49.640	165.000	140.000
2	Edge Coupled Offset Stripline 1B1A	3	100.000	100.030	130.000	110.000

- Notes**
 PCB Thickness = 1.6 mm (+/- 10%) - Board Material FR4 with a nominal Dielectric as stated above that conforms to RoHS/WEE & UL94-V0. Board Finish:-Ni/Au.
 1) Processed thicknesses (i.e. isolation distances) must be complied (within a +/- 10 % manufacturing tolerance) with to ensure consistent crosstalk characteristics and impedance.
 2) Track and gap width may be modified to meet target impedances. This must be approved by engineering Dept. before PCB manufacture can commence.
 3) If impedance targets cannot be met by modifying track geometries alone then dielectric thicknesses may be modified. This must be approved by engineering Dept. before PCB manufacture can commence.
 4) To aid manufacturing via sizes may be modified and Cross-hatching may be added to outer layers, but must be placed a least 250 thou (6.35mm) away from any tracks, pads or board outline.
 5) PCB must be tested to CAD net list supplied.
 6) Min plating down barrels of holes 25um.

Safety Markings (All PCB's MUST have the following on Component Side Ident)
 A. Manufacturer's Name or Logo. B. Manufacturer's Batch Code or Date Stamp C. UL Flammability marking:- 'UL94-V0'. "IF IN DOUBT... PLEASE ASK!"
 For Further Details Contact
 A Smith, PCB Design Dept. or R Brown, PCB Design Dept
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StackName: 8-Layer-Sample	Version: 1	Revision:	Modification:	Date of Revision:	Editor	Page 1/1
Date: 15/06/2010	Associated Documents:	A	des noted added	22-6-10	JAS	
Author: RB						
Department: Engineering						
Site: Head Office						